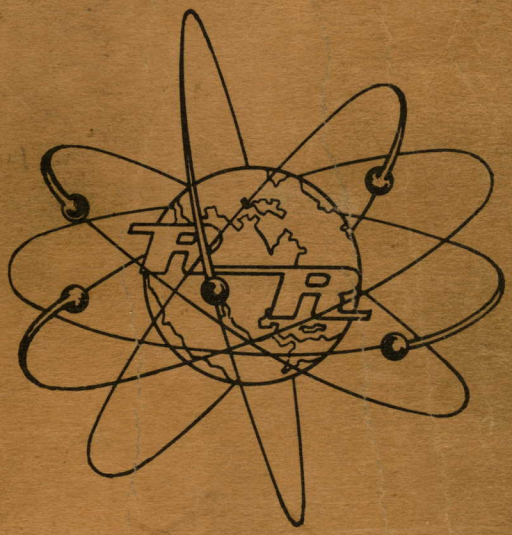
ELECTRONIC COMPUTOR
UNIVAC 60 & 120

Service Manual 21



Remington Rand

DIVISION OF SPERRY RAND CORPORATION

315 FOURTH AVENUE

NEW YORK, N. Y.

GMS - 1011 TM

ELECTRONIC COMPUTER
UNIVAC 60 & 120

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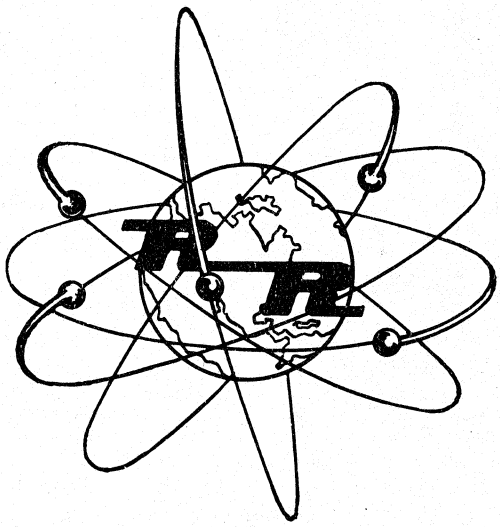

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F O R E W O R D

The material contained in this Manual describes the Mechanical and Electronic functions of the Electronic Computers, Univac 60 & 120.

The description of the machine has been divided into sections covering; Specifications, Mechanical Description, Circuit Description, Adjustments and Preventive Maintenance.

The plate drawings associated with each section will be found immediately following the section to which they pertain. A code letter suffix has been included with the plate drawing number to indicate its associated section. When reference is made to a plate number, unless otherwise indicated by a suffix letter, that reference is made to the plate number associated with the section therein.

ELECTRONIC COMPUTER

UNIVAC 60 & 120

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Printed in U. S. A.

ELECTRONIC COMPUTER

UNIVAC 60 & 120

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MECHANICAL SERVICE
COMMENTARY LETTER
MSC-285

June 24, 1957

UNIVAC 60 & 120 ELECTRONIC COMPUTER
CRANK UP MOTOR WIRING CHANGE FOR CONSTANT
VOLTAGE TRANSFORMER (C.V.T.) INSTALLATIONS

Incorrect operation of the Crank Up Motor has been experienced in some machines where the Sola C.V.T. Regulator has been installed. In these machines, the Crank Up Motor Supply becomes unstable when the B Plus Switch is closed. This causes the Crank Up Motor Control Relay to occasionally drop out.

To correct this condition, the Crank Up Motor Supply Line has been transferred from the B-2 leg to the A-2 leg. The A-2 leg is more stable than the B-2 leg and shows no variation when the B-Plus Interlock Switch is opened and closed.

The wiring change necessary for transferring the Crank Up Motor Supply Line to the A leg consists of disconnecting the lead marked "F-201 Rear" from the rear terminal of Fuse F-204 and connecting this lead to the rear terminal of Fuse F-202.

Figure 1 illustrates the Calculator Crank Up Schematic showing the wiring change.

Figure 2 illustrates the Fuse Panel location and the actual wiring change.

This change should be incorporated in all Univac 60 & 120 Electronic Computers where a Constant Voltage Transformer has been installed.

TABULATING SERVICES DEPARTMENT

MECHANICAL DESCRIPTION
of the
ELECTRONIC COMPUTER
UNIVAC 60 & 120
(Punch)

SECTION B

Remington Rand
DIVISION OF SPERRY RAND CORPORATION
315 FOURTH AVENUE
NEW YORK, N. Y.

ELECTRONIC COMPUTER
UNIVAC 60 & 120

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BASIC PUNCH OPERATION

Fig. B1

The Punch is divided into four basic sections: Feed, Sensing, Punching, and Receiving and the cards progress through the Punch in that sequence.

Three cycles are required to move the card from the Feed Magazine to the Receiving Magazine:

1. Feed Cycle
2. Sensing Cycle
3. Punching and Eject Cycle

The Feed section is located at the front of the machine and is composed of a Feed Magazine and components necessary to move the card into the Sensing Section. The cards are placed in the Feed Magazine in a pre-arranged sequence. The time at which the card is to be fed from the Feed Magazine is controlled by Base Timing. The normal stopping position of this Punch is between 268° and 275°. The card is moved out of the Feed Magazine by the Picker Knife. This knife pushes against the trailing edge of the card and the leading edge of the card is pushed between a rotating set of rolls called Feed Rolls. The card is then pulled by the Feed Rolls and moves through these rolls into the second section called the Sensing Section. The Picker Knife in the Feed Magazine returns once the Feed Rolls control the card movement.

The card enters the Sensing Section between a set of plates which are referred to as the Sensing Card Chamber. The Sensing Card Chamber contains Intermediate Feed Rolls which keep the card in motion when the card leaves the Feed Rolls. The motion of the card is stopped by a cam operated mechanism referred to as a Card Stop. The Sensing Card Chamber is located between two sets of Pin Boxes. Below the Sensing Card Chamber is the lower Sensing Pin Box which is cam raised and lowered. Above the Sensing Card Chamber is the Upper Sensing Pin Box and Sensing Switch Pin Box which are fixed. At the time the card enters the Sensing Card Chamber the Lower Sensing Pin Box is in an upward movement toward the Sensing Card Chamber. The machine requires one Base Cycle, 360° to move the card from the Feed Magazine into the Sensing Card Chamber against the Card Stop with the Lower Pin Box Pins just shy of contacting the card.

The second cycle of the base allows the Lower Sensing Pin Box to sense the Card located in the Sensing Card Chamber. The lower Sensing Pin Box contains a pin for each possible hole in the card, 540, and wherever a hole is present in the card, the pin proceeds on through the hole. Where no hole is present, the pin is depressed. The Lower Sensing.Pin Box continues to rise and the selected pins contact pins in the Upper Sensing Pin Box. The contacted pins in the Upper Sensing Pin Box are elevated sufficiently to be locked in this elevated position. The Lower Sensing Pin Box having reached its up limit starts down.

The elevated Upper Sensing Pins contact pins in the Sensing Switch Pin Box and the movement of the Sensing Switch Pins close switches which can be used in an electrical circuit. The information punched in the card is now retained in the Upper Sensing Pin Box and Sensing Switch Pin Box.

The Lower Sensing Pin Box having sensed the card returns to its low limit. After the pins in the Lower Sensing Pin Box have receded below the card, the Card Stop is opened. The Intermediate Feed Rolls move the card into another set of Feed Rolls.

These rolls move the card out of the Sensing Card Chamber to allow the next card to enter. The card is moved by the Feed Rolls into the Punching Chamber which is located in the Punching Section. The card reaches the Card Stop and its motion is stopped at the end of the second Base Cycle.

The third Base Cycle is the Punching Operation at which time information is punched into the card.

The card is now in the Punching Chamber directly below the Die Section. The Die Section contains the 540 punches required to punch the holes in the card. Above the Die Section is another form of Pin Box called the Set Bar Section. The pins in the Set Bar Section push the Punches through the card when the Set Bar Section is lowered. Above the Set Bar Section is the Tower. The information in the Tower is set up in the Set Bar Section.

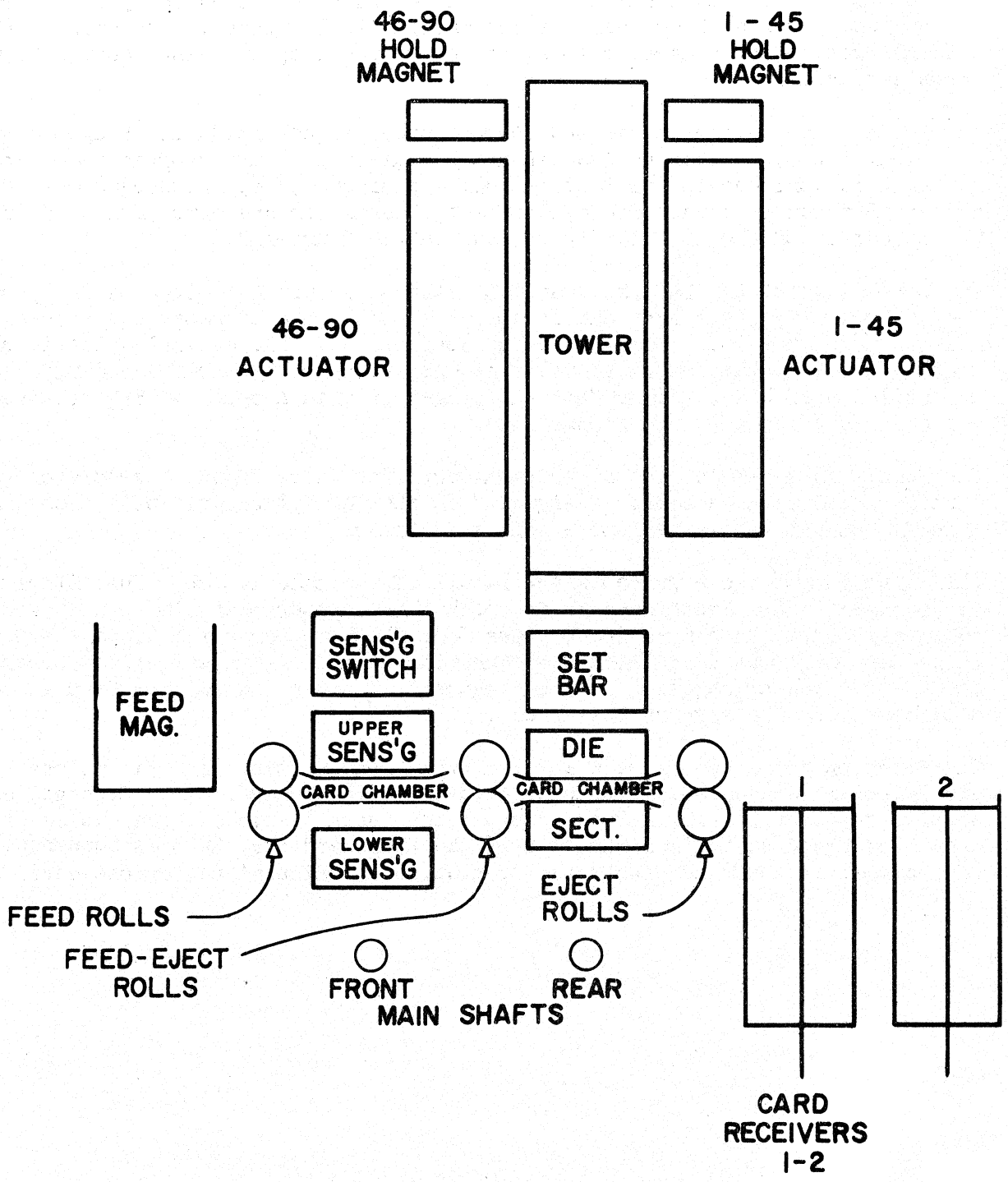
The Tower receives its information from an external source which energizes Actuators. The energized Actuators limit a Rocker Arm to condition a Rod within the Tower in a Set Up Operation.

The third Base Cycle starts with the card resting against the Card Stops in the Punching Chamber. The Set Bar Section moves up to read the set up in the Tower. The Tower set up locks down pins in the Set Bar Section before the Set Bar Section moves down to perform the Punching Operation. The locked down pins in the Set Bar Section contact the Punches in the Die Section and the downward motion of this Set Bar Section forces the contacted Punches through the card.

The Set Bar Section reaches its down limit and returns upward. The Punches are stripped from the card, the Card Stops open and the card is moved by action of the Intermediate Feed Rolls.

The Intermediate Feed Rolls move the card into another set of rolls called Eject Rolls. The Eject Rolls move the card onto the Receiver Bed where the card is deposited into a Receiving Magazine at the end of the third Base Cycle.

PUNCH BASIC BLOCK DIAGRAM
FIG. B-1



BASIC COMPUTER OPERATION

Fig. B2

The start of calculation originates in the Punch. The Start Cam in the Punch closes, and if a card is present in the Sensing Section, a signal is sent to Step Control in the Computer to start calculation. The Computer has a capacity of 40 Program Steps. Each Program Step performs one mathematical process. The signal from Step Control goes to the Plugboard to start the proper step and also causes the Computer to be zeroized.

The proper step is chosen and the Step Sequence signal reads the Plugboard to determine what factors are to be used in the calculation. Each Program Step performs a mathematical process on two factors called Minidend (M'd) and Subvisor (S'r). The M'd and S'r can be a Card Field, Constant, Storage or any combination of the three. The selection of the M'd and S'r is made on the Plugboard.

The completion of the Zeroize Operation starts the Control Circuits in operation. The Control Circuits select one factor at a time. The selected factor has its decimal and 90 Column Code numerical value conditioned. The decimal value is used to control shifts. The numerical value is entered into the Input Decoder. The Process controlled Sign Bias, Add or Subtract, together with a cycle of RIG will register the decoded value into the Accumulator.

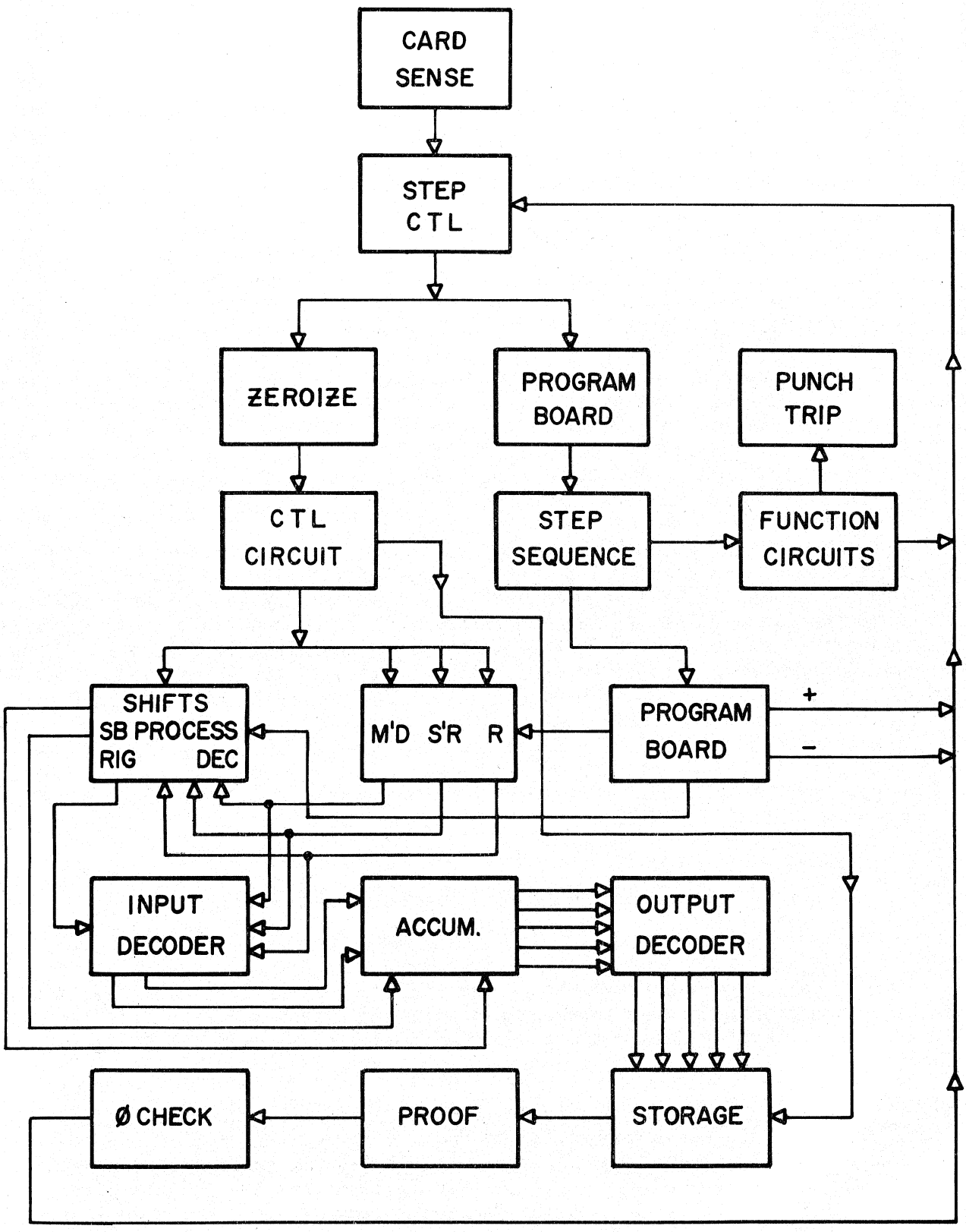
The Result is developed in the Accumulator. The value in the Accumulator is decoded through the Output Decoder. A signal from the Control Circuit will then place the decoded Accumulator Value into a selected Storage.

The value in Storage represents the result of the calculation. This Storage value is now used in the Proof Process to check the Computer operation. A correct calculation results in a Zero Check. The Zero Check releases the signal to Step Control to proceed into the next Program or Function step. The answer of a Program Step may be positive or negative so the Plugboard controls the Program Step selection depending upon the sign of the answer.

The Function Steps can be used in lieu of a Program Step. Function Steps can operate Selector Relays, energize Tower Actuators via Storage, Clear Storage, enable sorting to occur on a Card Feed or cause the Punch to cycle. The choice of which operation is to occur is controlled by the Plugboard via the Step Sequence. The Trip signal to the Punch indicates completion of calculation for one card.

COMPUTER BASIC BLOCK DIAGRAM

FIG. B-2



MOTOR DRIVE AND ELECTROMECHANICAL CLUTCH

Plate 4B

The source of all mechanical power is the Motor A-95. The Motor A-95 is a 230 volt, 1/3 H. P. constant speed motor which is mounted to a Cradle. The Cradle Extension and a bracket mounted on the side frame, together with a pin, form a hinge by which the Motor A-95 is fastened to the machine.

A clearance hole in the bracket permits the Adjusting Screw A-96, together with its Lock Nuts, to provide a sufficient drive belt tension. The Motor A-95 is controlled by the Motor Switch on the Operators Panel. The Motor Pulley and Flywheel A-97 are mounted on the Motor Shaft and control the machine speed.

The "V" Belt A-98 conveys the Motor Shaft rotation to the Clutch Pulley A-99. The Clutch Pulley A-99 is free floating on the Clutch Shaft A-102 which is coupled to the Line Shaft A-100. The Clutch Armature Disc A-101 is driven by the Clutch Pulley A-99 by means of the Spline A-103. The Clutch Coil A-104 is fixed to the frame but the Clutch Field Plate A-105 is keyed to the Clutch Shaft A-102. The Clutch Coil A-104 is energized by a 70 volt supply. The energized Clutch Coil A-104 creates a magnetic field in the Clutch Field Plate A-105 which causes the Clutch Armature Disc A-101 to adhere to the Clutch Field Plate A-105. The rotation of the Clutch Armature Disc A-101 will now cause the Clutch Field Plate A-105 to also rotate. The Clutch Field Plate A-105, being keyed to the Clutch Shaft A-102, causes the Clutch Shaft A-102 and Coupled Line Shaft A-100 to rotate. The control of the 70 volt supply to the Clutch Coil A-104 is shown on Plate 54C.

The rotation of the Clutch Shaft A-102 and Coupled Line Shaft A-100 is stopped by the operation of the Brake. The Brake is applied whenever the Clutch Coil A-104 is de-energized. The Brake Armature Disc A-109 is driven by the Spline A-108 which is keyed to the Clutch Shaft A-102. The Brake Coil A-106 and Brake Field Plate A-107 are fixed to the frame. The Brake Coil A-106 is energized by a 70 volt supply. The energized Brake Coil A-106 creates a magnetic field in the Brake Field Plate A-107 which causes the Brake Armature Disc A-109 to adhere to the Brake Field Plate A-107. The fact that the Brake Field Plate A-107 is fixed will stop the rotation of the Brake Armature Disc A-109. The Brake Armature Disc A-109, being keyed to the Clutch Shaft A-102, will stop rotation of this shaft and the Coupled Line Shaft A-100, causing the Punch to stop. The control of the 70 volt supply to the Brake Coil A-106 is shown on Plate 54C.

CARD FEED AND CARD CONVEYOR MECHANISM

Plate 5B

The Card Feed and Card Conveyor Mechanism consists of the Feed Magazine, Front Feed Rolls, Sensing Card Chamber Intermediate Feed and Pressure Rolls, Feed and Eject Rolls, Punching Card Chamber Intermediate Feed and Pressure Rolls, Eject Rolls, and Card Receivers.

The Tabulating Cards are placed in the Feed Magazine A-1. The feeding of the cards from the Feed Magazine is controlled by the cam driven Card Feed Slide A-9. The Card Feed Cam A-2 is located on the Front Main Shaft A-3. Card feeding begins with the rotation of the Card Feed Cam A-2. The Cam Follower Arm A-4 is held against the perifery of the Card Feed Cam A-2 by the Tension Spring A-16. The movement of the Cam

Follower Arm A-4 is conveyed to the Card Feed Shaft A-7 through Link A-5 and Arm A-6. The Card Feed Arm A-8 is attached to the Card Feed Shaft A-7. The motion of the Card Feed Arm A-8 is conveyed to the Card Feed Slide A-9 by the Card Feed Link A-10. The movement of the Card Feed Slide A-9 causes the Picker Knife A-11 to move the bottom card in the Feed Magazine A-1 between the Throat Knife A-13 and Throat Block A-12. The Picker Knife A-11 on the Card Feed Slide A-9 moves the card between the Front Feed Rolls A-14 and A-15. The Front Feed Rolls A-14 and A-15 grasp the card and the Card Feed Slide A-9 is returned by action of the Card Feed Cam A-2.

The Front Feed Rolls A-14 and A-15 continue the card movement into the Intermediate Feed Rolls A-17 and Pressure Rolls A-18 located in the Sensing Card Chamber. The Intermediate Feed Rolls A-17 and Pressure Rolls A-18 force the card against the closed Sensing Card Chamber Card Stop A-19. The Intermediate Feed Rolls A-17 skid on the bottom surface of the card to hold the card against the Sensing Chamber Card Stop A-19. The sensing of the card takes place at this time.

The Sensing Card Chamber Card Stop A-19 opens after the card has been sensed. The Intermediate Feed Rolls A-17 and Pressure Rolls A-18 move the card into the Feed Eject Rolls A-20 and A-21. The Feed Eject Rolls A-20 and A-21 move the card into the Intermediate Feed Rolls A-22 and Pressure Rolls A-23, located in the Punching Card Chamber. The Intermediate Feed Rolls A-22 and Pressure Rolls A-23 force the card against the closed Punching Chamber Card Stop A-24. The Intermediate Feed Rolls A-22 skid on the bottom surface of the card to hold the card against the Sensing Chamber Card Stop A-24.

The Punching Card Chamber Card Stop A-24 opens after the card has been punched. The Intermediate Feed Rolls A-22 and Pressure Rolls A-23 move the card into the Eject Rolls A-25 and A-26. The Eject Rolls A-25 and A-26 move the card into the Receiver Feed Rolls A-27. The Receiver Feed Rolls A-27 allows the card to drop in the Front Card Receiver A-29 or Rear Card Receiver A-30. The card drops in the Front Card Receiver A-29 when the Front Receiver Shutter Fingers A-28 have been raised.

The cards are stacked in the Card Receiver on the Card Platform A-31. The Card Platform A-31 is mounted on Shaft A-32. Shaft A-32 is supported by the Compression Spring A-33 so that the weight of the cards on the Card Platform A-31 will compress the Compression Spring A-33 allowing the Card Platform A-31 to lower.

CARD SENSING MECHANISM

Plates 6B, 7B, 8B

The Card Sensing Mechanism consists of the Lower Sensing Pin Box, Sensing Card Chamber and Card Stop, Upper Sensing Pin Box and Sensing Switch Box.

Plate 6B shows the Lower Sensing Pin Box A-34 at its low limit. At this time, the Sensing Card Chamber Card Stop A-19 is open to enable a card to be released into the Feed Eject Rolls A-25 and A-26. A second card is just entering the Sensing Card Chamber. The second card continues into the Sensing Card Chamber as the Sensing Card Chamber Card Stop A-19 closes. The Card Stop Cam A-45 causes the Card Stop Mechanism A-46 to close the Sensing Card Chamber Card Stop A-19. The second card, upon reaching the Sensing Chamber Card Stop A-19, has its forward motion stopped with the Intermediate Feed Rolls A-17 skidding on the bottom surface of the card.

The Lower Sensing Pin Box A-34 is now in its upward motion. The roll on the Pin Lock Mechanism A-38 is on the high part of the Dummy Cam A-37. This position of the Pin Lock Mechanism A-38 causes the Lock Slide A-36 to be held in a retracted position so that the extrusion on the Selecting Pins A-35 are in the open portion of the Locking Window of the Lock Slide A-36.

The Lower Sensing Pin Box A-34 in continuing to rise enables the Selecting Pins A-35 to contact the card which is held in the Sensing Card Chamber as shown on Plate 7B. From this point a Selecting Pin A-35 will either penetrate a hole in the card or be depressed where no hole exists due to the rising of the Lower Sensing Pin Box A-34. The No Card Sensing Plunger A-40 also contacts the card and is depressed causing the Pin Lock Control Lever A-41 to release the Pin Lock Mechanism A-38 so that the roll on the Pin Lock Mechanism A-38 can follow the slope of the Dummy Cam A-37. The Pin Lock Torsion Spring A-39 enables the roll on the Pin Lock Mechanism A-38 to follow the slope of the Dummy Cam A-37. This motion of the Pin Lock Mechanism A-38 moves the Lock Slide A-36 so that the extrusion on the Selecting Pins A-35 contacting the card will be depressed below the Latch in the Lock Slide A-36. The Selecting Pins A-35 which penetrate a hole in the card will have their extrusion above the Latch on the Lock Slide A-36. Just prior to the latched Selecting Pins A-35 contacting the Set Up Pins A-43 the selection in the Upper Sensing Pin Box A-42 is retracted.

The Retract Cam A-49 operates the Retract Mechanism A-50 so that the Retract Bail A-48 retracts the Lock Slides A-44. The Lock Slides A-44, during retraction, are positioned so that the extrsuions on the Set Up Pins A-43 are free of the Latch in the Lock Slide A-44. The Compression Spring on each Set Up Pin A-43 will force these pins down so that the shoulder on the Set Pin A-43 will limit against the Cell Plate A-52.

The selected pins in the ascending Lower Sensing Pin Box A-34 contact corresponding Set Up Pins A-43 in the Upper Sensing Pin Box A-42. The contacted Set Up Pins A-43 will be raised until the Lower Sensing Pin Box A-34 reaches its up limit. The selected Set Up Pins A-43 will now be retained by removal of the retraction on the Lock Slides A-44. The Retract Cam A-49 operates the Retract Mechanism A-50 so that the Retract Bail A-48 is positioned to enable the Lock Slides A-44 to move into a locking position. The tension of the Comb Spring A-51 moves the Lock Slide A-44 so the Latch will be positioned under the extrusion of the selected Set Up Pins A-43. The extrusion on the unselected Set Up Pins A-43 will be below the Latch on the Lock Slides A-44.

Plate 8B shows the selected Set Up Pins A-43 contacting and operating pins in the Sensing Switch Box A-86. A selected Set Up Pin A-43 contacts the Intermediate Sensing Pin A-87. The motion of the Intermediate Sensing Pin A-87 is transferred through

the Compression Spring A-88 and Pin Cap A-89 to raise the Contact Pin A-90. The raised Contact Pin A-90 compresses the Contact Pin Spring A-91 and operates the Contact A-92. Contact A-92 is moved to touch Contact A-93. Any additional motion is absorbed by the Compression Spring A-88. The selection in the Sensing Switch Box A-86 is entirely controlled by the Upper Sensing Pin Box A-42. The contacts A-92 and A-93 connect to a Removable Connector A-94, to complete the electrical circuits used in reading the sensed values in a card. The uses of the electrical circuit are explained in Section C.

The Lower Sensing Pin Box A-34 descends to its low limit with the information from the card retained in the Upper Sensing Pin Box A-42. The card is released from the Sensing Card Chamber when the Sensing Chamber Card Stop A-19 opens.

CARD PUNCHING MECHANISM

Plates 9B, 10B, 11B

The Card Punching Mechanism consists of the Tower, Set Bar Section, Punching Card Chamber and Card Stop and Die Section.

Plate 9B shows the Punching Mechanism at the position when information to be punched is impulsed to the Actuators A-53.

There is an Actuator A-53 for each hole position of the card. Only those Actuators A-53 which represent hole positions to be punched will be impulsed. An impulsed Actuator A-53 operates the Actuator Armature A-54. The movement of the Actuator Armature A-54 releases the Interposer Assembly A-55. The Spring tension on the Interposer Assembly A-55 causes the Assembly to limit against Screw A-56. The released Interposer Assembly A-55 is now positioned in the path of the Rocker Arm A-57.

The Set Bar Section A-59 and the Tower Rod Assembly A-60 are jointly raised as shown on plate 10B. Each Tower Rod A-58 contacts a Rocker Arm A-57. The upward movement of the Tower Rod A-58 causes the Rocker Arm A-57 to pivot. The extent of motion of each Rocker Arm A-57 is governed by the position of an associated Interposer Assembly A-55. All released Interposer Assemblies A-55 will limit the motion of the Rocker Arm A-57. The Rocker Arms A-57 which have restricted motion due to a released Interposer Assembly A-55 will cause depression of its respective Tower Rod A-58 as the Set Bar Section A-59 and Tower Rod Assembly A-60 are raised.

As the Set Bar Section A-59 is raised the Retract Cam A-61 raises the Cam Follower Arm A-62 and through Links A-63 and A-64 causes the Retract Shaft A-65 to rock. The motion of the Retract Shaft A-65 forces the Retract Bail A-67 against the Lock Slides A-68. The Lock Slides A-68 are moved so that the extrusions on the Set Bar Pins A-69 are in the open portion of the window in the Lock Slide A-68. Any Set Bar Pins A-69 which had been in a latched position will be released. A Tower Rod A-58 whose upward movement was restricted will contact a Set Bar Pin A-69 causing the Set Bar Pin A-69 to be depressed. The Set Bar Section A-59 reaches its up limit and all contacted Set Bar Pins A-69 will be depressed so their extrusion is below the Latch on the Lock Slides A-68.

The Retract Cam A-61 lowers the Cam Follower Arm A-62 and through Links A-63 and A-64 causes the Retract Shaft A-65 to normalize. The Retract Shaft A-65 normalizing allows the Lock Slides A-68 to be returned by the tension of the Comb Spring A-70. The extrusions on the depressed Set Bar Pins A-69 will now be under the Latch on the Lock Slides A-68. The Set Bar Section A-59 and Tower Rod Assembly A-60 are now lowered to perform the Punching Operation as shown on plate 11B. As the Set Bar Section A-59 is lowered, the depressed Set Bar Pins A-69 contact their corresponding Punches A-75. The card to be punched is located below the Punches A-75 in the Punching Card Chamber. The Card is being held against the Card Stop A-24 by the skidding action of the Intermediate Feed Rolls A-22 on the Lower surface of the card. The descending Set Bar Section A-59 forces the contacted Punches A-75 through the card into the dies A-78. The Set Bar Section A-59 reaches its lower limit at which time all contacted Punches A-75 have penetrated the card.

Retraction of the Interposer Assemblies A-55 occurs while the punching of the card occurs. The Tower Retract Cam A-71 operates the Retract Mechanism A-72. The Retract Mechanism A-72 rocks the Retract Bail A-73. The movement of the Retract Bail A-73 causes the Interposer Assembly Restore Links A-74 to be raised. The studs on the Interposer Assembly Restore Links A-74 return the released Interposer Assemblies A-55

to a latched position on the Interposer Armature A-54.

The Set Bar Section A-59 rises and the Stripper Plate A-77 also rises to strip the Punches A-75 from the card. The Card Stop A-24 opens to release the card from the Punching Card Chamber.

RESET SOLENOID FUNCTION

Plate 11B

An additional feature of the Punch Unit is the Reproduce Operation. Reproduce is employed to transfer information from one Card Field to another in the same card or to duplicate the information from the first card into the following card or cards. Where information is to be duplicated into following cards, a mechanism is used to prevent resetting the Interposer Assemblies in the columns being punched by Reproduce. This mechanism is the Non-Restore Actuator A-79. The Non-Restore Actuator A-79 is impulsed from the card containing the information to be reproduced. The released Interposer Assembly A-55 of the Non-Restore Actuator A-79 prevents the Interposer Assembly Restore Link A-74 retract operation. The upward movement of the Interposer Assembly Restore Link A-74 is limited by the Interposer Assembly A-55 of the Non-Restore Actuator A-79. The Yield Spring A-81 absorbs the motion from the Retract Bail A-73. There is a Non-Restore Actuator A-79 for each of the 80 columns.

The Reproduce information is cleared by the Reset Solenoid A-80 operation. Whenever the Reset Solenoid A-80 is energized the Reset Bail A-82 is rocked. The motion of the Reset Bail A-82 restores the Interposer Assembly A-55 of the Non-Restore Actuator A-79 to a latched position on the Non-Restore Actuator Armature A-54. The Interposer Assembly Restore Link A-74 will now reset all Interposer Assemblies A-55.

NON-RESET SOLENOID FUNCTION

Plate 11B

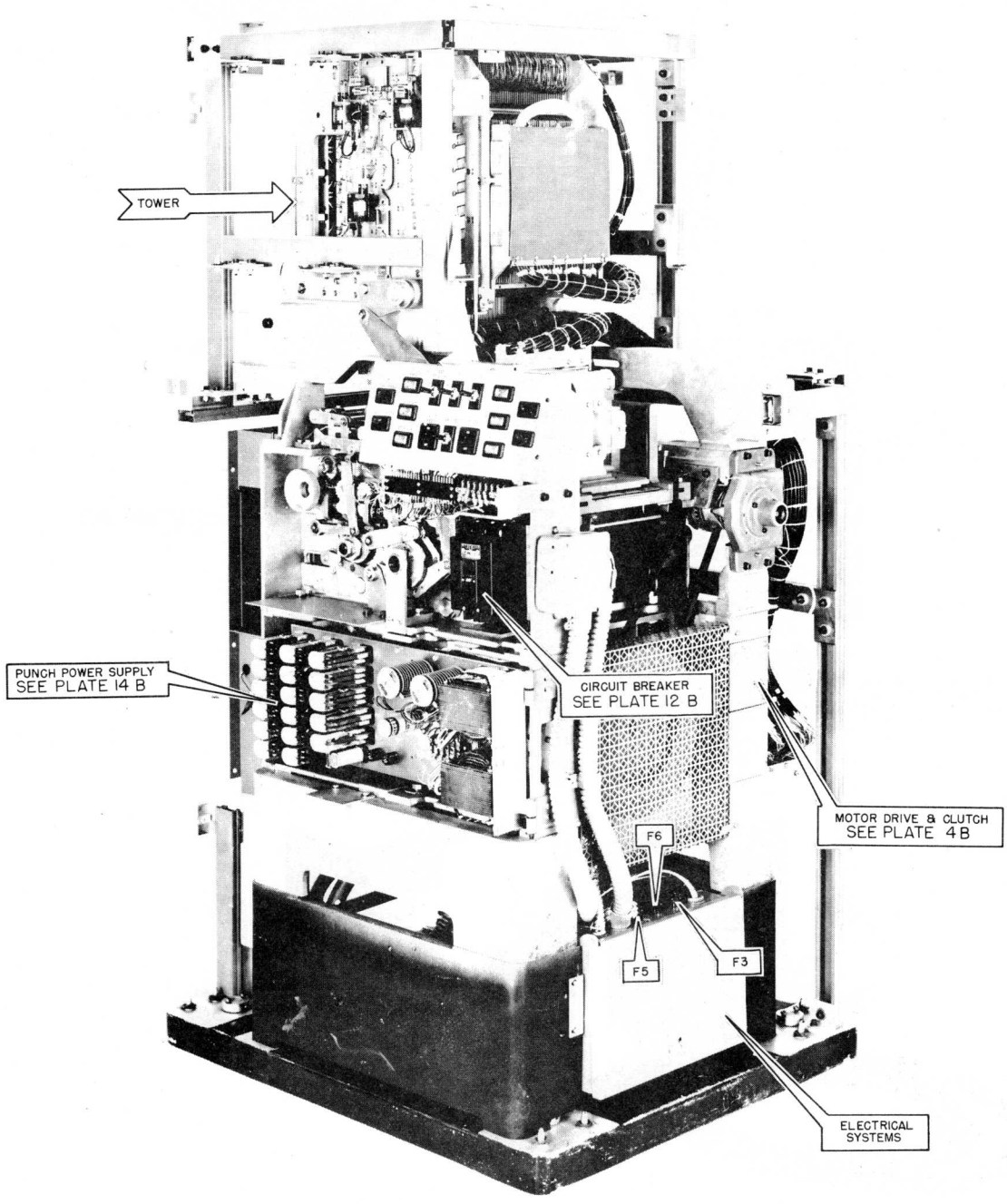
The resetting of all Interposer Assemblies A-55 is defeated by operation of the Non-Reset Solenoid A-83. The circuit to energize the Non-Reset Solenoid A-83 is energized when the Tower Retract Mechanism A-72 is on the low part of the Tower Retract Cam A-71. The plunger movement of the energized Non-Reset Solenoid A-83 disengages the Tower Retract Latch A-84 from the Tower Retract Mechanism A-72. The movement of the Tower Retract Mechanism A-72 caused by the Tower Retract Cam A-71 is not projected to the Tower Retract Bail A-73. The Interposer Assembly Restore Links A-74 will not be raised so any Interposer Assemblies A-55 which were released will remain in this position. The de-energizing of the Non-Reset Solenoid A-83 will enable the Tower Retract Latch A-84 to again engage the Tower Retract Mechanism A-72 for normal Tower retraction on the next machine cycle.

SKIP

Plate 10B

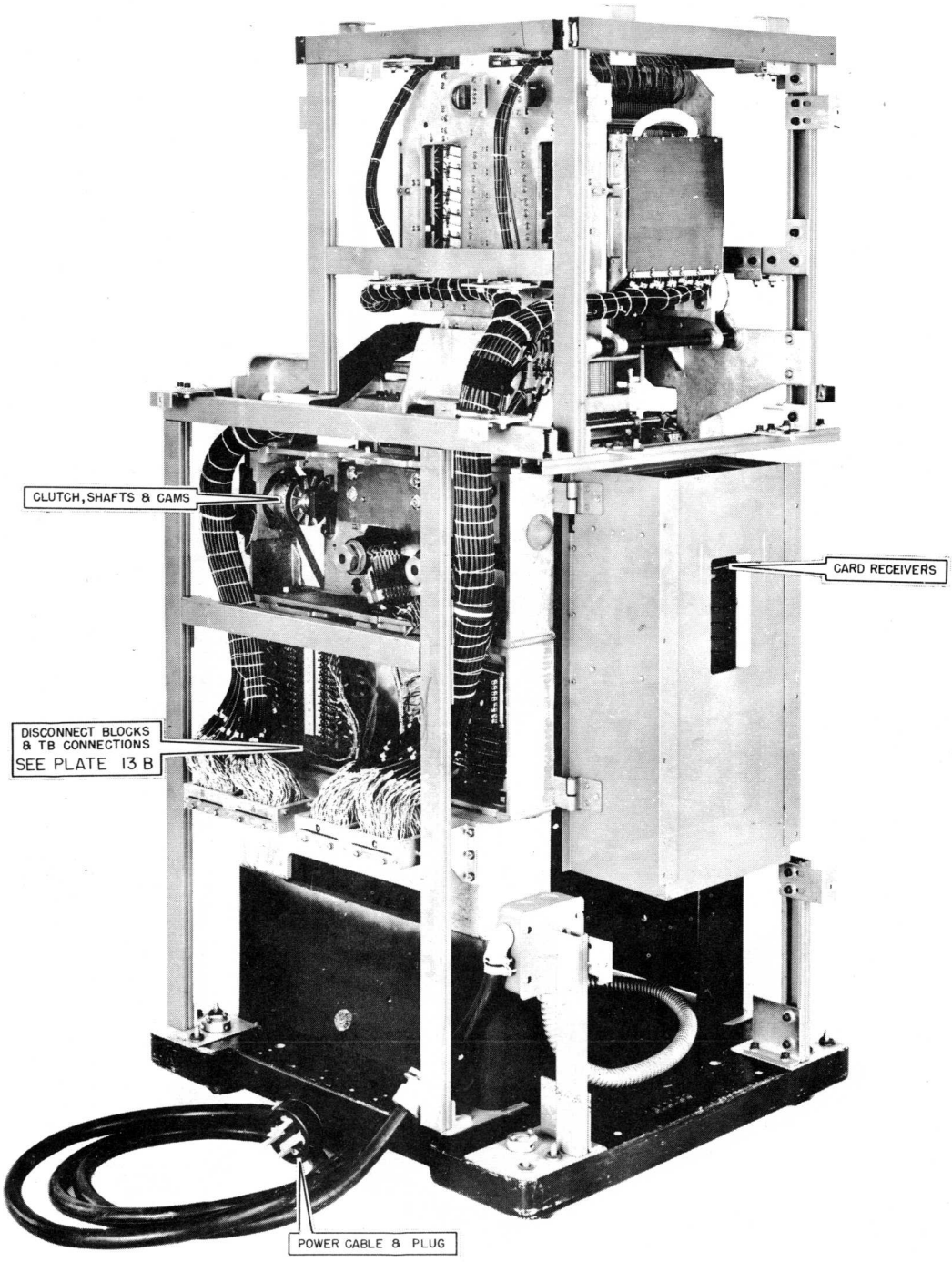
Card punching is defeated by operation of the Skip Solenoid A-111. The circuit to en-

ergize the Skip Solenoid A-111 is shown in Plate 55C. The Skip Solenoid A-111 is energized when the Cam Follower Arm A-62 is on the high part of the Set Bar Retract Cam A-61. The plunger movement of the Skip Solenoid A-111 pulls the Link A-112 and Skip Interposer A-113 under the Stud A-114. At this time, the Set Bar Retract Shaft A-65 is rocked holding the Lock Slides A-68 in a retracted position. The Cam Follower Arm A-62 cannot follow the perifery of the Set Bar Retract Cam A-61 since Link A-63 and Link A-64 are being retained in a retract condition by action of the Skip Interposer A-113 on the Stud A-114. The Set Bar Section A-59 is held retracted during the punching operation so no set up is maintained in the Set Bar Pins A-69. The Skip Interposer A-113 is held under the Stud A-114 until the Cam Follower Arm A-62 again is on the high part of the Set Bar Retract Cam A-61. At this time, the action of Spring A-115 restores the Skip Solenoid Plunger Link A-112 and the Skip Interposer A-113 to its normal position.



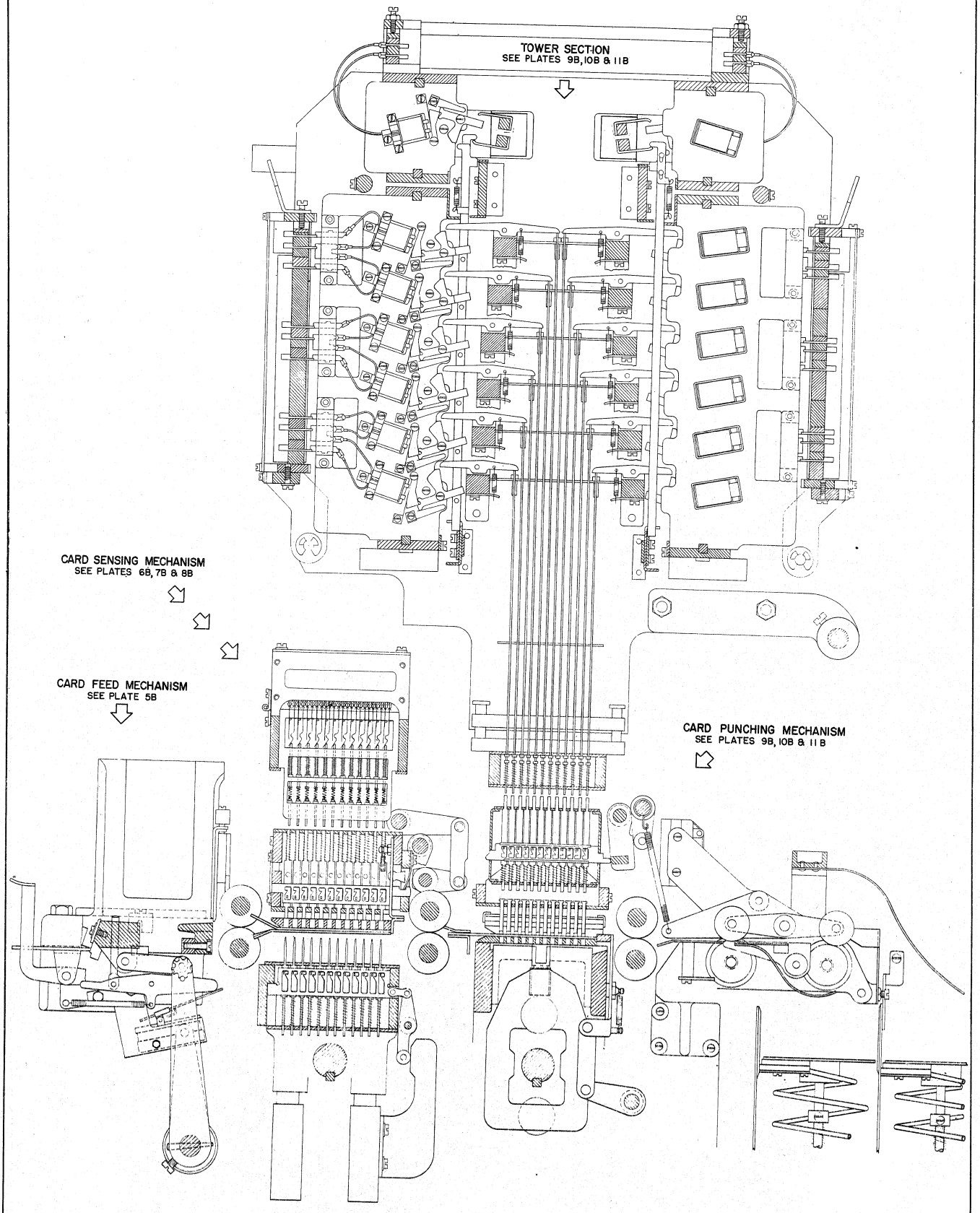
PUNCH - FRONT VIEW

PLATE 1 B



PUNCH - REAR VIEW

PLATE 2B

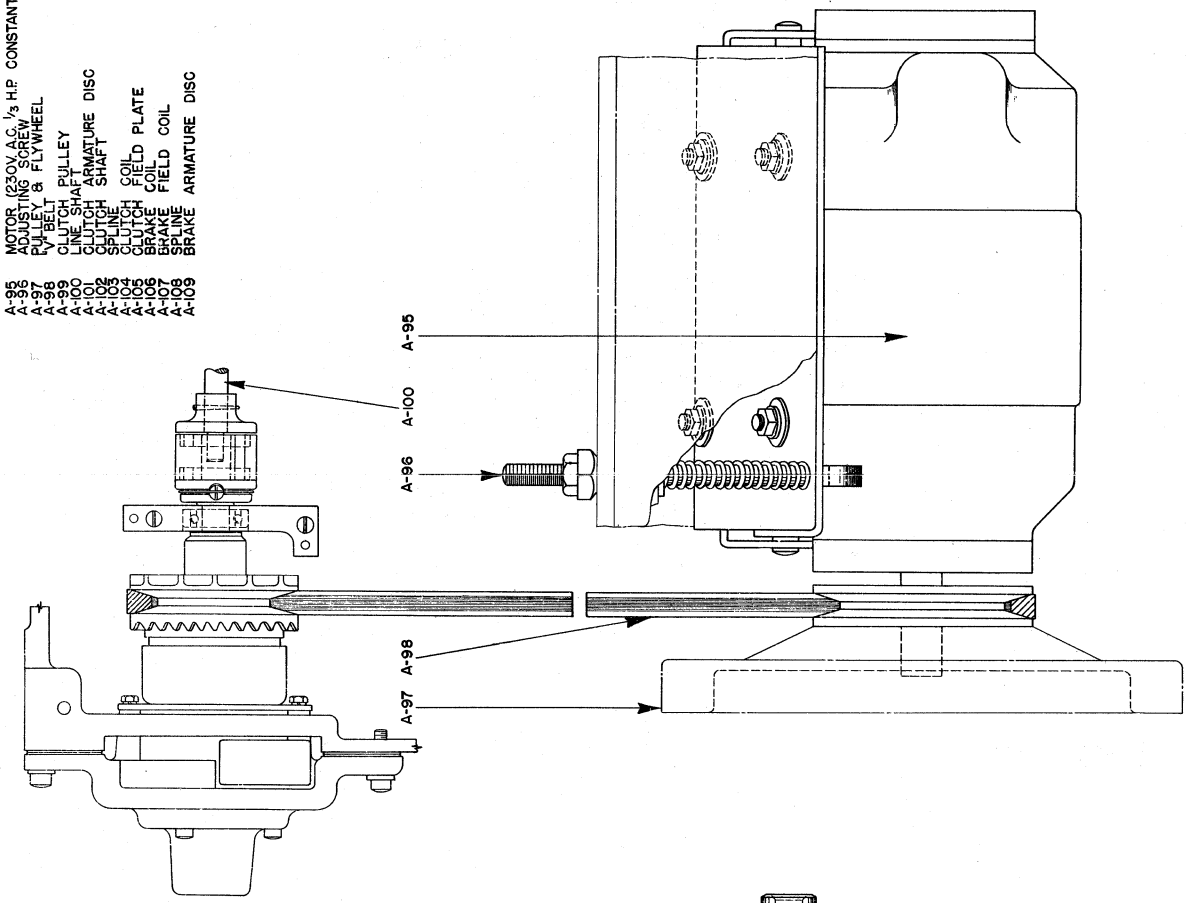


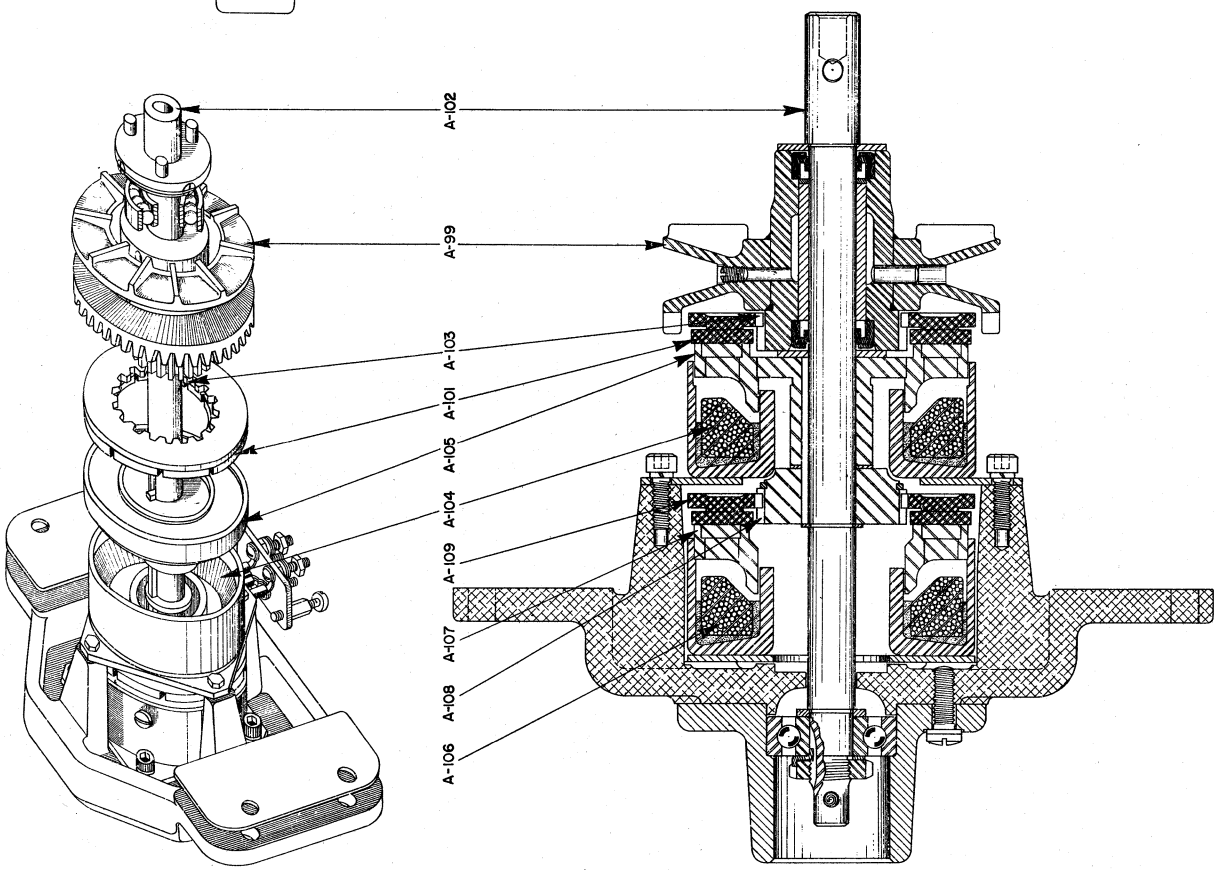
PUNCH CROSS SECTIONAL VIEW.

PLATE 3B

PARTS NOMENCLATURE

A-95	MOTOR (230V A.C. 1/3 H.P. CONSTANT SPEED)
A-96	ADJUSTING SCREW
A-97	PULLEY & FLYWHEEL
A-98	V-BELT
A-99	CLUTCH PULLEY
A-100	LINE SHAFT
A-101	CLUTCH ARMATURE DISC
A-102	CLUTCH SHAFT
A-103	SPLINE
A-104	CLUTCH FIELD PLATE
A-105	CLUTCH COIL
A-106	BRAKE COIL
A-107	BRAKE FIELD COIL
A-108	SPLINE
A-109	BRAKE ARMATURE DISC



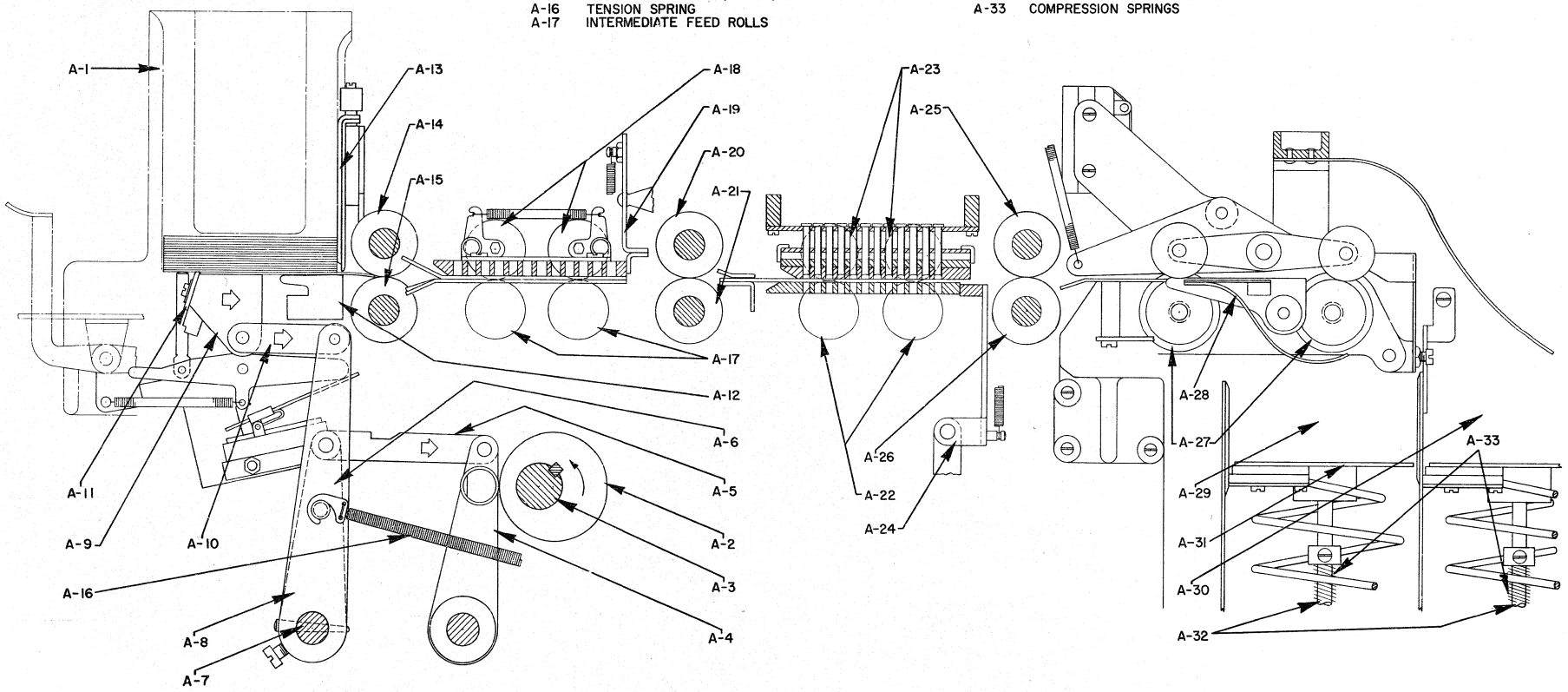


MOTOR DRIVE & CLUTCH

PLATE 4B

PARTS NOMENCLATURE

A-1	FEED MAGAZINE
A-2	CARD FEED CAM
A-3	FRONT MAIN SHAFT
A-4	CAM FOLLOWER ARM
A-5	LINK
A-6	ARM
A-7	CARD FEED SHAFT
A-8	CARD FEED ARM
A-9	CARD FEED SLIDE
A-10	CARD FEED LINK
A-11	PICKER KNIFE
A-12	THROAT BLOCK
A-13	THROAT KNIFE
A-14	FRONT FEED ROLL (UPPER)
A-15	FRONT FEED ROLL (LOWER)
A-16	TENSION SPRING
A-17	INTERMEDIATE FEED ROLLS
A-18	INTERMEDIATE PRESSURE ROLLS
A-19	SENSING CHAMBER CARD STOP
A-20	FEED EJECT ROLL (UPPER)
A-21	FEED EJECT ROLL (LOWER)
A-22	INTERMEDIATE FEED ROLLS
A-23	INTERMEDIATE PRESSURE ROLLS
A-24	PUNCHING CHAMBER CARD STOP
A-25	EJECT ROLL (UPPER)
A-26	EJECT ROLL (LOWER)
A-27	RECEIVER FEED ROLLS
A-28	FRONT RECEIVER SHUTTER FINGER
A-29	FRONT CARD RECEIVER
A-30	REAR CARD RECEIVER
A-31	CARD PLATFORM
A-32	SHAFT
A-33	COMPRESSION SPRINGS

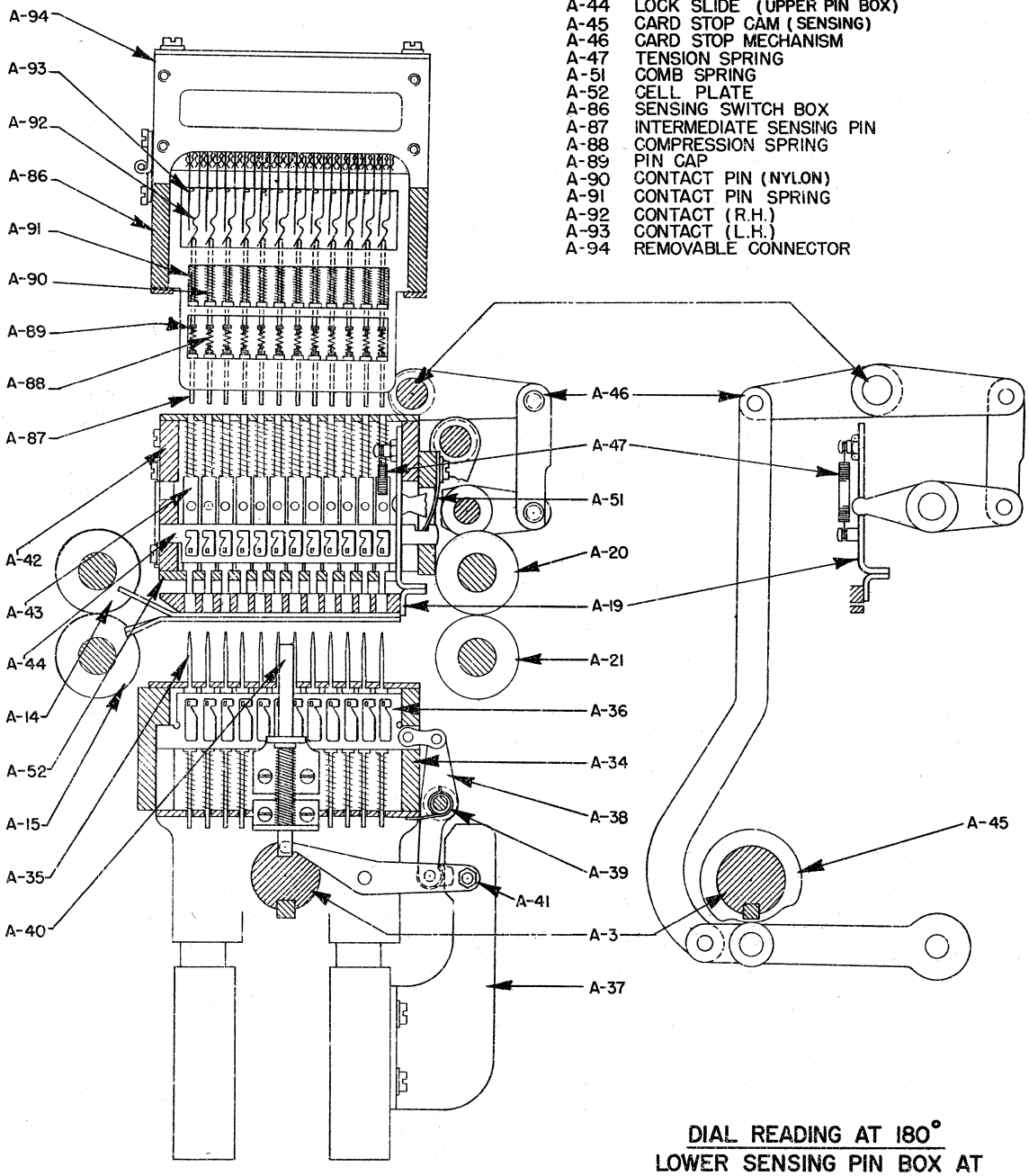


DIAL READING 132°

FEED MAGAZINE IS IN FULL FEED POSITION.

PARTS NOMENCLATURE

A-3	FRONT MAIN SHAFT
A-14	FRONT FEED ROLL (UPPER)
A-15	FRONT FEED ROLL (LOWER)
A-19	SENSING CHAMBER CARD STOP
A-20	FEED EJECT ROLL (UPPER)
A-21	FEED EJECT ROLL (LOWER)
A-34	LOWER SENSING PIN BOX
A-35	SELECTING PIN (LOWER PIN BOX)
A-36	LOCK SLIDE (LOWER PIN BOX)
A-37	DUMMY CAM
A-38	PIN LOCK MECHANISM
A-39	PIN LOCK TORSION SPRING
A-40	NO CARD SENSING PLUNGER
A-41	PIN LOCK CONTROL LEVER
A-42	UPPER SENSING PIN BOX
A-43	SET-UP PIN (UPPER PIN BOX)
A-44	LOCK SLIDE (UPPER PIN BOX)
A-45	CARD STOP CAM (SENSING)
A-46	CARD STOP MECHANISM
A-47	TENSION SPRING
A-51	COMB SPRING
A-52	CELL PLATE
A-86	SENSING SWITCH BOX
A-87	INTERMEDIATE SENSING PIN
A-88	COMPRESSION SPRING
A-89	PIN CAP
A-90	CONTACT PIN (NYLON)
A-91	CONTACT PIN SPRING
A-92	CONTACT (R.H.)
A-93	CONTACT (L.H.)
A-94	REMOVABLE CONNECTOR



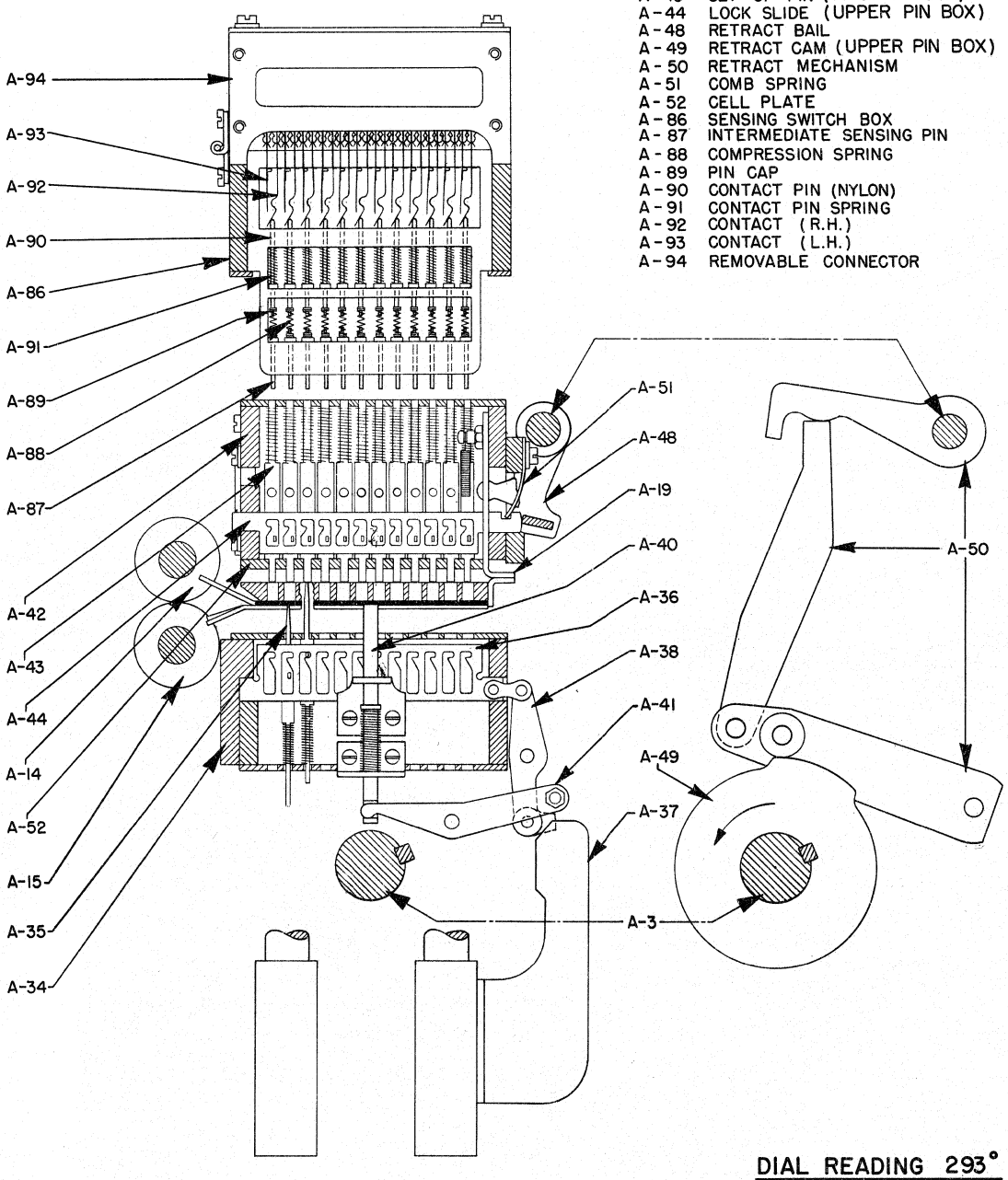
DIAL READING AT 180°
LOWER SENSING PIN BOX AT
ITS LOW LIMIT - NO SELECTION.

SENSING 180°

PLATE 6B

PARTS NOMENCLATURE

A-3	FRONT MAIN SHAFT
A-14	FRONT FEED ROLLS (UPPER)
A-15	FRONT FEED ROLLS (LOWER)
A-19	SENSING CHAMBER CARD STOP
A-34	LOWER SENSING PIN BOX
A-35	SELECTING PIN (LOWER PIN BOX)
A-36	LOCK SLIDE (LOWER PIN BOX)
A-37	DUMMY CAM
A-38	PIN LOCK MECHANISM
A-40	NO CARD SENSING PLUNGER
A-41	PIN LOCK CONTROL LEVER
A-42	UPPER SENSING PIN BOX
A-43	SET-UP PIN (UPPER PIN BOX)
A-44	LOCK SLIDE (UPPER PIN BOX)
A-48	RETRACT BAIL
A-49	RETRACT CAM (UPPER PIN BOX)
A-50	RETRACT MECHANISM
A-51	COMB SPRING
A-52	CELL PLATE
A-86	SENSING SWITCH BOX
A-87	INTERMEDIATE SENSING PIN
A-88	COMPRESSION SPRING
A-89	PIN CAP
A-90	CONTACT PIN (NYLON)
A-91	CONTACT PIN SPRING
A-92	CONTACT (R.H.)
A-93	CONTACT (L.H.)
A-94	REMOVABLE CONNECTOR



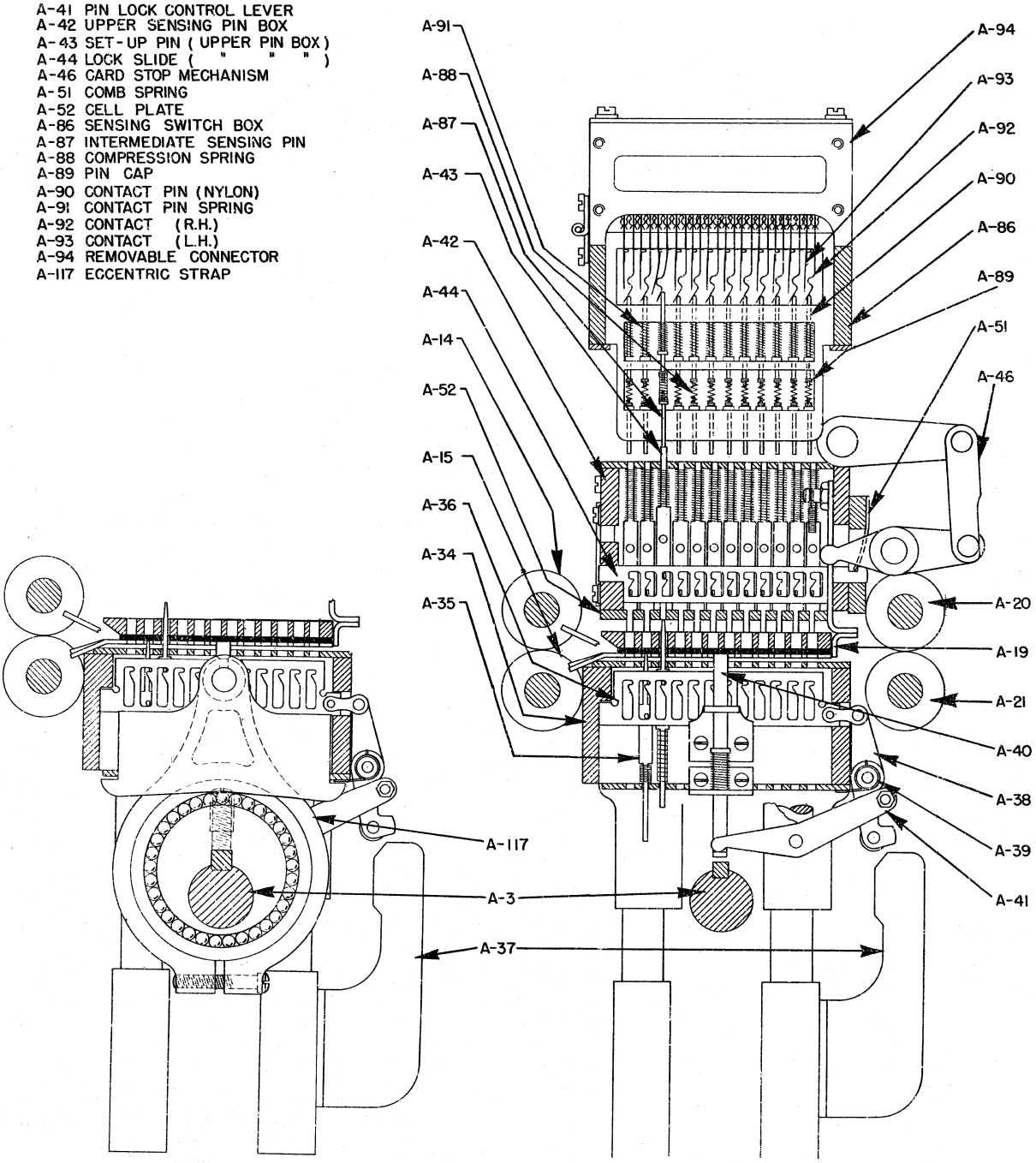
DIAL READING 293°
SELECTING PINS ARE JUST CONTACTING SET-UP PINS.

SENSING 293°

PLATE 7B

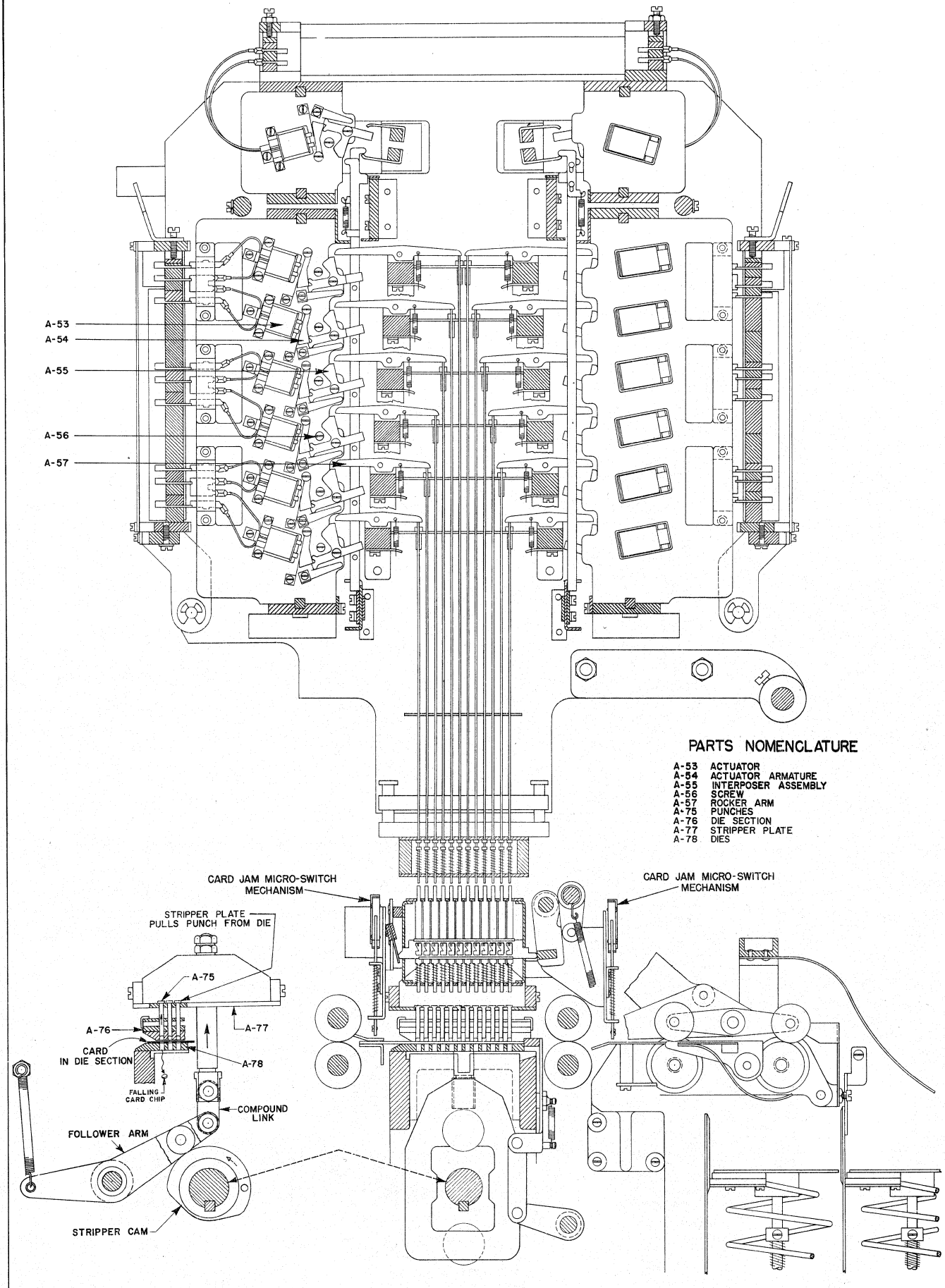
PARTS NOMENCLATURE

A-3 FRONT MAIN SHAFT
A-14 FRONT FEED ROLLS (UPPER)
A-15 FRONT FEED ROLLS (LOWER)
A-19 SENSING CHAMBER CARD STOP
A-20 FEED EJECT ROLL (UPPER)
A-21 FEED EJECT ROLL (LOWER)
A-34 LOWER SENSING PIN BOX
A-35 SELECTING PIN (LOWER PIN BOX)
A-36 LOCK SLIDE (" " ")
A-37 DUMMY CAM
A-38 PIN LOCK MECHANISM
A-39 PIN LOCK TORSION SPRING
A-40 NO CARD SENSING PLUNGER
A-41 PIN LOCK CONTROL LEVER
A-42 UPPER SENSING PIN BOX
A-43 SET-UP PIN (UPPER PIN BOX)
A-44 LOCK SLIDE (" " ")
A-46 CARD STOP MECHANISM
A-51 COMB SPRING
A-52 CELL PLATE
A-86 SENSING SWITCH BOX
A-87 INTERMEDIATE SENSING PIN
A-88 COMPRESSION SPRING
A-89 PIN CAP
A-90 CONTACT PIN (NYLON)
A-91 CONTACT PIN SPRING
A-92 CONTACT (R.H.)
A-93 CONTACT (L.H.)
A-94 REMOVABLE CONNECTOR
A-117 ECCENTRIC STRAP



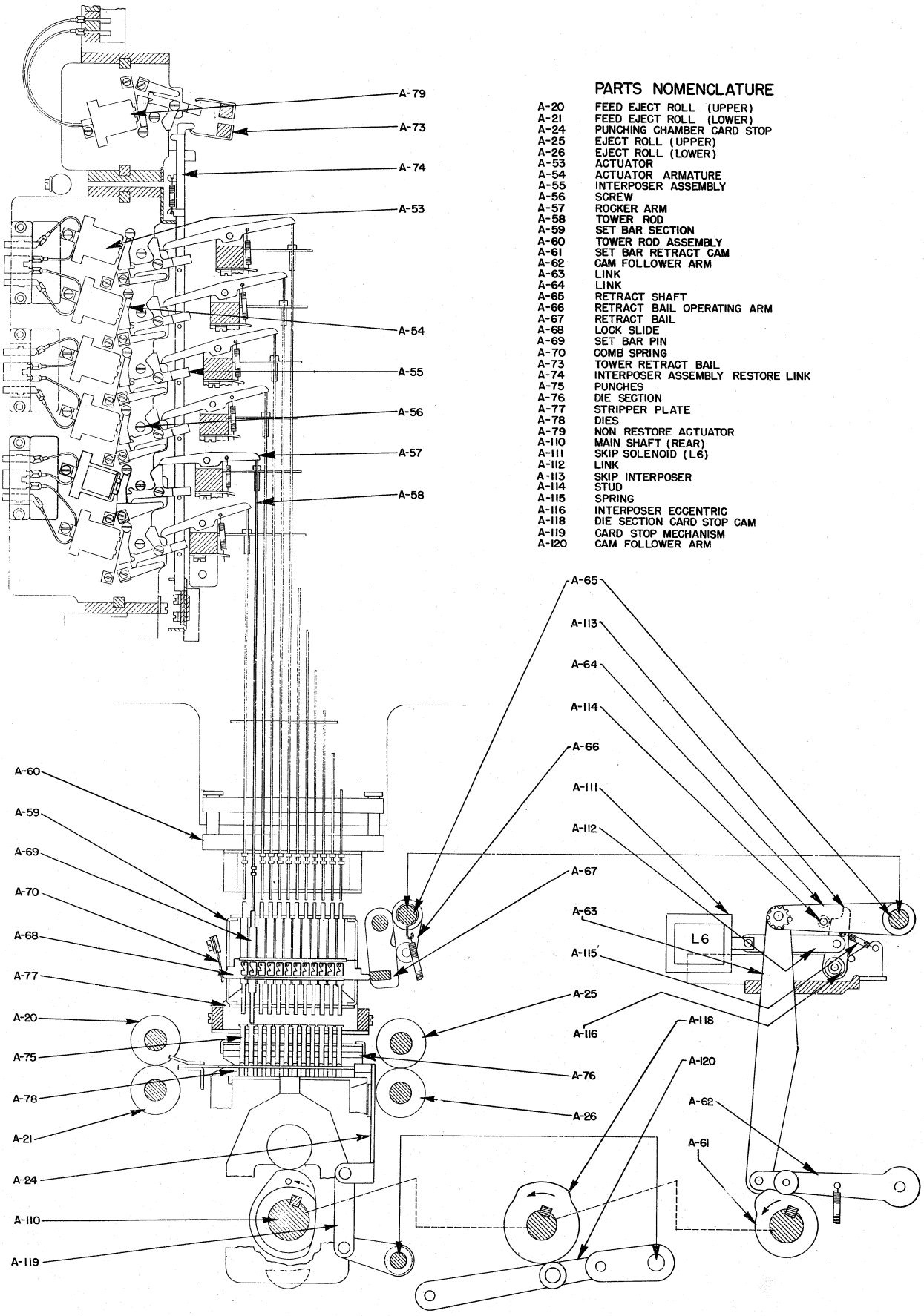
DIAL READING AT 360°
LOWER SENSING PIN BOX AT
ITS UP LIMIT-SELECTION IS
COMPLETED.

SENSING 360°	PLATE 8B



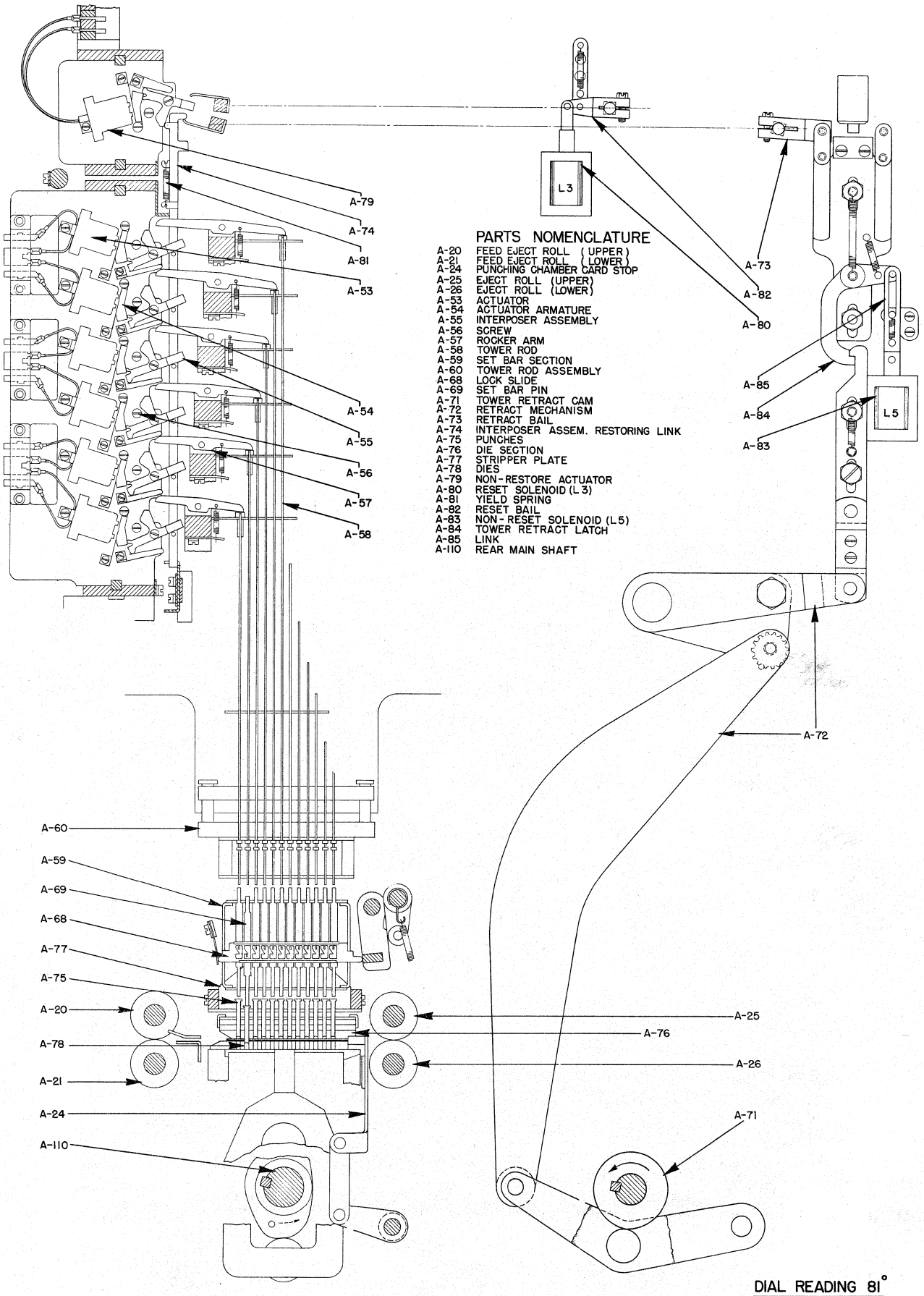
PUNCHING 180°

PLATE 9B



PARTS NOMENCLATURE

A-20	FEED EJECT ROLL (UPPER)
A-21	FEED EJECT ROLL (LOWER)
A-24	PUNCHING CHAMBER CARD STOP
A-25	EJECT ROLL (UPPER)
A-26	EJECT ROLL (LOWER)
A-53	ACTUATOR
A-54	ACTUATOR ARMATURE
A-55	INTERPOSER ASSEMBLY
A-56	SCREW
A-57	ROCKER ARM
A-58	TOWER ROD
A-59	SET BAR SECTION
A-60	TOWER ROD ASSEMBLY
A-61	SET BAR RETRACT CAM
A-62	CAM FOLLOWER ARM
A-63	LINK
A-64	LINK
A-65	RETRACT SHAFT
A-66	RETRACT BAIL OPERATING ARM
A-67	RETRACT BAIL
A-68	LOCK SLIDE
A-69	SET BAR PIN
A-70	COMB SPRING
A-73	TOWER RETRACT BAIL
A-74	INTERPOSER ASSEMBLY RESTORE LINK
A-75	PUNCHES
A-76	DIE SECTION
A-77	STRIPPER PLATE
A-78	DIES
A-79	NON RESTORE ACTUATOR
A-110	MAIN SHAFT (REAR)
A-111	SKIP SOLENOID (L6)
A-112	LINK
A-113	SKIP INTERPOSER
A-114	STUD
A-115	SPRING
A-116	INTERPOSER ECCENTRIC
A-118	DIE SECTION CARD STOP CAM
A-119	CARD STOP MECHANISM
A-120	CAM FOLLOWER ARM



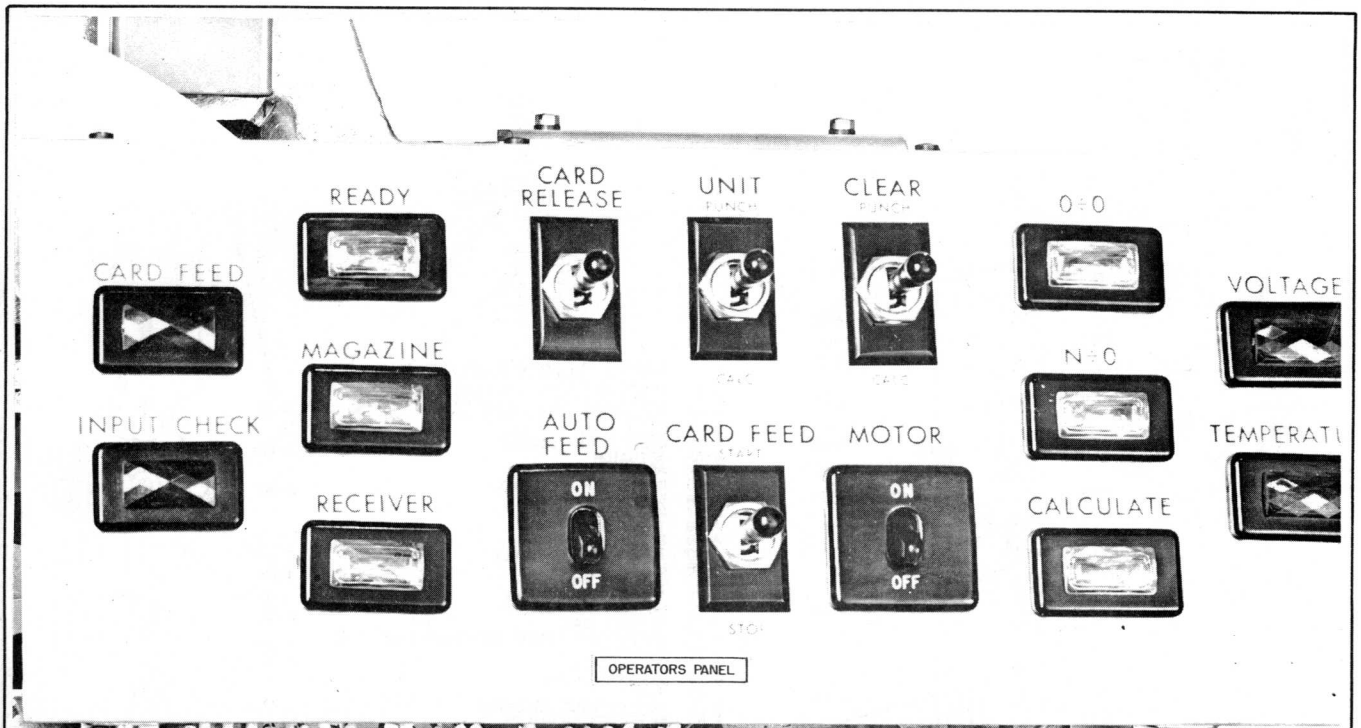
PARTS NOMENCLATURE

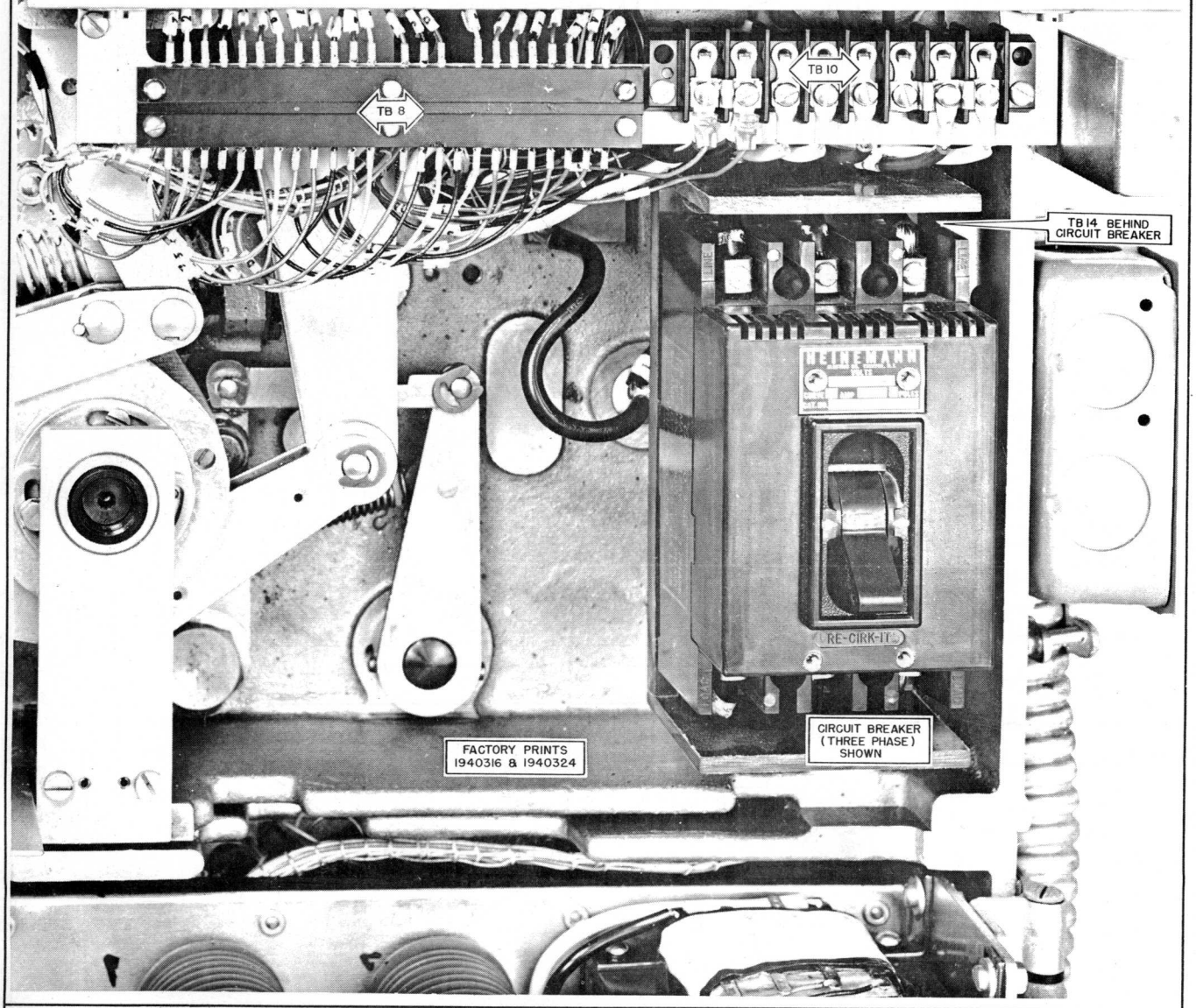
A-20	FEED EJECT ROLL (UPPER)
A-21	FEED EJECT ROLL (LOWER)
A-24	PUNCHING CHAMBER CARD STOP
A-25	EJECT ROLL (UPPER)
A-26	EJECT ROLL (LOWER)
A-53	ACTUATOR
A-54	ACTUATOR ARMATURE
A-55	INTERPOSER ASSEMBLY
A-56	SCREW
A-57	ROCKER ARM
A-58	TOWER ROD
A-59	SET BAR SECTION
A-60	TOWER ROD ASSEMBLY
A-68	LOCK SLIDE
A-69	SET BAR PIN
A-71	TOWER RETRACT CAM
A-72	RETRACT MECHANISM
A-73	RETRACT BAIL
A-74	INTERPOSER ASSEM. RESTORING LINK
A-75	PUNCHES
A-76	DIE SECTION
A-77	STRIPPER PLATE
A-78	DIES
A-79	NON-RESTORE ACTUATOR
A-80	RESET SOLENOID (L3)
A-81	YIELD SPRING
A-82	RESET BAIL
A-83	NON-RESET SOLENOID (L5)
A-84	TOWER RETRACT LATCH
A-85	LINK
A-110	REAR MAIN SHAFT

DIAL READING 81°

PUNCHING 81°

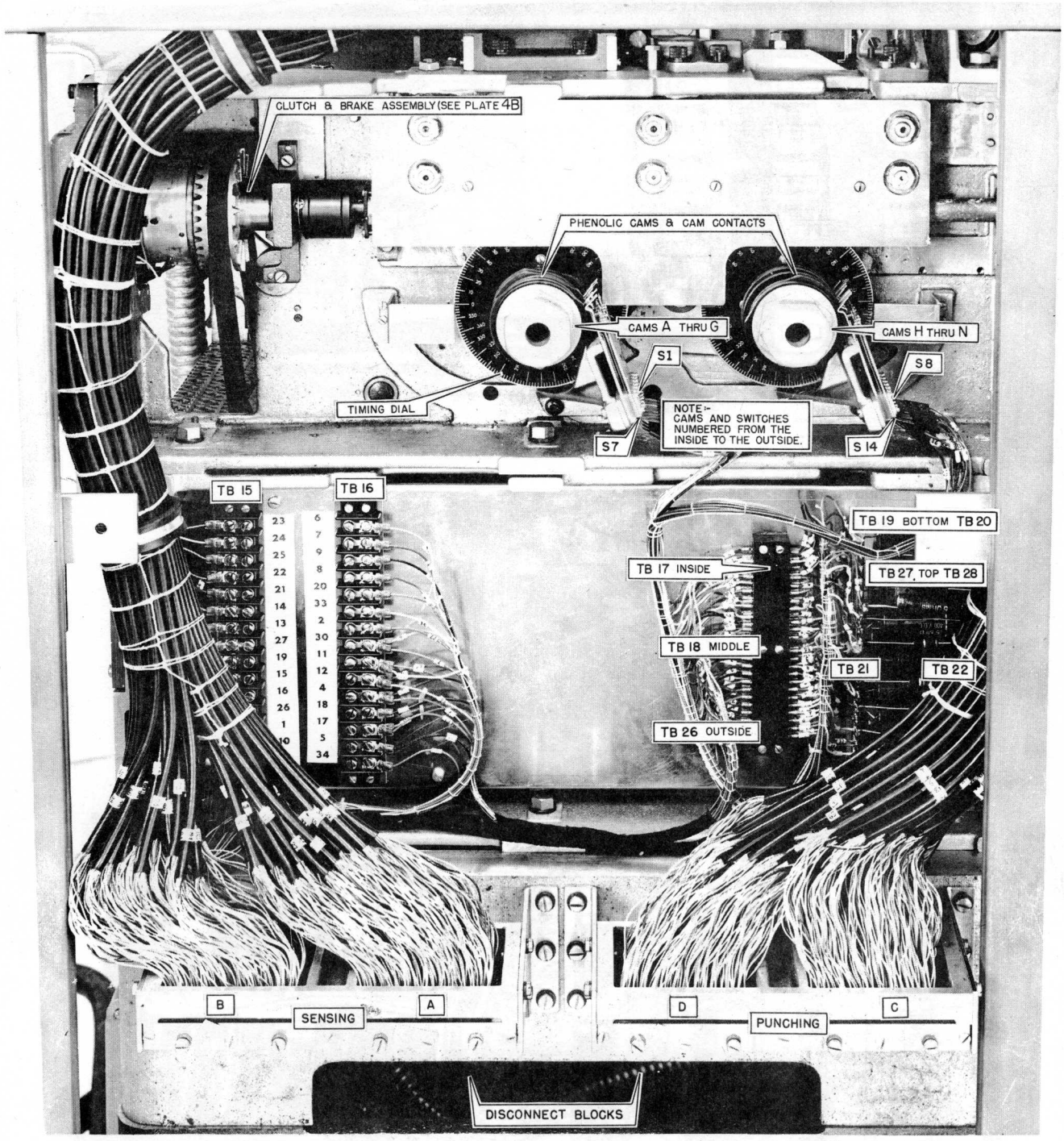
PLATE 11 B





TERMINAL BOARD - LEFT SIDE

PLATE 12 B

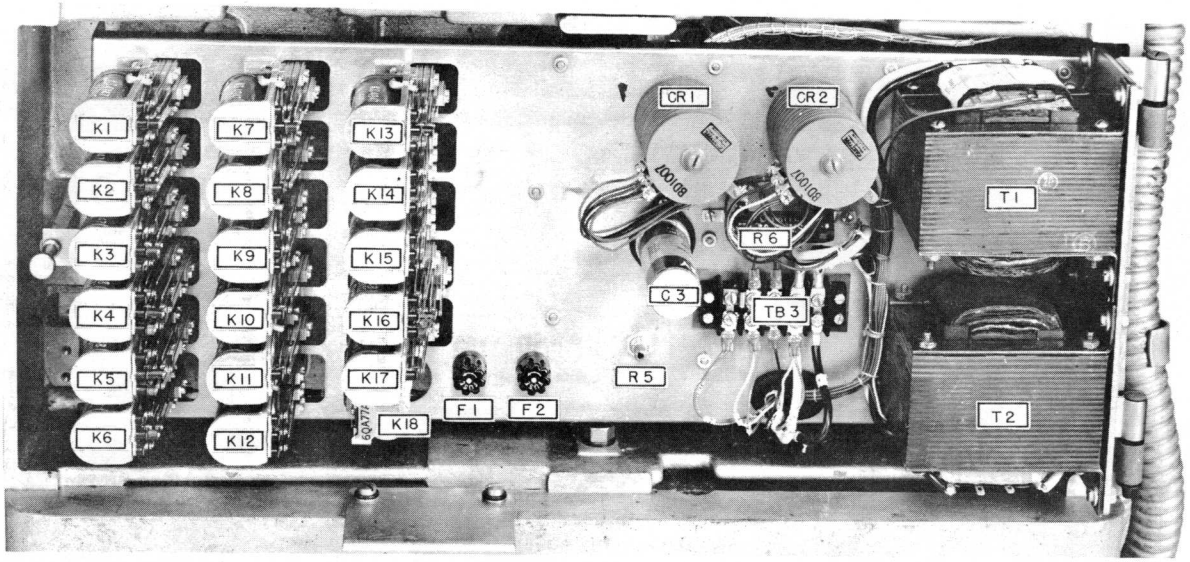


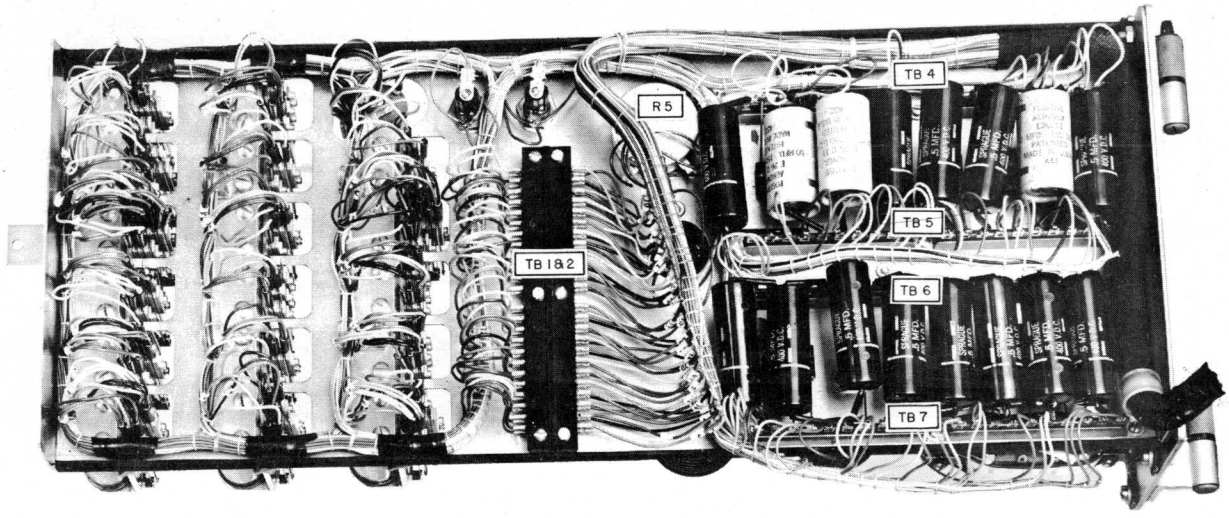
FACTORY PRINTS 1940317 & 1940321

TERMINAL BOARDS - RIGHT SIDE

PLATE 13B

TOP





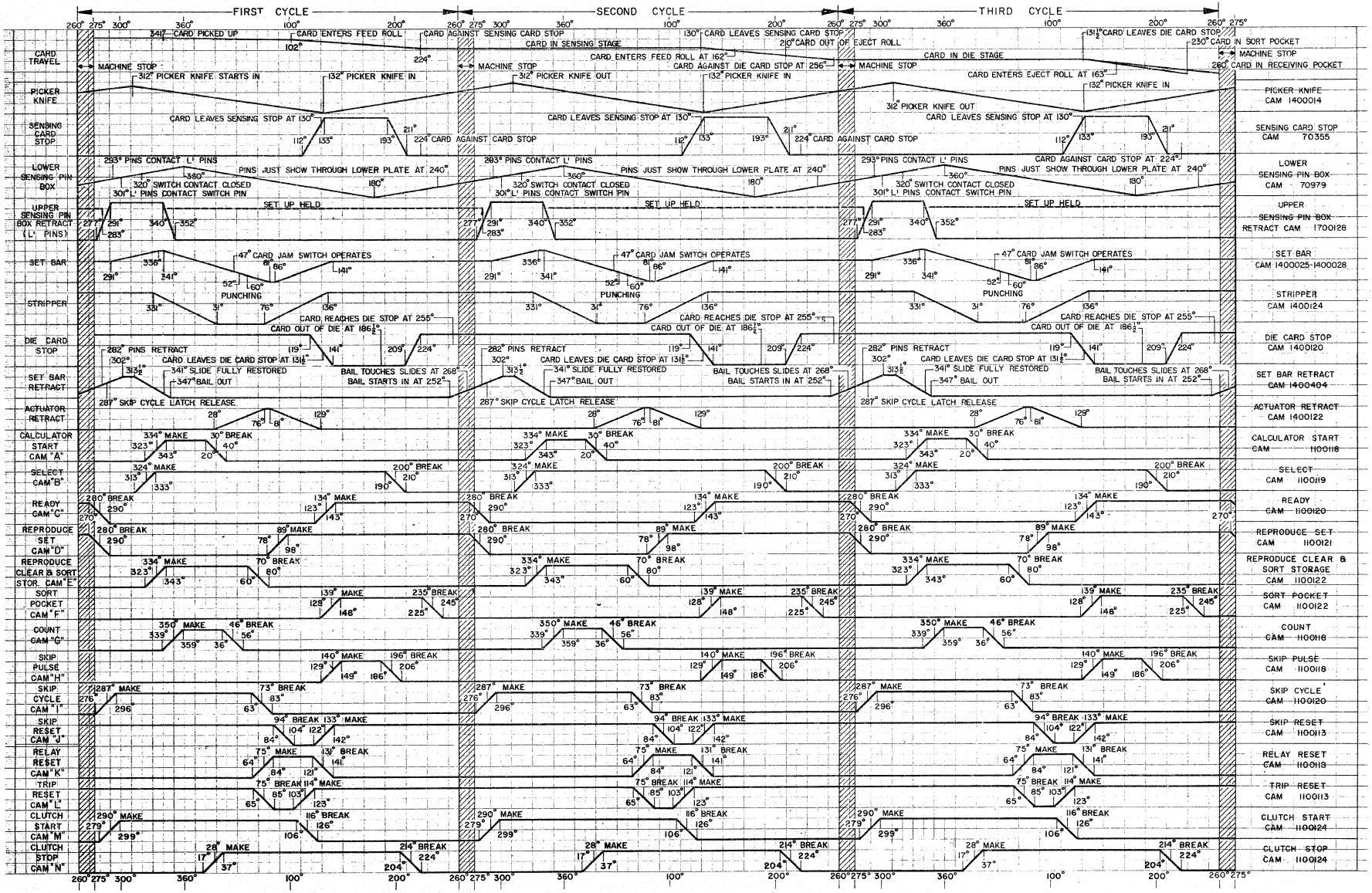
TOP

FACTORY PRINT
1940325

PUNCH POWER SUPPLY	PLATE 14B

TIMING CHART

PLATE 15 B



CIRCUIT DESCRIPTION
of the
ELECTRONIC COMPUTER
UNIVAC 60 & 120
COMPUTER

SECTION C

Remington Rand
DIVISION OF SPERRY RAND CORPORATION
315 FOURTH AVENUE
NEW YORK, N. Y.

ELECTRONIC COMPUTER
UNIVAC 60 & 120

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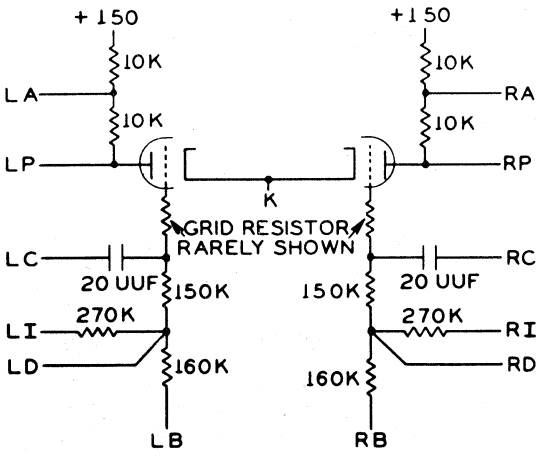


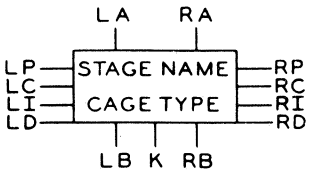


FIGURE A

BASIC CIRCUIT DESIGNATIONS AND BLOCK SCHEMATIC DIAGRAMS

1. Cage type designation:

   A) Letters represent a general cage type and the number represents a variation of the general cage type.

   B) Letter definitions:

LETTER	STAGE	NOTES
A	Pulse Amplifier	Grid return to -15 Volts unless otherwise specified.
C	A.C. Cathode follower	
D	D.C. Amplifier	Divider return to -150 Volts unless otherwise specified.
F	Flip-Flop	
G	Gate	Divider return to -150 Volts unless otherwise specified.
K	D.C. Cathode follower	Divider return to -150 Volts unless otherwise specified.
L	Limiter	
M	Multi-Vibrator	

R	Regulator Type	
RC	MISC.	Any cage not defined by other cage types.
S	Schmitt Trigger	
T	Trigger	
X		Designates tube with no associated cage.
(-)	A (-)-1	Designates unused cage section.

C. Combination of letter denotes combination of various cage types.

1. G G - Double Gate
2. D A - D.C. and A.C. Amplifier
3. L (-) - Single Limiter
4. (-) A - Single A.C. Amplifier
5. S - Schmitt Trigger

D. Left letter designates section of cage used with left tube section.

E. Right letter designates section of cage used with right tube section.

F. Single letter with (-) designates cage design to be used with half section of tube.

G. Single letter designates both section of cage and tube are used for a single function.

H. Left and right sections of tubes are defined as follows:

TUBE	LEFT SECTION				RIGHT SECTION			
TYPE	G	K	P	H	G	K	P	H
5964	6	7	1	4	5	7	2	3
6AL5	-	5	2	4	-	1	7	3

I. Grid Resistor Designations

No Symbol indicates a 680 Ω Grid Resistor.

A Triangle Symbol indicates a 22K Grid Resistor

A Square Symbol indicates a 47K Grid Resistor

A Dot Symbol is always accompanied by the given Grid Resistor Value.

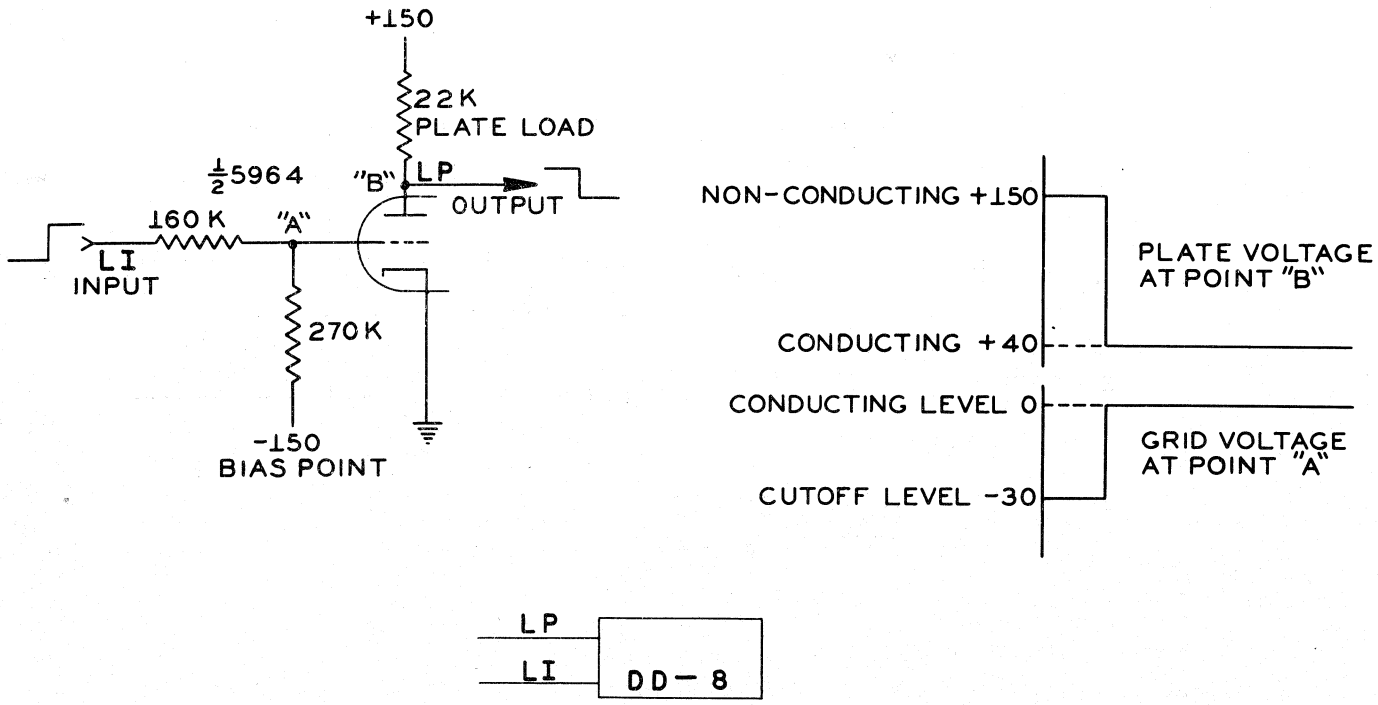


FIGURE C1

DIRECT COUPLED AMPLIFIER

The D. C. Amplifier utilizes one half of a dual triode tube and is connected as shown on Figure 1. Since the input to the grid is a resistive input, a pulse or short duration voltage change will have no effect upon the grid. Any change at the grid will be maintained for a definite length of time.

Assuming the input to the grid is low, the level of the grid is below cutoff, which will prevent any conduction between the cathode and plate. In this state, the plate potential will be +150 volts, since there is no current flow in the plate circuit and subsequent voltage drop. By raising the level of the grid to a point above cutoff, conduction will occur. With a current flow in the plate circuit and resulting voltage drop across the plate load resistor, the potential of the plate will drop to about +40 volts. Now, by lowering the grid below cutoff, the plate will rise again to +150 volts. See Figure 1 for plate levels.

The D. C. Amplifier has two stable states:

1. Conduction and current flow
   Grid high - Plate low

2. No conduction - no current flow
   Grid low - Plate high

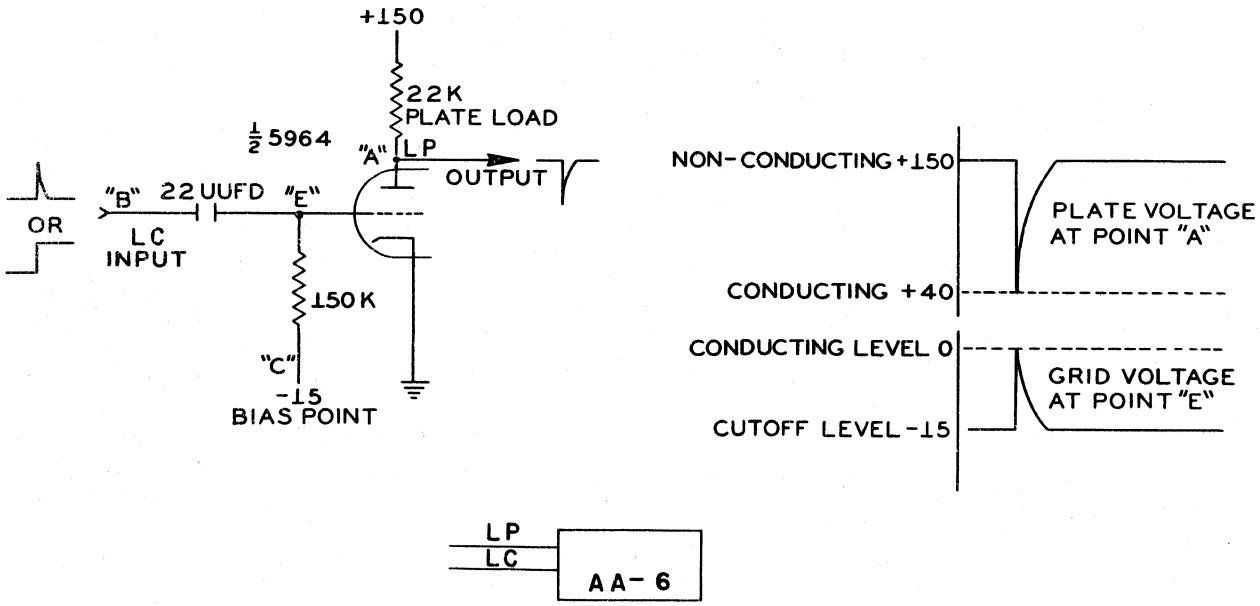


FIGURE C2

POSITIVE PULSE AMPLIFIER

A Positive Pulse Amplifier consists of a triode tube and other components as drawn in Figure 2.

First, to analyze its normal or non-conducting state, note that its cathode is tied to ground (0 voltage). The grid is tied to -15 volts through a 150K resistor. In this state, the grid voltage is of low enough potential to suppress or repel any electron emission from the cathode.

The plate is tied to a +150 volts through a 22K resistor and, in turn, to an external circuit which it is to control. Since the grid was of sufficient potential to suppress any electron flow from the cathode to the plate, there is no electron flow in the plate circuit. At this state, the plate circuit has no current flow and the potential (voltage) is present, but inactive. A +150 volt source is located at Point A. In the Computer, the function this amplifier is to accomplish will operate only on a change of potential; therefore, the condition of the tube previously explained will be of no value to us at this time.

It is necessary to change the voltage level of the plate to make use of the tube, let us see how this is done. At Point B, a rising potential, step wave or pulse, is applied. In a condenser, an equal and opposite charge will develop when a potential is applied. This positive potential is reflected on the grid, causing its level to be positive with respects to the cathode and thereby, allow conduction to occur. The electrons now flow through the 150K resistor to the opposite side of the condenser to equalize its plates.

The plate of the capacitor on the grid side now wants to return to its original value of -15 volts; but, because of the 150K resistor in the circuit, this recovery is

delayed. This delay allows the grid to pass electrons from the cathode to the plate for a longer period of time than if the 150K resistor were not in the circuit. The electrons flowing from the cathode to the plate cause current to flow in the plate circuit. The plate is tied to +150 volts through a 22K resistor. The current flowing in this plate circuit causes a voltage drop through the 22K resistor which, in Computer tubes, drops the value at Point "A" from +150 volts to about +40 volts.

The above condition was only momentary while the condenser was attempting to equalize its plates. Eventually (time being in micro seconds) the condenser will equalize and there will be no electron flow through the 150K resistor in the grid circuit. Without this electron flow, there will be no loss of potential through the resistor and, therefore, Point E will return to its original value (-15). The grid is now lowered to a negative value sufficient to stop the flow of electrons from the cathode to the plate. Since there will be no electron flow through the 22K resistor to the +150 volt source at the plate, there will not be any loss of potential through it and consequently, Point A will rise to +150 volts.

A negative pulse or step wave at Point B will only succeed in driving the grid more negative than normal. The tube was normally cutoff so the more negative value on the grid causes no reflection at the plate. This negative pulse is said to be rejected.

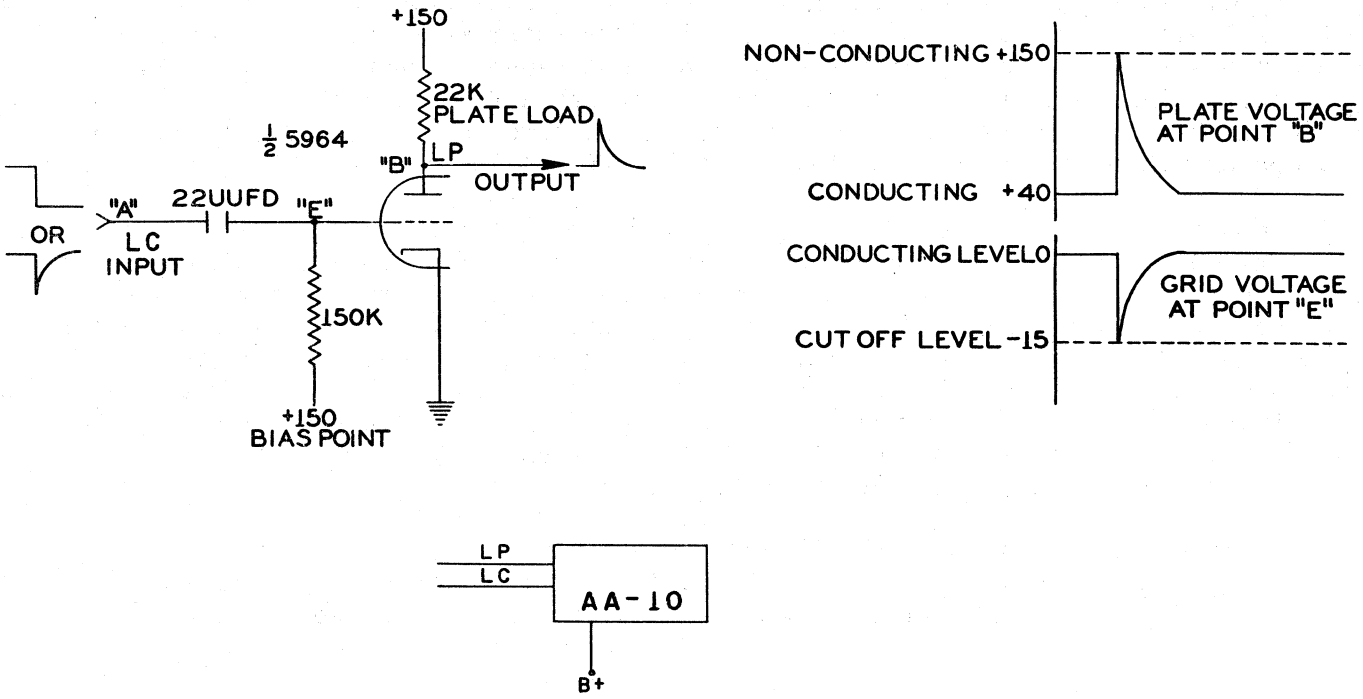


FIGURE C3

NEGATIVE PULSE AMPLIFIER

A Negative Pulse Amplifier is basically the same as the Positive Pulse type, except that its "bias point" is connected to a positive voltage source as shown in Figure 3. By connecting its grid to a positive source, conduction is maintained continuously. (The Positive Pulse Amplifier was normally non-conducting). A voltage change or pulse at Point A to a lower voltage than that normally applied would bring the grid to a value low enough to stop conduction. This voltage change on the grid occurs due to the electron flow through the 150K grid resistor while the condenser is attempting to equalize its plates. The loss of potential through the resistor is reflected on the grid recovery rate.

It was stated before that the tube was normally conducting, but now the grid was lowered and stopped this conduction. During its conduction range, the current flowed through the plate load resistor of 22K Ohms and caused a voltage drop.

Point B during this period will maintain a potential of about +40 volts, a drop of 110 volts through this resistor. Now with the grid value low enough to stop conduction, there will be no electron flow through the 22K resistor in the plate circuit. With no electron flow here, there will not be any voltage drop and Point B will rise to a +150 volts.

The condenser will eventually equalize its plates and there will be no loss of voltage through the 150K grid resistor due to no electron flow through it. The grid will now rise and allow conduction to take place. Again, there will be a loss through the plate resistor and Point B will drop to about +40 volts.

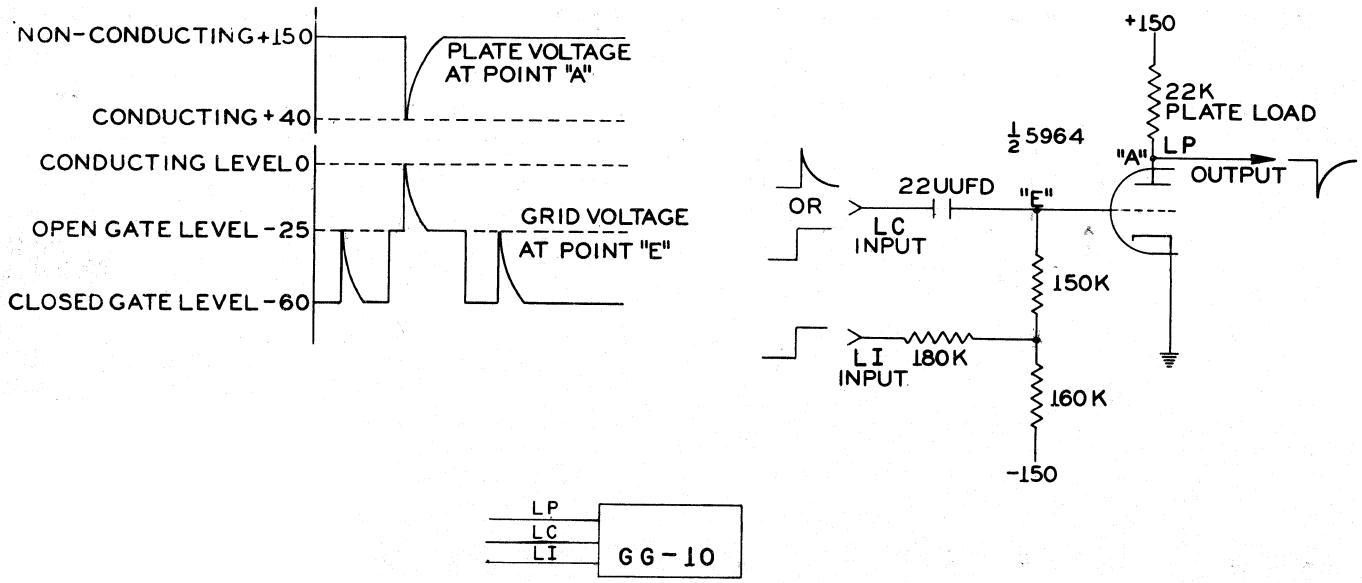


FIGURE C4

GATE

A Gate utilizes one half of a dual triode and its internal connections are shown in Figure 4.

With the cathode connected to ground and the plate to +150 volts, it can be seen that by controlling the grid potential, conduction of the tube may be controlled. By connecting the grid to -150 volts, the tube is normally cutoff. In this state, there will be no current flow and no voltage drop across the plate load resistor which will maintain a plate level of +150 volts at Point A.

The first controlling factor applied to the grid is the input at the resistive input point. By raising the potential level at this point, the current flow through the bias resistor will cause a voltage drop across it to raise the bias point from -150 volts to about -25 volts. Since the cutoff point of the tube is about -8 volts, the grid level now is still capable of stopping any current flow from cathode to plate.

It is this resistive point that is the controlling factor of the Gate. By raising the level at the resistive point of one Gate, we may have a common pulse at the capacitive point hit a series of Gates. Since only one Gate has been conditioned, only that plate will show a pulse while all the other Gates will not have any changes reflected at their plate.

When the capacitive input receives a positive potential change at one of its plates, the opposite plate starts to charge itself. During this charging time the grid potential is raised above cutoff to about 0 volts. The combination of a high resistive input and a positive pulse at the capacitive point allows the grid to permit conduction to occur.

The voltage rise caused by the charging of the capacitor will be only momentary and governed by the (R-C) resistive and capacitive component values. This means that the grid level will rise to 0 volts only for an instant then drop to -25 volts again.

This momentary change at the grid will allow conduction to take place between the cathode and plate allowing current to flow in the plate circuit. The current flow through the plate load resistor will cause a voltage drop across it, lowering the potential level of the plate to about +40 volts. Since the current will flow only for an instant, the drop across the plate load resistor will eventually decrease and the plate level will rise to +150 volts again.

1. Resistive point level raised causing grid to rise to -25 volts - no conduction.

2. Pulse at capacitive point - grid level raised to 0 volts. - Conduction occurs.

3. Capacitor charging - grid level gradually going more negative. - Conduction still takes place.

4. Capacitor fully charged - grid level lowers to -25 volts, - no conduction.

5. Grid level at -25 volts - plate at +150 volts.

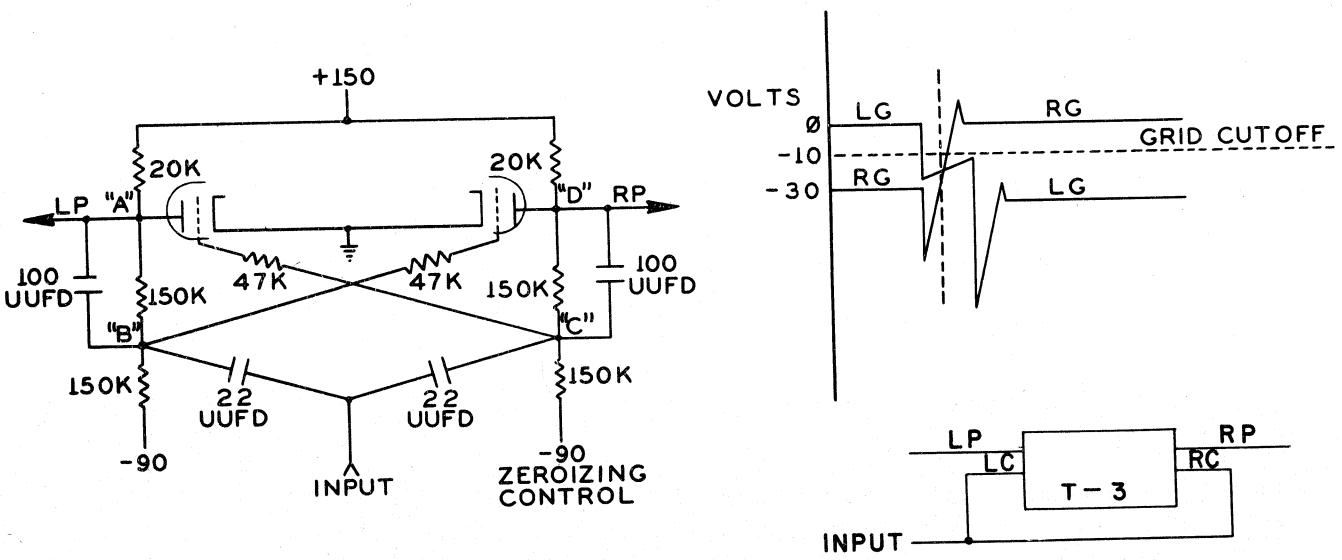


FIGURE C5

TRIGGER

The Trigger is a double triode tube with added circuit components to control its conduction periods as shown in Figure 5. The tube itself is under a common envelope with component parts connected to it, each independent of the other.

Each triode has its cathodes connected together, then to ground. Its individual plates are, in turn, connected to a +150 volt source through individual 20K resistors. As in any circuit, to maintain a current flow there must be a potential difference to cause the electrons to flow. In this case, there is a difference of ground (0 volts), the cathode potential, and a +150 volt source at the plate.

By referring to the circuit diagram, there are many resistors and condensers added to form what is called a Trigger. From each plate a line has been connected to a -90 volt source, through two resistors. Discarding the condenser at this time, the potential values at Points A and B can be found. A Trigger has two stable states. The first stable state is with the left triode conducting. This means that the left grid must have a positive value of about 0 volts. How is that value maintained?. A sequence of voltage changes at certain points, due to voltage loss through resistors, must be followed to find the two grid values. The left plate conducting holds the right grid below cutoff and the right side is not conducting.

1. When the left side conducts, there is current flow. This current flow, through the 20K resistor, results in a voltage drop, which will bring the plate potential to a plus 40 volt value.

2. Between the +40 volt plate point and the -90 volt bias point, 130 volts must be lost. If this is so, an equal amount must be lost in each resistor since their values are the same, 150K. This maintains Point B at about -25 volts.

3. The right grid is below cutoff, therefore, the right plate must be high, since there is no voltage drop across the plate load resistor. Two 150K resistors are in series between +150 volts and -90 volts, therefore, voltage lost will be such that Point C will maintain a level of about +30 volts. This in turn, connected to the left grid maintaining its level so that conduction will take place.

The Trigger is now in one of its stable states and will remain this way unless pulsed from some external source.

With the Trigger in this stable state, its left plate is at +40 volts and its right plate at +150 volts. These voltage levels are used to control the input point of a gate or will enable a neon to fire, showing the Trigger's position.

Assume a negative pulse is received at the input point. This pulse will create a potential difference across the condenser, which will charge it. During the charging period of both condensers, current will flow. The subsequent current flow, during the charging period of the condenser, will result in Points B and C dropping. These points will drop to a point where both grids will be cutoff. As shown in Figure 5, the more negative potential will rise sooner than that negative potential which was controlling the left grid. At point 1 on the graph, the condensers are fully charged and Points B and C will begin to recover. Point B or the right grid, had a more negative charge than Point C, or the left grid. The operation of the circuit is such that the more negatively charged condenser has a faster recovery rate.

Point B reaching cutoff causes the right plate to start conduction which causes a drop in voltage on the right divider at Point C. Therefore, before Point C could recover to the cutoff level its voltage is lowered because of conduction in the right plate circuit. The right grid, allowing conduction to take place, causes Point D to drop to +40 volts due to the current flow through the 20K plate load resistor resulting in a 110 volt drop across it. The voltage drop between Point D (+40 volts) and the bias point (-90 volts) must equal the 130 volt difference. Since both resistors are equal, the drops will be equal. The left grid is now cutoff.

A summary of the past operation will show that a pulse at the input point lowered both grid levels below cutoff. Since the most negative value had a more rapid rise than the other, the right grid allowed conduction to occur. This in turn, created a drop across the 20K plate load resistor, lowers Point D to +40 volts, which in turn, lowered Point C to about -25 volts. The left grid being tied to Point C is now cutoff, allowing conduction to be maintained on the right side. This is the other stable state which the Trigger will maintain.

If the input point were pulsed again, Points B and C would have the opposite values impressed upon them and result in Point C rising more rapidly. This would allow the left grid to rise and conduction would occur. The subsequent drop across the plate load resistor for the left plate would result in Point B maintaining a -25 volts. The Trigger would now be conducting on the left side and be in its original stable state.

The condensers which are connected between Points D and C and Points A and B are to create a faster reflection of any voltage changes to Points B and C. This condenser action is necessary due to the time required for a voltage to drop across the 150K resistor.

NOTE: It is also possible to trigger this circuit by a negative pulse input on the non-conducting side of the Trigger at either plate.

Only a negative pulse, or negative step wave at a capacitive point, or a negative pulse at a plate or divider point will trigger this circuit.

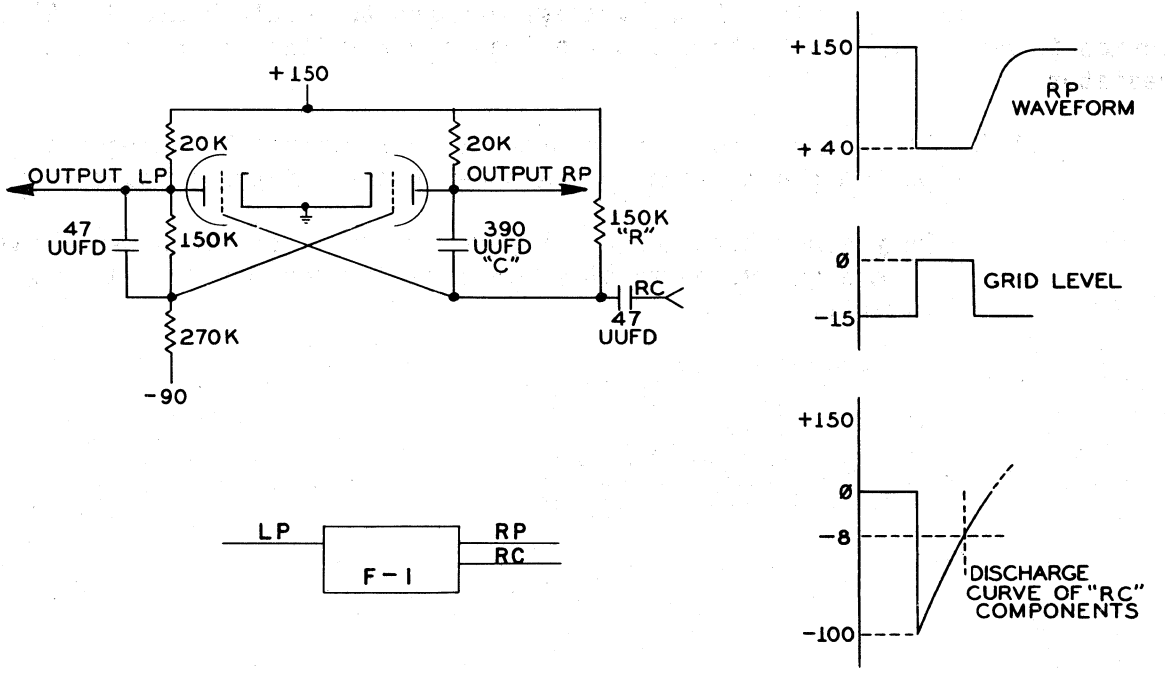


FIGURE C6

FLIP FLOP

A Flip-Flop is a double triode tube with connected components to maintain the two triodes in different states as shown in Figure 6.

The basic principle is to cause one side (one triode) to conduct for a predetermined time while the other side (one triode) is not conducting, then the two triodes will revert back to their original condition. The time that the opposite side conducts varies with the application it is to be used for.

In the normal state of a Flip-Flop, the left plate is conducting and is of a +40 volt value due to the current flow through the 20K resistor and subsequent voltage drop across it. Due to the current flow through the 150K resistor, the potential is further decreased low enough to maintain the right grid below cutoff, the right plate is not conducting and is at a +150 volt potential. In its normal state, the right plate (right triode) is maintained at +150 volts. At the same time condenser C's plates are equalized, the +150 volts is impressed at resistor "R". Due to the small current flow from the left grid to the +150 volt supply there will be a voltage drop across "R". This drop will keep the left grid just above cutoff, maintaining the left side (left triode) conducting.

Under the above conditions the Flip-Flop is said to be in a normally stationary state, i.e. conduction between the left cathode and plate with the right side not conducting.

A negative pulse (a drop of potential to a lower value than it originally was) at the 47 uufd. condenser, will cause the plates of this condenser to become unequal. Since the opposite plate must have an equal and opposite charge, electrons must travel in an attempt to adjust the other plate. The electron flow now created will cause a

voltage drop across resistor "R" which will cause the potential applied to the left grid to drop below cutoff.

The left side is now not conducting. With the current flow through the 20K plate load resistor and 150K bias resistor extremely small, the +150 volts will raise the divider point, which in turn will raise the right grid.

The value of the right grid is now high enough to allow conduction. The electron flow between the cathode and plate now causes electron flow through the 20K plate load resistor which will cause a voltage drop across it. This will bring the right plate down to about +40 volts.

NOTE: The Flip-Flop has been "Kicked"

Since the condenser "C" plates now have become unequalized electrons must flow through resistor "R" in an attempt to adjust its plates. The electron flow through "R" causes the +150 volts to drop to a lower value which will in turn be impressed at the left grid bringing it below cutoff. The electron flow through "R" and the subsequent voltage drop will last only as long as it takes condenser "C" to discharge and equalize its plates.

The current flow through "R" returns the condenser to its original state and raises the left grid above cutoff. The time necessary for condenser "C" to regain its original static condition depends upon the size of "R" and "C".

Assuming condenser "C" has become discharged, there will be less voltage drop across "R" (excluding the normal grid to plate current flow) and the left grid will rise above cutoff allowing conduction to occur at the left plate. Current flow through the left plate's 20K resistor and the 150K resistor will now bring the right grid below cutoff cutting off conduction. The right plate's potential now rises to +150 volts due to no current flow. A change of +40 volts to +150 volts is now impressed at one plate of condenser "C".

Since the plates of the condenser are attempting to rise to +150 volts, the voltage drop across "R" will not be sufficient to lower the grid left grid below cutoff.

NOTE: The Flip-Flop has now "Returned"

By following the above circuit operation, the following results were obtained.

1. A potential drop (negative pulse) was received at the right condenser.
2. The left plate which was at +40 volts, stopped conducting and rose to +150 volts.
3. The right plate which was at +150 volts, started conducting and dropped to +40 volts.
4. After a predetermined time (Condenser "C" discharging rate) the above conditions reversed themselves.

NOTE: It is also possible to trigger this circuit by a negative pulse input on the right plate or right divider point.

Only a negative pulse or negative step wave at the right capacitive point, or a negative pulse at the right plate or divider point will trigger this circuit.

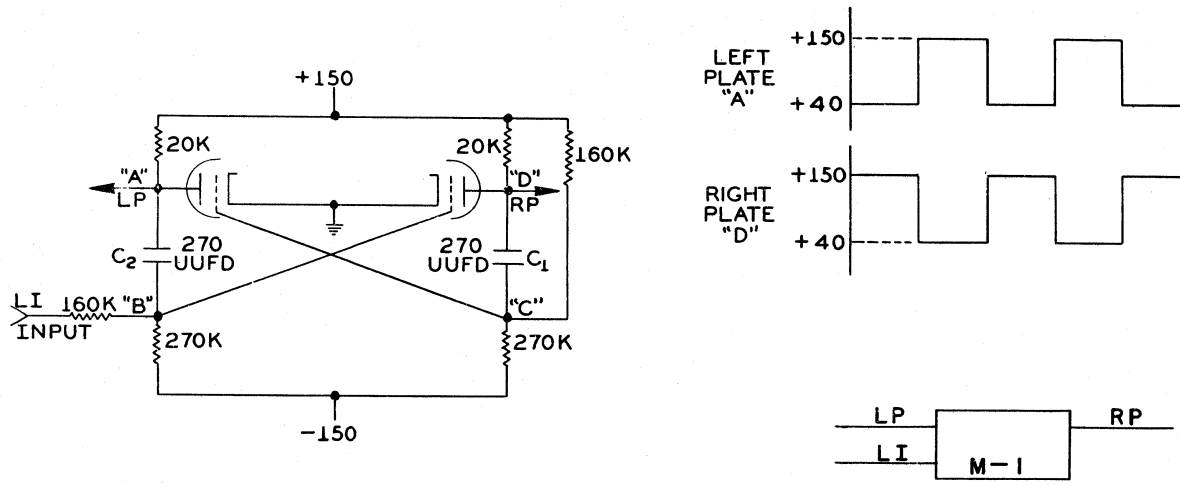
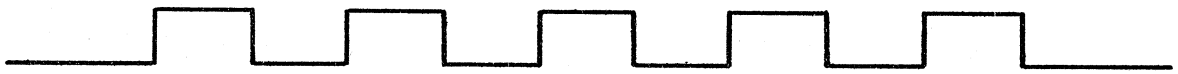


FIGURE C7

MULTIVIBRATOR

A Multi-Vibrator is designed to generate voltage variations (Square Wave Forms) at specific intervals. These square waves are the result of a plate conducting or not conducting, since a plate conducting will cause it to drop to +40 volts and a non-conducting plate will maintain a +150 volts potential.

The pulses generated are referred to as the "frequency output." This is shown by the figure below which denotes the change of voltage per second, and is governed by the R. C. (Resistive-Capacitive) components in a Multi-Vibrator.



The inoperative state of this circuit will be explained to show the various potential values at the controlling points.

With a low input, the Multi-Vibrator is considered inoperative. At the left input point a +40 volts is applied. This will hold Point B at a -30 volts, the right grid being below cutoff allows the right plate to maintain a +150 volts. Assuming the input to have been constant with C1 in a discharged state, Point C will maintain a +39 volts through the 160K shunt resistor. This will in turn hold the left grid above cutoff and allow conduction at the left plate. This current flow through the plate load resistor drops Point A to a +40 volts. Since this condition has existed for a time interval, condenser C2 is in a charged state and will have no effect upon Point B.

These are the conditions which exist when a low input is applied. The Multi-Vibrator is actually shut off.

By applying a high potential at the input point, the Multi-Vibrator will generate pulses at its designed frequency. With the input at a high potential, Point B will be raised to +30 volts which will in turn, raise the right grid above cutoff. This will create a current flow in the right plate circuit dropping Point D to +40 volts.

This change of potential on the right plate will charge condenser C1. The condenser C1 will charge to the potential now applied, and while charging, will cause a further drop across the 160K shunt resistor. Due to increased current flow and subsequent drop, Point C will lower the left grid below cutoff. Point C will maintain the left grid below cutoff as long as C1 is charging. The left plate has been cutoff and Point A rises to a +150 volts. The potential now impressed at Point A will tend to maintain Point B at a positive value through condenser C2.

Condenser C1 eventually becomes charged and the added current flow through the shunt resistor ceases, raising Point C back to a +39 volts. Since the left grid is connected to this point it will be raised above cutoff allowing conduction to occur. Current flow in the left plate circuit will cause Point A to drop to a +40 volts. This drop at Point A will be reflected upon the lower plate of condenser C2 as a 110 volt decrease. (This is the <u>equal</u> and opposite value which was changed on the upper plate). The value impressed upon the lower plate will create a current flow in its attempt to equalize itself. This current will maintain Point B at a potential sufficient to cutoff the right grid. Point B will hold the right grid below cutoff as long as condenser C2 is charging.

When the condenser C2 becomes charged Point B will rise to +30 volts and the Multi-Vibrator will revert to conducting on the right side as previously explained. The conditions described will continually change providing a high input is maintained. This will result in the changing of the right and left plates values to form a square wave output at Points A and D.

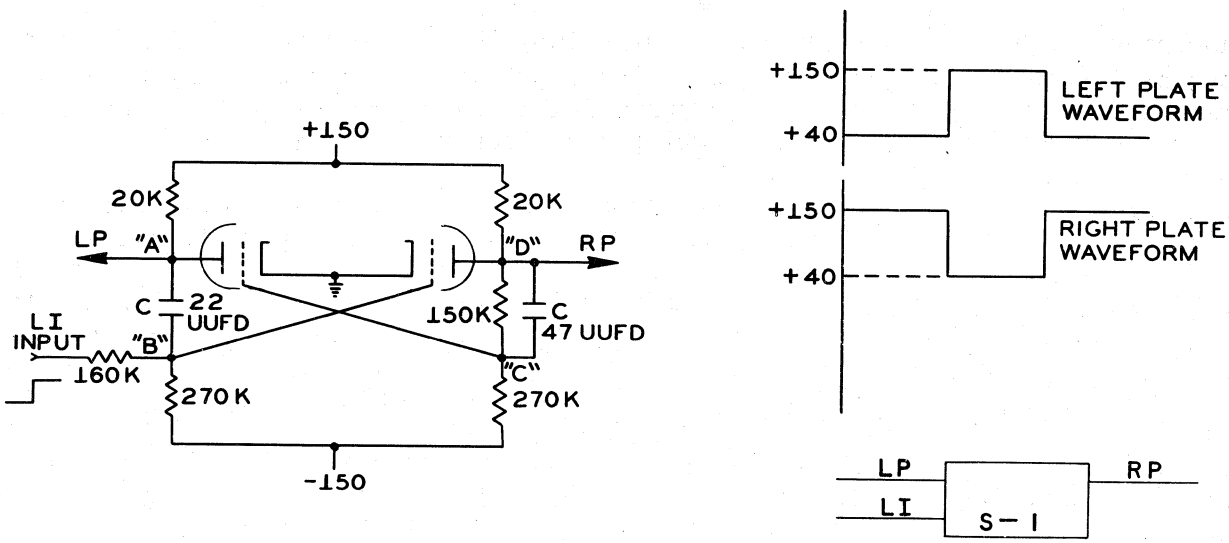
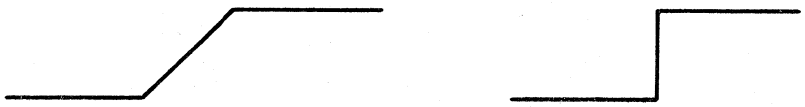


FIGURE C8

SCHMITT TRIGGER

The Schmitt Trigger differs from the regular type Trigger in that its input point is resistive rather than capacitive as shown in Figure 8. Its input must also be maintained at one level and since it has a resistive input, a pulse will not effect it.

This type Trigger is designed to change a slowly rising input to a sharply rising output.



The first stable condition to be considered is with a high input resulting in a high left plate and a low right plate. A low input will result in a low left plate and a high right plate.

After studying this Trigger circuit, the first stable condition will be reviewed. Assuming the input to be high, Point B will maintain a +30 volt potential. This +30 volts which controls the right grid will, in turn, allow conduction to occur at the right plate. The current flow at the right plate through the 20K plate load resistor to +150 volts, will drop Point D to about +40 volts. This drop to +40 will create a subsequent loss lowering Point C to a -28 volts. This in turn, is connected to the left grid which will cutoff the left side allowing the left plate to maintain a +150 volts.

Under the above conditions, the results below occurred.

1. Input high (+150 volts)
2. Right grid high (+30 volts)
3. Right plate low (+40 volts)

4. Left grid low (-28 volts)
5. Left plate high (+150 volts)

The second stable state of this Trigger will occur when the input point drops to about +40 volts. This change will drop Point B to a -28 volts which will in turn cutoff the right side.

The lowering of the right grid results in the right plate rising to a +150 volts since there is no current flow in the plate circuit and no drop across the plate load resistor. The right plate has risen from +40 to +150 volts which will charge Point C to +33 volts. The 47 mmfd condenser is inserted to reflect this change more rapidly than through the resistor. Point C rising rapidly to +33 volts will bring the left grid high enough to allow conduction at the left plate. The subsequent drop across the 20K plate load resistor will drop Point A to a +40 volts. The 22 mmfd condenser is inserted to create a sharper rise at Point B.

Under the above conditions, the results below occurred.

1. Input low (+40 volts)
2. Right grid low (-28 volts)
3. Right plate high (+150 volts)
4. Left grid high (+33 volts)
5. Left plate low (+40 volts)

NOTE: It is possible to trigger a Schmitt Trigger by controlling the voltage level on the right plate. Assume a voltage level of +40 volts is impressed on the right plate when the left resistive input is also +40 volts. The +40 volt level on the right plate will pull down the right voltage divider and cause the left grid to drop below cutoff resulting in a high level, +150 volts, on the left plate. This condition is similar to that which occurs when the left resistive input is high, +150 volts.

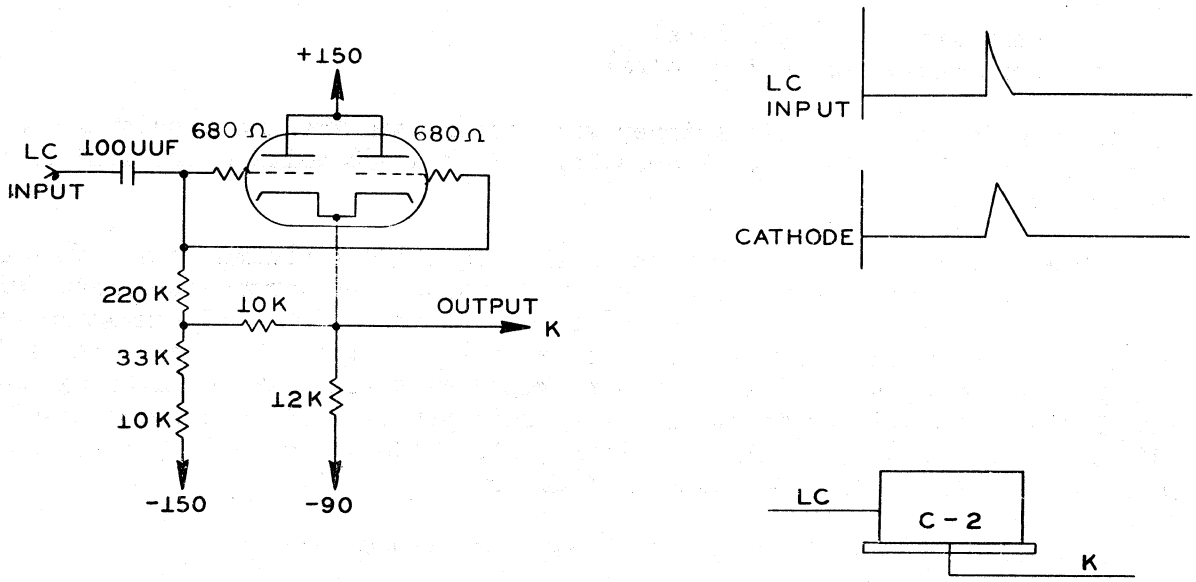


FIGURE 09

A.C. CATHODE FOLLOWER

The A. C. Cathode Follower generally employs both sides of a duo-triode as shown in Figure 9.

In this circuit the input is capacitive and reflected on the grids. The output is reflected at the cathode instead of at the plate. The load resistor for the tube is in the cathode circuit. The tube has slightly less than unity amplification factor when used as shown. It has a low impedance output and is usually used where the output signal is to be used in many stages.

The A. C. Cathode Follower, in its stable state, has a grid control which is usually sufficient to maintain the tube cutoff. This means that Point K will maintain approximately the cathode return level.

A positive pulse or step wave applied at the capacitive point will raise the grids of the tube causing conduction to occur. The length of time the tube conducts, is controlled by the capacitive resistive components of the circuit.

When the grid is raised electron flow can occur from -90, through the 12K resistor, through the tube to the +150 supply. The current flow through the 12K resistor causes a voltage drop so that point K will rise, releasing a positive pulse at the output approximately equal in magnitude to the input voltage magnitude.

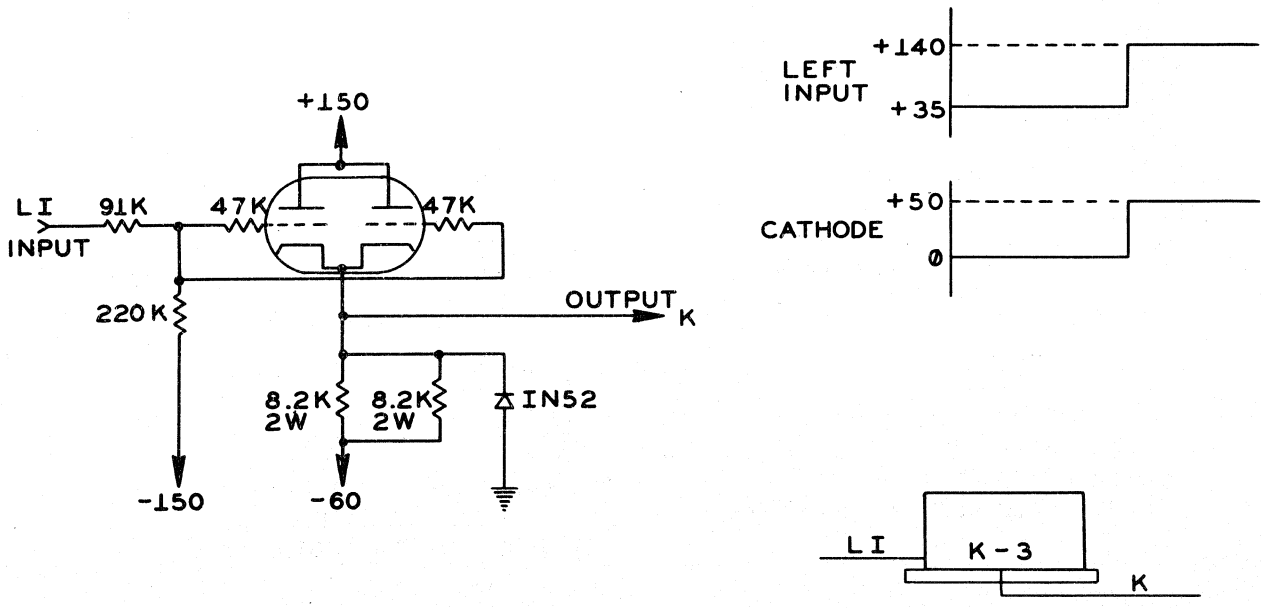


FIGURE C 10

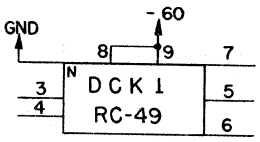
D.C. CATHODE FOLLOWER

The D. C. Cathode Follower generally employs both sides of a duo-triode as shown in Figure 10.

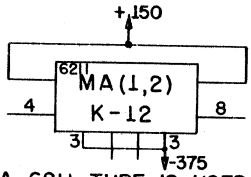
In this circuit, the input is resistive and reflected on the grids. The output is reflected at the cathode instead of at the plate. The load resistor for the tube is in the cathode circuit. The tube has slightly less than unity amplification factor when used as shown. This circuit is generally employed to control the cathode level of other stages. The input and output waveform is a step wave.

This Cathode Follower is controlled, at all times, by the level of the resistive input. The cathode or output is said to follow the grid level. If the grid is high the output is high and vice versa.

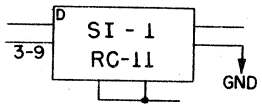
In the circuit of Figure 10, the IN52 germanium diode is used as a limiter. The output point cannot go below zero potential because of action of IN52. If the grid is lowered below ground, the tube stops conducting and the cathode remains at ground. When the grid is raised above ground, the tube conducts, IN52 stops conducting, and the cathode follows the grid level.



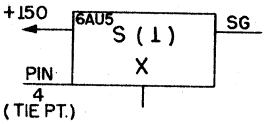
A. CAGE WITH NO ASSOCIATED TUBE.
B. NUMBERED CONNECTIONS TO CAGE ONLY.



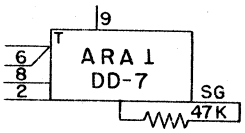
A. 6211 TUBE IS USED.
B. NUMBERED CONNECTIONS TO CAGE ONLY.



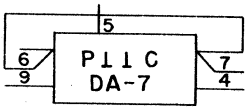
A. DIODE TUBE IS USED.
B. NUMBERED CONNECTIONS TO CAGE ONLY.



A. 6AU5 TUBE IS USED.
B. NO ASSOCIATED CAGE.
C. SG IS THE SCREEN GRID.



A. THYRATRON TUBE IS USED.
B. NUMBERED CONNECTIONS TO CAGE ONLY.
C. SG IS THE SCREEN GRID.



A. 5964 TUBE IS USED.
B. NUMBERED CONNECTIONS TO CAGE ONLY.

FIGURE C II

BLOCK SCHEMATIC EXAMPLES

Standard Notations on Block Schematics

1. A small (D) in upper left corner designates a Diode Tube is used.

2. A small (T) in upper left corner designates a Thyratron is used.

3. A small (N) in upper left corner designates no tube is used.

4. All numbers on Block Schematics refer to cage pin connections.

5. Tube pin numbers are not shown on Block Schematics.

6. A number in the RP, LP or K location generally indicates a cage connection which also connects to the corresponding tube points.

7. Lack of a number in any location indicates the connection to the tube only.

8. If two leads connect to the same location, the numbered lead is the cage pin connection and the unnumbered lead is the tube pin connection.

9. Any bias return to other than standard voltage is specified at the bias position.

The purpose of an Accumulator is to add one digit to another or subtract one digit from another. There are 22 such Accumulators in the Computer connected so as to form a ring. In other words, Accumulator 1A is connected to 2A, 2A to 3A, 11A to 1M--11M to 1A. This connection is necessary to handle the carry operation, 5 plus 7, and enable the Computer to shift the digits to different Accumulator positions.

The Accumulator does not use the 90 column code, instead a combination of Ø, 1, 2, 4, 6, and 8 is used. Each number is represented by a Trigger Circuit. A Trigger conducting on the right side will represent a value but when the Trigger is conducting on the left side it has no value. When the Accumulator has no value the TØ Trigger is right to so indicate.

The same Accumulator Triggers are used whether the Computer adds or subtracts. The add or subtract control within the Accumulator is the bias level of the Trigger Amplifiers. Each Trigger has its associated Amplifier, with its bias so controlled that a Trigger pulsing the Amplifier will increase the value in Addition or decrease the value in Subtraction. The Amplifier biases have a high or -15 volt level when effective and a low or -90 volt level when normal or ineffective.

The general operation of the Accumulator is to progress from Trigger to Amplifier to Trigger. In Addition, when a Trigger is pulsed left, its signal is fed through an Amplifier, add side, then to the next higher Trigger value to pull it right. In Subtraction, when the Trigger is pulsed left, its signal is fed through an Amplifier, subtract side, then to the next lower Trigger value to pull it right.

There are two ways in which a counter of the Accumulator may add or subtract. A negative pulse can be incoming on the Odd or Carry Line which denotes a value of one for each pulse. The maximum pulses incoming on this line is limited to two during one registration. The second method is by an incoming pulse on the Even Line which denotes a value of two for each pulse. The maximum incoming pulses on this line are limited to four during one registration.

The Accumulator has a value of zero when all Numerical Triggers are conducting left and the TØ Trigger is conducting right. These Triggers are conditioned by a Zeroize Pulse or Operation. In a Zeroize Operation either the right or left bias of the Trigger is raised to approximately ground while the other bias is retained at -90 volts. This will cause the Trigger to conduct on one side or the other depending upon which bias was raised. To Zeroize a Trigger on the left, the right bias of the Trigger is raised which results in raising the left grid so that the circuit conducts on the left. When the bias is returned to normal the Trigger Circuit is retained in this condition. To Zeroize a Trigger on the right, the left bias is raised which results in raising the right grid so that the circuit conducts on the right. Plate shows the Zeroize Line connected to the right bias of all Triggers except TØ which has its left bias connected. This means that all Triggers except TØ are Zeroized on the left.

Addition Operation

The right bias of the Amplifier stages will be raised to -15 volts by the operation

of the Sign Bias circuit, and the left bias will be retained at -90 volts. The Sign Bias circuit controls all 22 Accumulators with respect to raising the Add or Subtract Bias. This raised right bias will allow any positive pulse or step wave to pass through the right side of the Amplifiers but the left side of the Amplifiers will reject any and all pulses. The Accumulator has been Zeroized and a value of six is to be registered. A six is composed of a pulse on the Odd Line, two pulses on the Even Line, and then another pulse on the Odd Line.

The first pulse is a negative pulse on the Odd Line which hits the ØT1 Trigger at both the RC and LC points. This will trigger ØT1 to the right. The RP of ØT1 goes low to the RC of R1 where it is rejected. The LP of ØT1 goes high to the LC of R1 where it is rejected because of a low bias.

The second pulse is a negative pulse on the Even Line which hits the LC points of the TØ, T8, T6, T4 and T2 Triggers. A Trigger which is non-conducting on the left is the only one which can be triggered. The TØ is triggered left by this negative pulse. The RP of TØ goes high to the RC of R2 which releases a negative pulse at its RP which, in turn, hitting the RP of T2, pulls T2 Trigger right. The high from the RP of TØ to the LC of RC is rejected because of a low bias. The negative step from the RP of T2 to the RC of R4 is rejected.

The third pulse is another negative pulse on the Even Line which hits the LC points of TØ, T8, T6, T4, and T2. This time T2 Trigger is non-conducting on the left so the Trigger is pulled left. The RP of T2 goes high to the RC of R4 which releases a negative pulse from its RP to the RP of T4, pulling T4 right. The negative step from the RP of T4 to the RC of R6 is rejected as is the high from the RP of T2 to the LC of RØ.

The final pulse is another negative pulse on the Odd Line. Trigger ØT1 was right when this pulse occurs, so hitting ØT1 at the RC and LC points triggers ØT1 left. The LP of ØT1 goes low to the LC of R1 and is rejected. The RP of ØT1 goes high to the RC of R1 releasing a negative pulse at the RP of R1. This negative pulse from the RP of R1 is released on the Even Line and, as before, hits the LC of all Triggers. Trigger T4 is on the right so the negative pulse to its LC point returns T4 left. The RP of T4 goes high to the RC of R6 releasing a negative pulse from the RP of R6 to the RP of T6, triggering T6 right. The high from the RP of T4 to the LC of R2 is rejected because of low bias.

At the completion of the 4 pulses all Triggers are left except T6 which is right to indicate a value of 6.

Subtraction Operation

The left bias of the Amplifiers will be raised to -15 volts and the right bias will remain at -90 volts by the operation of the Sign Bias circuit. This raised left bias will allow any positive pulse or step wave to pass through the left side of the Amplifier but the right side of the Amplifier will reject any and all pulses. The Accumulator, for example, has a value of six, T6 right, and the Computer is going to subtract 3. A 3 is composed of a pulse on the Even Line then a pulse on the Odd Line.

The first negative pulse is released on the Even Line to the LC point of TØ, T2, T4, T6 and T8. The only Trigger non-conducting on the left is T6 so this negative pulse at its LC point will pull T6 left. The RP of T6 goes high to the LC of R4 which releases a negative pulse at the LP of R4 to the RP of T4, pulling T4 right. The high from the

RP of T6 to the RC of R8 is rejected because of a low bias.

The next and last pulse is a negative pulse on the Odd Line. This pulse is applied to the RC and LC point of ØT1 to pull it right. The RP of ØT1 going low to the RC of R1 is rejected. The LP of ØT1 goes high to the LC of R1 releasing a negative pulse from the LP of R1 onto the Even Line. This negative pulse on the Even Line hits the LC point of TØ, T8, T6, T4 and T2. Trigger T4 is right so the negative pulse at its LC point will pull T4 left. The RP of T4 goes high to the LC of R2 releasing a negative pulse from the LP of R2 to the RP of T2, pulling Trigger T2 right. The high from the RP of T4 to the RC of R6 is rejected because of a low bias.

The Computer has now subtracted a value of 3 from a value of 6. The Accumulator has Trigger T2 and Trigger ØT1 on the right for a total of 3.

Accumulator Overcarry Operation

An overcarry occurs when:

1. Accumulator exceeds 9 in Addition.
2. A number is subtracted from zero.
3. A number is subtracted from a smaller number.

An overcarry in an Accumulator is present when the TC Trigger is right. This TC Trigger is pulled right when T8 returns left in Addition or TØ returns left in Subtraction. In either case the pulse from the plate of RC will kick Trigger TC right. The Overcarry Condition is not corrected at the instant it occurs, but rather, after all pulses required to register a number from zero to nine have been generated.

The LP of TC goes high to the RI of AC, DC Amplifier, causing its RP to go low to the LI of CB. The RP of CB goes high opening the right side of Gate CX to condition for carries. All the AC stages, except 11A and 11M, have their right plates connected to the LI of CB so that the Computer cannot tell where the carry is needed. As shown on plate 3, the carries are released to all 22 TC triggers LC point. Whichever TC Trigger or Triggers are right will be returned left by the Carry Pulse from the plate of CA. The return of the TC Trigger to the left will do two things:

1. LP of TC returns low to the RI of AC to stop the call for carries from that Accumulator.
2. RP of TC returns high to the LC of AC releasing a negative pulse from the LP of AC which goes to the Odd and Carry Input Line of the next higher order adjacent Accumulator, 1 to 2, 2 to 3, etc. This negative pulse on the Odd and Carry Input Line will either add one or subtract one from this Accumulator depending upon which Sign Bias is high at the time.

ACCUMULATOR SHIFT OPERATION

Plate 2C

The purpose of the Accumulator Shift Operation is to shift a value from one Accumulator to another, shifting from 1A toward 11M. Shifting is necessary to place numbers in decimal alignment, place a digit in a specific Accumulator or shift a number a predetermined number of Accumulator positions.

The Shift Pulses are originated in the Decimal Counter as shown on plate 4. Each of the 22 Accumulator values shift simultaneously. Each of the 22 Accumulator operations are identical in theory of operation.

Operation

Each numerical Trigger in an Accumulator controls an associated Shift Gate. Each plate of the Trigger controls one side of a Double Gate Circuit. This means that one side of the Double Gate Circuit is always open to accept and pass a Shift Pulse. For example, assume that #1 Accumulator has a value of 4 when a shift occurs. Trigger T4 is right and all other Triggers including TØ are left. The RP of T4 is low to the LI of S4 (Gate closed). The LP of T4 is high to the RI of S4 (Gate opened). When the Shift Pulse hits Gate S4 the RP of S4 releases a negative pulse to the RP of T4 in #2 Accumulator, pulling T4 Trigger right. At the same time #1 Accumulator is shifting its value into #2 Accumulator, #11 Accumulator is shifting its value into #1 Accumulator, etc. in each of the 22 Accumulators. Trigger T2 in #1 Accumulator is left so the LP of T2 is low to the RI of S2 (Gate closed) and the RP of T2 is high to the LI of S2 (Gate open). The Shift Pulse to S2 releases a negative pulse on the LP of S2 to the LP of T2 in #2 Accumulator. If Trigger T2 of #2 Accumulator is left no change is noted but if T2 had been on the right T2 would be brought back left.

The Trigger in #1 Accumulator controls a Gate in #2 Accumulator. The resistive components of the Gate circuit are located in #1 Accumulator but the tube is in #2 Accumulator.

CARRY INPUT GENERATOR

PLATE 3C

This circuit is employed whenever an Accumulator or Accumulators exceeds its capacity. Whenever an Accumulator, by Addition or Subtraction, creates a call for carry, this circuit will create Carry Pulses to enable the Accumulator to carry out to the next adjacent higher order Accumulator. This circuit can be employed in any process. Every time a cycle of RIG is required this circuit is checked automatically to see if carries are required before the control circuits can continue. If carries are required then the control circuits wait until all carries are satisfied.

An Accumulator overcarry condition is not automatically corrected as soon as the overcarry occurs. After a cycle of RIG is completed, as shown on plate 5, all Accumulators are automatically checked for overcarries. One overcarry may, upon being satisfied, create an overcarry in the next Accumulator. If such is the case the Carry Input Generator continues to run until all overcarries are satisfied.

Operation

Assume that no Carry Triggers (TC) are right. At the same time that the RIG1 pulse is released on the completion of a cycle of RIG:

Trigger R1 is returned left, causing its LP to go low which will trigger the Flip-Flop CD to the right for a time delay of 50 microseconds. This delay is necessary to allow the RIG1 pulse to be registered in the Accumulators.

After 50 microseconds, CD returns left and its LP will release a negative step wave to the LC point of the Negative Pulse Amplifier CDA. The LP of CDA releases a positive pulse to the RC and LC points of Gate CX which at this time is open on the left. The Gate CX has its inputs controlled by the Schmitt Trigger CB. The input to CB is controlled by the 22 TC Triggers of the Accumulators through their respective AC stage.

NOTE: Accumulators 11A and 11M do not have their AC stage connected directly to the LI of CB. The RP of AC of Accumulator 11A is connected to the LI of PS11 as shown on plate 20. The RP of PS11 is connected to the LI of P11C. The LP of P11C is connected to the LI of CB. The RP of AC of Accumulator 11M is connected to the LI of C11M as shown on plate 20. The RP of C11M is connected to the LI of CCM as shown on plate 41. The LP of CCM is connected to the LI of CB.

The negative pulse released from the LP of CX is called the CX, or Carries Satisfied, Pulse and indicates the completion of carries.

Assume that one or more of the Carry Triggers (TC) are right when the RIG1 Pulse is released indicating completion of RIG:

Trigger R1 is returned left, causing its LP to go low which will trigger the Flip-Flop CD to the right for a time delay of 50

microseconds. This delay is necessary to allow the RIG1 pulse to be registered in the Accumulators.

After 50 microseconds, CD returns left, its LP releasing a negative step wave to the LC point of CDA. The LP of CDA will release a positive pulse to the RC and LC points of Gates CX. Since there is a call for carries, the input to Schmitt Trigger CB is low. The LP of CB and LI point of CX are low. The RP of CB and the RI of CX are high. The positive pulse from CDA finds Gates CX open on the right, releasing a negative pulse from its RP.

The negative pulse from the RP of CX will pull Trigger CT to the right. The RP of Trigger CT goes low to the LI point of the DC Amplifier CMA. The LP of CMA will then go high to the LI point of the Multi-Vibrator CM, causing it to operate. The Multi-Vibrator CM, going right, sends its LP high to the LI point of DC Amplifier CA. The plates of CA will release a negative step which is sent to the LC points of all 22 TC Triggers. Any TC Triggers that are right will be returned left. The Multi-Vibrator then returns left, causing its RP to go high and read the Gate CS. Gate CS is controlled by the LP of Schmitt Trigger CB. Gate CS left input will remain low until all carries are satisfied.

The Multi-Vibrator continues to send out Carry Pulses as long as a TC Trigger is right. When the last TC Trigger returns left, Gate CS does not open soon enough to stop the Multi-Vibrator CM until one additional Carry Pulse has been released.

Multi-Vibrator CM returns left, causing its RP to go high to the LC point of Gate CS. Gate CS, having a high input at this time, passes the positive pulse releasing a negative pulse at its LP. This negative pulse hits Trigger CT and returns it left. The RP of CT goes high to:

> The LI point of the DC Amplifier CMA, causing its LP to go low to the LI point of CM and shut off the Multi-Vibrator CM.
>
> The RC point of Positive Pulse Amplifier CMA resulting in a negative pulse from its RP which is the CX Pulse indicating all carries are satisfied.

Stages SCK, SCK1, CS (right side) and CSK are used in the Test Counter operation.

DECIMAL REGISTRATION AND SHIFT OPERATION

Plate 4C

When the Decimal Locator is plugged, the Input Lines (True and Complement) have been selected and their numerical value is determined with respect to the Calc. Decimal Reference Point (6/5).

The Decimal System Code is shown in the following chart.

DECIMAL POSITION	DECIMAL INPUT CODE									DECIMAL REFERENCE VALUES	
	T&C	TRUE				COMPLEMENT					
	1	2	4	8	16	2^1	4^1	8^1	16^1	TRUE	COMP.
1/0					X	X	X			16	6
2/1	X	X	X	X		X	X			15	7
3/2		X	X	X				X		14	8
4/3	X		X	X				X		13	9
5/4			X	X		X		X		12	10
6/5	X	X		X		X		X		11	11
7/6		X		X			X	X		10	12
8/7	X			X			X	X		9	13
9/8				X		X	X	X		8	14
10/9	X	X	X			X	X	X		7	15
11/10		X	X						X	6	16
NOTE:-	1	USED FOR TRUE & COMPLEMENT									

DECIMAL CODING SYSTEM

The K. B. rises and the Input Lines (True and Complement) selected through the Decimal Locator will raise the Input to the True and Complement Gates. To open the True or Complement Gates, the following requirements must be met to pass a positive pulse:

A. High Input.
B. Low Cathode.

When registering a Decimal Complement, the DBC cathode line will be low. When registering a True Decimal, the DBT cathode line will be low.

Decimal Registration is called for when DEA Flip-Flop returns left, pulling DP1 right.

A cycle of Decimal Registration consists of 5 pulses generated by the following Flip-Flops in the order listed: DP1, DP2, DP4, DP8, DP16.

The Decimal Counter is composed of five Triggers with a numerical value corresponding to its stage name. Triggers DC2 and DC8 each have a negative value. The value of the Decimal Counter is obtained by adding or subtracting the value of the Triggers conducting on the right.

Decimal Registration is completed when DP16 returns left.

An overcarry occurring during a Decimal Registration will be corrected at the completion of the Decimal RIG. DP16 returning left sends its RP high to DIC which, in turn, will return Trigger DCC left, sending out the Correction Pulse.

The Decimal Counter is also employed in a Shift Operation. Shifting is required to align one decimal position with another. The Decimal Registration prepares the Decimal Counter as to the location of a specific decimal. A count of 22 in the Decimal Counter indicates decimal alignment. Whenever the control circuit calls for shifting for decimal alignment a Shift Operation will result, even though the decimals may be already aligned. Shifting occurs from right to left.

Decimal Registration Operation

The Decimal Registration Circuit is used whenever a Decimal Registration is called for regardless of whether it is a True or Complement Registration. This circuit is also used in conjunction with the Constant 17, which is employed in the Multiplication and Division process.

The Decimal Registration circuit begins when Flip-Flop DEA is pulled right. Flip-Flop DEA is a 150 us delay. The delay is necessary to allow the Keyboard Bias to rise prior to the time the circuit begins its operation. When DEA returns left, its LP goes low to the RC point of Flip-Flop DP1, pulling it right. The LP of DP1 will go high to the LC and RC points of Gate DI1. After 25 us, DP1 returns left sending its LP low to the LC point of the Negative Pulse Amplifier DA1-16. The LP of DA1-16 will release a positive pulse to the LC and RC points of DKG.

NOTE: On a Constant 17 Registration, Trigger DK will be right and its LP will be high to the left side of Gate DKG. The positive pulse from DA1-16 will then pass through the left side of DKG and pull Flip-Flop DP16 to the right registering the 16 which thereby completes the registration of 17.

On a Decimal Registration (True or Complement), Trigger DK will be left; its RP will go high to the right side of Gate DKG. The positive pulse from DA1-16 will now pass through the right side of DKG and pull Flip-Flop DP2 right. DP2 going right sends its LP high to the RC point of D2-4T and the LC point of D2-4C. After 25 us, DP2 returns left, sending its LP low to the RC point of Flip-Flop DP4. DP4 going right will send its LP high to the LC point of D2-4T and the RC of D2-4C.

After 25 us, DP4 returns left sending its LP low to the RC point of DP8 and kick DP8 right. The LP of DP8 will go high to the RC Point of D8-16T and the LC point of D8-16C.

After 25 us, DP8 returns left, sending its LP low to the RC point of Flip-Flop DP16. DP16 going right will send its LP high to the LC point of D8-16T and RC point of D8-16C.

When DP16 returns left, it indicates the completion of Decimal Registration, (True or Complement) or Constant 17. The RP of DP16 will go high to the RC of the Positive Pulse Amplifier DIC. The negative pulse from the RP of DIC goes to the following places:

(a) The RC point of Negative Pulse Amplifier DA1-16, which will indicate to the control circuits completion of Decimal Registration.

(b) The LC point of Trigger DCC, to check for overcarry. If an overcarry is present, DCC right, this will return DCC left and initiate the correction operation as described under "Decimal Counter Shift Operation".

Decimal Counter Shift Operation

Assume that the Decimal Counter has a count of 11 at the time a call for shifts begins. A call for shifts is caused by either Trigger DRS or DAS going right. The LP of the Trigger going right will raise the input to the Multi-Vibrator SM.

Because of a backfeed from the M-V SM, when in operation, it has become necessary to isolate the plates of the Shift Call Triggers. A call for shifts from either Diode SI1, SI2 or ENM1 will cause the cathodes of these diodes to go high. This raises the left grid of stage SMC Cathode Follower. The cathode of SMC is also raised and since the right grid of SMC is fixed at ground (Ø) potential the RP of SMC stops conducting and raises the input to the M-V SM, starting it in operation. When the cathodes of the Diodes SI1, SI2 and ENM1 are again lowered, the left grid of SMC also is lowered. The cathode of SMC returning low allows the right side of the tube to conduct which lowers the voltage on the RP and shuts off the M-V SM.

The Decimal Counter, with a count of 11, will have the following Triggers right. DC1, DC2, DC4, DC8 and DC16.

The high input to the Multi-Vibrator causes it to begin its operation. When it returns left, its RP will send a positive step to the LC point of the Positive Pulse Amplifier SMG. The negative pulse from the LP of SMG hits the Negative Pulse Amplifier SMA at its RC point, resulting in a positive pulse from the RA point of SMA to the LC point of Gates SG and DIC.

NOTE: The Gates SG and DIC are controlled by the Overcarry Trigger DCC. Trigger DCC is normally left except when the count of 22 is reached or exceeded in the Decimal Counter. With DCC left at this time, its LP will be low to the LI point of Gate DIC holding it closed. The RP of DCC will be high to the LI point of Gate SG, conditioning it open.

Since Gate SG is open, the positive pulse from SMA will pass through SG resulting in a negative pulse from its LP to the RC point of the Negative Pulse Amplifier SG. The positive pulse from the RP of SG is passed through the AC Cathode Follower SK1. (There are 3 of these Cathode Followers -- 2 in parallel to insure a strong shift pulse). This pulse is the Shift Pulse which goes to all 22 Accumulators. This will advance each digit one Accumulator position.

The positive pulse from the cathode of SK1 also goes to the LC point of the Positive Pulse Amplifier DB4, resulting in a negative pulse from its LP. This negative pulse goes to the RC and LC points of Trigger DC1. Trigger DC1 will always be triggered and in this case, it will be returned left. The RP of DC1 will go high to the LC point of DB2, resulting in a negative pulse from the LP of DB2. This negative pulse will trigger DC2 and return it left. The LP of DC2, going low to the RC point of a

Positive Pulse Amplifier, is rejected. This leaves the following Triggers right: DC4, DC8 and DC16 -- indicating a count of 12.

Shift Pulses will continue to be released by the shift Multi-Vibrator increasing the DCR to a value of 21 with the following Triggers right: DC1, DC4 and DC16. The next shift pulse into the Decimal Counter will trigger DC1 left. The RP of DC1 will go high to the LC point of DB2, resulting in a negative pulse from the LP of DB2 which triggers DC2 right. The LP of DC2 goes high to the RC point of DB4, resulting in a negative pulse from the RP of DB4 which will trigger DC4 left. The RP of DC4 will go high to the LC point of DB8, resulting in a negative pulse from its plate which will trigger DC8 right.

The LP of DC8 will go high to the RC point of DB16, resulting in a negative pulse from its plate which will return DC16 left. The LP of DC16 will go low to the RC point of Trigger DCC, pulling Trigger DCC to the right. Trigger DCC going right sends its RP low to the LC points of Triggers DRS and DAS, returning whichever Trigger that was right back to the left. This Trigger returning left will lower the input to the Multi-Vibrator stopping its operation. No more Shift Pulses will be released and the Counter is now in the Overcarry Condition with Triggers DC2 and DC8 on the right.

Correction Operation

Following a cycle of Decimal Registration, it is necessary to check whether or not the Decimal Counter is in an Overcarry Position. Flip Flop DP16, returning left, indicates the completion of a cycle of Decimal Registration. The RP of DP16 goes high to the RC point of the Positive Pulse Amplifier DIC, resulting in a negative pulse from its RP. This negative pulse from the RP of DIC goes to two places:

1. To the RC of DA1-16 to continue machine operation.

2. To the LC point of Trigger DCC to check for an Overcarry Condition. If DCC is on the right, there is an Overcarry Condition and the negative pulse from DIC will return Trigger DCC left. Trigger DCC, returning left, sends out the Correction Pulse as follows:

   (a) The RP of Trigger DCC goes high to the RC point of the Positive Pulse Amplifier DB8, resulting in a negative pulse from its plate to trigger DC8.

   (b) The RP of DCC will also go high to the Positive Pulse Amplifier SMG, resulting in a negative pulse from its RP which pulls the Flip-Flop DCCD right for 25 us. This delay is necessary to allow the -8 Correction Pulse to accomplish its operation. Flip-Flop DCCD, returning left, causes its RP to go high to the RC point of the Positive Pulse Amplifier DB2, resulting in a negative pulse from its RP which triggers DC2.

   (c) The Decimal Counter is now in a corrected condition with the proper Triggers right.

Correction Operation When Decimal Counter Shifts Beyond a Count of 22

In Multiplication or Division it becomes necessary to continue shifting beyond the

count of 22. At the count of 22, Trigger DCC is pulled right. Trigger DCC being right causes its RP to go low to the LI point of Gate SG, closing the Gate. The LP of Trigger DCC will go high to the LI point of Gate DIC opening the Gate.

The next potential Shift Pulse coming from the RA point of SMA will now be blocked at Gate SG, preventing a shift of the digits in the Accumulators and also any increase in the count in the Decimal Counter. Gate DIC will pass this positive pulse from SMA, resulting in a negative pulse from the LP of DIC. This negative pulse from DIC will trigger DCC back left. DCC returning left sends out the Correction Pulses in the exact manner as described in the previous Correction Operation. At this time, when the Correction Pulses are completed, all Triggers will be left, indicating a zero value in the Decimal Counter. The next positive pulse from SMA will now pass through Gate SG and shifting will continue in the normal way.

Decimal Input Lines Limiters

The purpose of the Limiter Circuit is to prevent the grid level of the True and Complement Gates from being raised above -15 volts by the Input Lines coming from the Decimal Locator. The reason these Input Lines must be controlled is because the neons in the line can cause too great a variance in the line level when fired.

The Limiter Circuit is composed of two decimal diodes connected in series. The plate of Diode #1 is controlled by a Decimal Input Line. The cathode of Diode #1 is returned through a Resistor to -60 Volts, but is also tied to the plate of Diode #2. The cathode of Diode #2 is tied directly to -15 Volts. A rise in the input voltage will raise the plate of Diode #1, which causes it to conduct, raising the voltage on the cathode of #1 Diode through the Resistor. The plate of Diode #2 is raised, but since the cathode of Diode #2 is tied to -15 Volts, the high limit of this circuit is restricted to -15 Volts because of conduction of Diode #2.

Keyboard Bias Detector Circuit

The purpose of this circuit is to sense the presence of a Keyboard Bias and thereby prevent a CX Pulse if no Keyboard Bias is present. The control for this circuit is tied in with the Decimal Input Limiter Circuit. Whenever the Limiter Circuit cathode line is raised to -15 volts, the tube DCCL will conduct, its plate voltage will then lower the input to the Cathode Follower SCK, whose cathode will then hold the cathode of Gate CX to low (zero potential).

When the Limiter cathode lines are not raised but are approximately -45 Volts because of no Keyboard Bias, tube DCCL will not conduct and, therefore, Gate CX will end up with a high cathode which will reject all positive pulses on its grid.

NOTE: In the case of a non-Ø CK in Multiplication or Division it is necessary to add the additional 1 into 1A but no Keyboard Bias is present. This is bypassed by raising the Limiter cathode line from the LP of Trigger C9T.

REGISTRATION INPUT GENERATOR (R.I.G.)

Plate 5C

The Generator (R.I.G.) is a composition of various stages, designed to generate a predetermined amount of pulses at certain intervals. These pulses are sent to the Input & Output Chassis which will pass the required pulses necessary to register a digit. In passing through the IO chassis these pulses are inverted.

A complete set of pulses are generated in one cycle. Each cycle is generated within a total time of 125 micro seconds. The sequence in which they are generated is shown in Figure 12

Operation

The Registration Input Generator is started by pulsing the RP of RD with a negative pulse. The RP of RD will go low which holds the left grid low while the condenser is charging. This conduction will exist for 100 micro seconds which allows Sign Bias time to rise. When RD went right its LP went high hitting the R.C. point of Flip-Flop RS, which merely raised the left grid of this Flip-Flop higher allowing it to remain in its stable state. After 100 micro seconds RD returns left and its LP goes low. This drop is reflected at the capacitive input to RS which will lower its left grid allowing it to conduct on the right side for 25 micro seconds as determined by the condenser. The RP of RS going low hits the left capacitive input of R1'8, a Negative Pulse Amplifier, which will lower its grid momentarily. A positive pulse is created on the LP. This plate is connected to the two grid inputs of Cathode Follower R1'1' and will reflect a positive pulse off the cathode of R1'1'. As shown on the graph, the first pulse generated is the RIG1' Pulse. The positive change on the LP of RS will be rejected at the capacitive input of R1 since it will only raise the left grid higher.

After 25 micro seconds RS will return left and its LP will go low.

This change, being connected to the right capacitive input of R1, will trigger R1 right allowing its RP to go low. The low output from the RP to the LI point of the DC Amplifier R1M, causes the LP of R1M to go high. Its LP is connected to the Multi-Vibrator R8 which will cause the Multi-Vibrator to oscillate. With a high input the Multi-Vibrator will conduct on the right side lowering its RP. This drop is reflected at the RC of R1'8 as a negative pulse. A positive pulse results from its RP through the Cathode Follower R88. This is the first RIG 8 Pulse generated as shown in Figure

After its designed time interval Multi-Vibrator R8 returns to conducting on the left side resulting in its LP going low. This negative drop hits the double capacitive input of Trigger R4 reverting it to conducting on the right side. The RP of R4 drops and is reflected as a negative pulse at R42, a Negative Pulse Amplifier. A positive pulse from its LP hits the input points of Cathode Followers R44 and R66 resulting in both cathode points showing a positive pulse. At this time, as shown on the graph, RIG4 and RIG6 Pulses are generated.

Multi-Vibrator R8 returns right since its input is still high causing its RP to drop. This drop hits the Negative Pulse Amplifier R1'8 resulting in a positive

pulse from its RP. This pulse through Cathode Follower R88 is the second RIG 8 Pulse generated as shown on the graph.

R8 now returns left again lowering its LP which results in a negative pulse at the double capacitive input of R4, triggering it back left. The positive pulse from the RP of R8 is rejected by the Negative Pulse Amplifier R1'8.

R4, now returning left, allows its LP to drop which will in turn trigger R2 right. The RP of R2 going low to the Negative Pulse Amplifier R42 results in a positive pulse from its RP. This positive pulse hits the input points of Cathode Followers R22 and R66 which will in turn show a positive pulse at their cathodes. These two pulses are the RIG 2 and RIG 6 Pulses as shown on the graph.

Since the Multi-Vibrator still has a high input it will now return to conducting on its right side. Its RP going low, through Amplifier R1'8 to the input point of Cathode Follower R88 results in the third RIG 8 Pulse as shown on the graph.

Upon the return of R8 left, its LP will drop, reflecting a negative pulse at capacitive points of R4 triggering it right. The RP of R4 goes low to the Negative Pulse Amplifier R42. The positive pulse from its LP hits the Cathode Follower R44 and R66 resulting in RIG 4 and RIG 6 Pulses as shown on the graph.

Multi-Vibrator R8 goes right again causing its RP to go low to Amplifier R1'8. A positive pulse from its RP through Cathode Follower R88 is the last RIG 8 Pulse generated as shown on the graph.

When R8 returns left its LP going low triggers R4 back left. R4 going left causes its LP to go low which in turn triggers R2 back left. (Both right plates of R2 and R4 going high are rejected by the Negative Pulse Amplifier R42). The LP of R2 dropping hits the RC of R1M resulting in a positive pulse from its RP. This positive pulse hits the Cathode Follower R11 which will be the RIG 1 Pulse, the last pulse generated as shown on the chart. The same pulse which hit Amplifier R1M also hits the LC of Trigger R1 triggering it back left.

The RP of R1 going high to the DC Amplifier causes it to conduct dropping its LP. The lowering of the LP shuts off the Multi-Vibrator R8 since its input point is lowered.

The negative pulse from the LP of R1 is sent to the Carry Input Generator, Plate 3 stage CD, indicating a completion of an RIG cycle.

A cycle of RIG is necessary to register a number from:

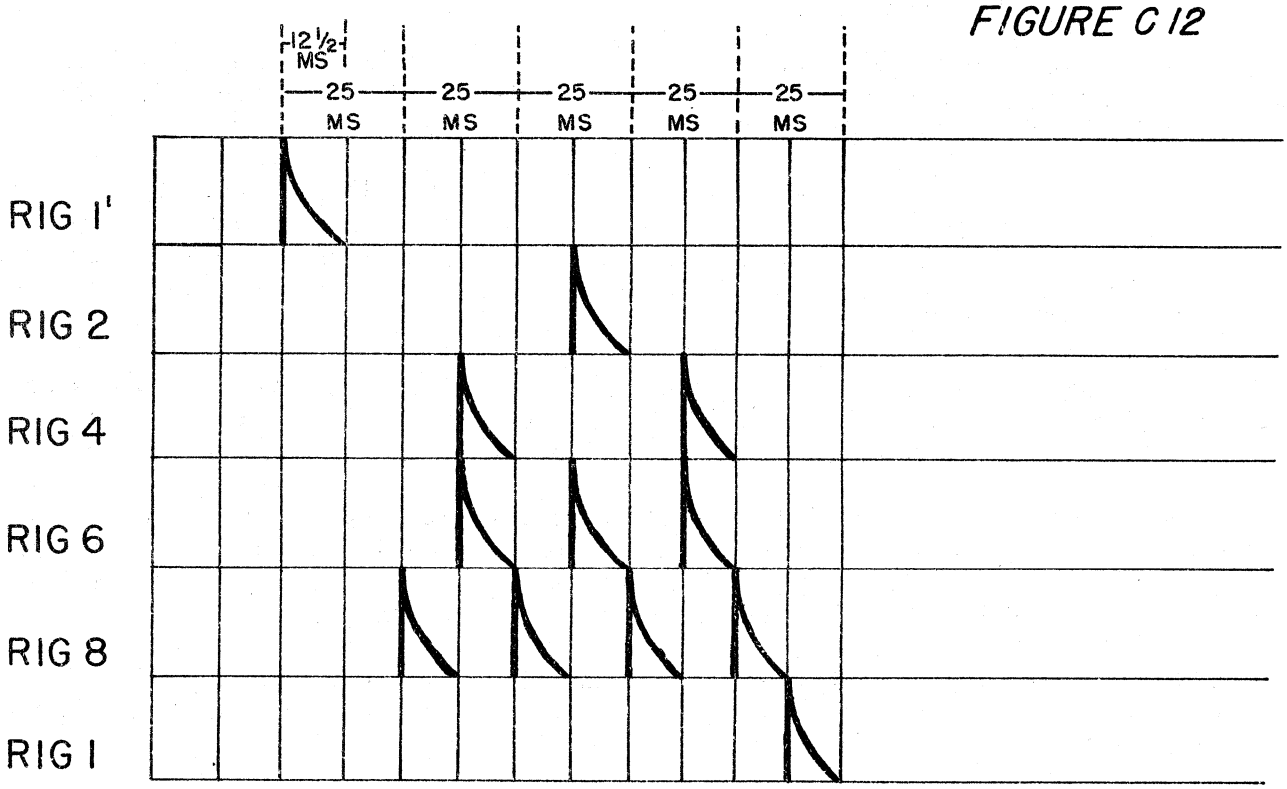
A. Card Field

B. Constants

C. Storage

REGISTRATION INPUT GENERATOR PULSES

FIGURE C 12



DECODING

DIGIT	90 COL. CODE	BI. Q. CODE	PULSES REQUIRED ON ODD LINE	PULSES REQUIRED ON EVEN LINE	
1	1	1, 0	RIG 1		
2	1, 9	2	" 1/1'		
3	3	1, 2	" 1	RIG 2	
4	3, 9	4	" 1/1'	" 2	
5	5	1, 4	" 1	" 4	
6	5, 9	6	" 1/1'	" 4	
7	7	1, 6	" 1	" 6	
8	7, 9	8	" 1/1'	" 6	
9	9	1, 8	" 1'	" 8	

INPUT CIRCUIT

Plate 6C

The INPUT DECODER is one-half of the Input-Output Chassis. There are ten of these chassis -- one for each of the 1A to 10A Accumulators. The Input Lines to the INPUT DECODER may come from any one of three places:

1. Card Field Input
2. Constants
3. Storage

The level of the Input Lines is controlled by K.B. The Input Lines are normally low and become high from a signal from K.B.

The I1, I3, I5 and I7 Input Lines all control the -60 cathode line; any one of these coming high will raise the -60 cathode line whose high voltage is limited to -15 Volts through the left side of IA9 conducting. The grid or left bias point of stage I09 will then be at -15 Volts which will allow it to pass a positive pulse. The grid or left bias point of stage IA9 will also be at -15 Volts, and since its cathode is tied to -15 Volts, this tube will conduct. The LP of IA9 will drop its voltage and, through a Voltage Divider, will pull the RG and RP of IA9 to approximately -60 Volts. This point is tied to the LD point of stage I9, holding its grid also at -60 Volts, preventing it from passing a positive pulse (RIG8). If the I9 Line is raised in conjunction with any other Input Line (even number), the only additional change is that Gate I79 is open on the right to pass the RIG1' Pulse.

In the event only the I9 Line is raised, the -60 cathode line will <u>not</u> be raised. The LD of stage I09 will be returned to -60 Volts preventing the passage of a positive pulse, RIG1. The LD of IA9 will also be returned to -60 and the tube will not conduct. The LP of IA9 will be high and through a Voltage Divider and the limiter action of the right side of IA9, will hold the LD of I9 from rising above -15 Volts. The Input Line I9 through the right side of diode C09, will hold the RD of I09 from rising above -15 Volts when the I9 Input Line is high. The RIG8 Pulse is now free to pass through the Decoder to be released on the Even Input Line.

In the event none of the Input Lines come high (zero), the circuit is similar to the condition created when only the I9 Input Line is high with this exception --

> The right side of stage I09 will have a low grid and, therefore reject positive pulses (RIG8).

The only out-going lines in this circuit are the Even Input, which increased the Accumulator value by 2 and the Carry and Odd Input Line which changes the Accumulator value by one. The Input Line indicates what value is going to register and the RIG's when it will be registered.

NOTE: RIG8 can be blocked at I9 or I09.
Any number <u>but</u> 9 and Ø will raise the cathode line (-60 Volts).

<u>Operation</u>

Assume a figure is to be registered from a closed contact of the pin box.

Keyboard Bias, as determined by the plugboard will rise and sense any closed contacts of the designated field. At this time assume that a contact is closed, designating number 1 to be registered. The high potential raises the plate of the I1 neon creating a voltage differential allowing it to fire. This will raise the plate potential of diode C17. By raising the plate potential of C17 to a more positive value than its cathode the tube will conduct. The plate current flow now causes a further drop across the 470K bias resistor raising the cathode line to a more positive value. This line cannot rise above a -15 volts. If it does, Limiter IA9 will conduct and maintain this line at -15 volts. This is due to the fact that if the left grid of IA9 becomes more positive with respect to its cathode, current will flow and keep this line at its cathode potential. The cathode of C17 is connected to I09 (left side) maintaining its grid level at a point just below cutoff.

At this time only the grid of the I09 tube was raised enough to allow an RIG Pulse to affect its grid. The grid level of the other tubes are way below cutoff and an RIG Pulse is unable to raise their respective grids high enough to allow them to conduct.

The RIG 1 Pulse hitting the left grid of I09 is sufficient to raise it high enough for conduction to occur. The LP of I09 releases a negative pulse to its respective Accumulator Odd Line. The pulse on the Odd Line will trigger the ØT1 Trigger right in the Accumulator, showing a one registered.

Reading a "3" selection will fire the I3 neon, which would raise the LP of C35. With the plate more positive than its cathode, conduction occurs and the cathode line would rise to a -15 volts as controlled by Limiter IA9.

Since the left input of Gate I35 is high, the RIG 2 Pulse will be able to raise the grid momentarily to allow conduction to take place.

The LP of I35 releases a negative pulse which will be sent out on the Even Line to register a two in the Accumulator.

The left grid of I09 is at -15 volts which allows the RIG 1 Pulse to raise the grid high enough for conduction, resulting in a negative pulse on the Odd Line to register a one. The RIG 1 Pulse is the last pulse generated and a three has been registered.

If a high input (Keyboard Bias) were maintained at lines I5 or I7 the same condition would occur as previously stated. The only exception would be that the Input Line would condition either the right grid of I35 or the left grid of I79 which would pass the RIG 4 Pulses or the RIG 6 Pulses on to the Even Line. The RIG 1 Pulse would always pass with the selection of I1, I3, I5 or I7.

The registration of a nine is accomplished by passing four RIG 8 Pulses and also the RIG 1' Pulse. With the RP of C09 at -15 volts connected to the right grid of I79 the RIG 1' Pulse will be able to raise the grid momentarily to allow conduction. This momentary conduction period results in a negative pulse on the Odd Line.

The I1, 3, 5 & 7 Input Lines are all low on the registration of a 9. The left grid of IA9 will not be raised. The left grid of IA9 will remain at -60 volts. The cathode of IA9 is at -15 volts so the grid of this tube is well below cutoff. The LP of IA9 will not be conducting therefore, its plate will be high. Through the Voltage Divider from +150V to -150V and no conduction occurring, the RP and right grid of IA9 will have a potential of approximately -15V. IA9 is used only as a Limiter to prevent the left grid of I9 from being raised above -15V. Should the

right grid of IA9 try to go higher than -15V, the tube will conduct since the cathode is tied to -15V. The left grid of I9 being held at -15V will raise high enough during the RIG 8 Pulse to emit a negative pulse from its plate for each RIG 8 Pulse (25 us intervals). The right grid of I9 is tied through a 100K resistor to +150V making it a Negative Pulse Amplifier. The negative pulses from the LP of I9 will momentarily lower the right grid of I9 resulting in positive pulses emitted from the plate. The right grid of I09 is controlled by the I9 Input Line which at this time is high. This grid is still below cutoff but the positive pulses from the RP of I9 will raise the right grid of I09 momentarily above cutoff, resulting in negative pulses emitted from its RP. These negative pulses are on the Even Input Lines into the Accumulator.

The RP of IA9 is at -15 which is connected to its grid, therefore, this is essentially a Diode Limiter. Should the RP rise above -15 volts, its right grid would also rise. The RP would be positive with respect to its cathode and the right grid would also be positive, with conduction resulting in pulling down the RP to a -15 volts. This is the action of a Limiter.

By reviewing the RIG chart it is established that one pulse on the Odd Line and four on the Even Line are necessary to register a nine in the Accumulator.

The opposite condition of this circuit may be noted when the selection of an even number is made. The Bi-Quinary system used in a Tabulating Card is such that the registration of a "2" requires a "1" and a "9". This means that the I1 Line and the I9 Line must be high for the registration of "2".

As previously explained, the I1 Line going high will raise the -60 volts bias line to a -15 volts by current flow through the 470K resistor. This line rising to -15 volts, is connected to the left grid of I09 and will enable the RIG 1 Pulse to pass through onto the Odd Line to the Accumulator.

As shown on the plate the RP of IA9 is at -60 volts which will maintain the left grid of I9 in a cutoff position. The RIG 8 Pulses are insufficient to raise the grid high enough to allow conduction. The Limiter IA9 will not conduct since its RP is more negative than its cathode.

The I9 Line being high will condition the right grid of I79 as previously described, permitting the RIG 1' Pulse to pass through, onto the Odd Line to the Accumulator.

The registration of a "2" has taken two pulses on the Odd Line with all other RIG Pulses unable to pass through.

The following is a summary of the operation of the Input Circuit.

1. The selection of 1, 3, 5, or 7 will allow the RIG 1 Pulse to pass.

2. The 3, 5 and 7 lines allow either the RIG 2, RIG 4 or RIG 6 Pulses to pass plus the RIG 1 Pulse.

3. The selection of 1, 3, 5 or 7 plus a 9 will pass their required pulses plus the RIG 1' Pulse.

4. Selection of 9 only will pass RIG 8 Pulses plus the RIG 1' Pulse.

5. The operation of the LP of C09 is described in the Minidend Registration Circuit.

DOUBLE INPUT CHECK CIRCUIT (ALPHA INPUT)

Plate 7C

A review of the Rem Rand 90 Column Code (see Input write-up) shows that no digit is represented by the raising of more than one of the 1, 3, 5 or 7 Input Lines. If the Keypunch Operator should punch, for example, a 3, 5 and 9 into a given card column instead of a desired 3, 9 (decimal digit 4), the decimal digit 8 would be entered into the Accumulator. As far as the Calculator and its proof circuitry is concerned, the Input Lines 7 and 9 were raised instead of the actual 3, 5 and 9 lines and calculations will be performed accordingly, the proof process detecting no error. This type error is detected, however, by the Input Check Circuit and the calculating process terminates as indicated by the Input Check Light on the Punch Operating Panel.

Another type error which the normal proof process of the machine cannot detect, but which can be caught by the Input Check Circuit, is that of false Storage setting. If the number to be set into Storage is the decimal digit 8 for example, then the 7 and 9 Storage Input Lines are raised. If the 5 bit should also fire, the error would not be determined by the proof process since the Proof M'd Input Registration is no different for bits 5, 7 and 9 fired than for 7 and 9 fired. Hence, the false 5 gets punched into the card by mistake.

Double Input Operation

Each Input-Output chassis has one double input sensing triode LP-MØCC, the grid of which is tied to a mixing circuit that senses the levels of the 1, 3, 5 and 7 Input Lines of that I-O chassis. If zero or one of these Input Lines is high, the LP of MØCC is cut off. If two, three or four of these Input Lines are high, the LP of MØCC is conducting. The left plates and cathode of all 10 MØCC stages are tied together so that a Double Input in any or all input columns lowers the common plate voltage activating the Calculator Kill Circuit (raising the cathode of CX). This Kill Circuit is in the Check Counter Chassis and includes the RP of IOCK. Due to the filtering required in the circuitry, it is necessary to keep all four Input Lines from raising during the portion of EZ at which time the Clear Pulse is applied to the Storage being used in that step. This is prevented by keeping the Storage Call Read-Out Bus high during EZ so that the Input Amplifiers (IS-1-L through IS-9-L), in the IO chassis will stay in conduction. This is done by raising the right grids of FK (1 through 12), through SKBH and SKBK in the Check Counter Chassis during EZ as shown on plate 10.

Input Gate Restore Operation

A restore circuit is provided in order to close the Input Gates for the Accumulator rapidly and prevent erroneous indication of a double input. These Gates might close slowly due to various capacities, from 1, 3, 5 or 7 lines. The operation of DEA to call for a Decimal Registration operates ICL through EBG. The left plate of ICL pulses the grid of the Power Pentode VTIC from cut-off to conduction. The plate of VTIC then pulls the cathode of the Isolation Diodes in IO down for 100 microseconds to return the 1, 3, 5 and 7 Gates through their -15 Volt Clamping Diodes to their

low level. ICP contains the plate load for VTIC which consists of a divider from +150 Volts to ground. ICC contains the grid capacitor and load while MSKK contains the grid bias divider for VTIC.

OUTPUT DECODER

Plate 8C

The Output Decoder is the means by which any value in an Accumulator from 1A-10A can be decoded from the Accumulator Code to the 90 Column Card Code. There is a Decoder for each Accumulator, 1A through 10A inclusive. The information from the Accumulators is decoded preparatory to being placed in Storage. The decoded number must still be read by a Storage Set Pulse (plate 10) before it can be placed in Storage. Any time a number is present in any Accumulator from 1A to 10A that number is immediately and automatically decoded.

The Output Circuit is enclosed in a chassis with the Input components to form a common Input-Output (I-O) chassis. This circuit does not utilize the RIG Pulses but merely conditions the grid of a tube. By applying the Accumulator Trigger's plate potential to the input point of a DC Amplifier to allow the plate of the Amplifier to control the grid of a tube, it will in turn control the conditioning of Storage Bits. A plate potential may be high only if the plates connected to it are also high. By connecting two or more plates together it can be seen that the input to these stages must all be below cutoff. Should any stage have a high input dropping its plate, the plates connected to it will be unable to go high. As an added control the cathodes of these stages are raised or lowered to allow an even or odd number to register.

By referring to the Accumulator Bi-Quinary System one may see that the ØT1 Trigger, if conducting on its right side, will indicate an odd number. Inversely, if the Trigger were on the left, an even number must be in the Accumulator. The right and left plates of this Trigger are connected thru Cathode Followers, ME and MO, to the cathodes they will control. (ME = odd, MO = even). Assuming ØT1 to be conducting on the right (odd number), its left plate would be high, thru MO to the cathodes of MA9, M57 and M13. With a high cathode the grids of these stages would actually be negative with respect to the cathode resulting in a high (+150 volts) plate. The right plate of ØT1 being low thru ME, would condition the cathodes of M17, M9 and M35 so they could conduct.

NOTE: The designations used on the diagram (RC and X) refer to the components within them and all stages are considered DC Amplifiers with resistive inputs.

The following examples will show how the various Accumulator Triggers condition DC Amplifiers, so they will in turn condition the IS stages which go to the D1 diodes of all the Storage Bits. Since the circuit utilizes DC Amplifiers the input and plate points will be referred to only as high or low.

Operation

A value of one is assumed to be in the Accumulator and the ØT1 Trigger is on the right. This means that the right plate of ØT1 is low thru ME which will allow the cathodes of M17 and M35 to conduct if their grid levels are raised. Whenever a cathode is lowered and its grid raised, the tube will conduct. With a high cathode and a high grid, the grid is still negative with respect to the cathode and the tube will remain cutoff.

A value of one in the Accumulator Code is a one in the 90 Column Code. When a value

of one is decoded the right cathode of IS1 will be high. It is suggested to work from the 90 Column Code value backward, to see if the conditions are present to condition this Output Line properly.

In order for the RK of IS1 to be high the RI of IS1 must be high. The RI of IS1 is controlled by the RP of M17 and the LP of M13. M13 has a high cathode so that stage is cutoff. M17 has a low cathode but the right grid is controlled by the RP of TØ which is right and therefore the right grid of M17 is low. A low cathode and low grid of M17 cannot cause conduction so the RP of M17 and LP of M13 are free to go high and raise the RK of IS1, indicating a value of one in the Accumulator.

The right cathodes of all other IS stages will be low at this time. Only one Odd Line can come high at a time.

A value of four is assumed to be in the Accumulator. Trigger T4 is the only Trigger right in this Accumulator. Trigger ØT1 is left so the RP of ØT1 is high through the Cathode Follower ME raising the cathodes of M9, M17 and M35. The LP of ØT1 is low through the Cathode Follower MO lowering the cathodes of MA9, M57 and M13.

A value of 4 in the 90 Column Code is comprised of a 3 and a 9. When a 3 is decoded the RK of IS3 is high. In order for the RK to be high the RI of IS3 must also be high. The RI of IS3 is controlled by the LP of M35 and RP of M13. M35 has a high cathode so this stage cannot conduct. M13 has a low cathode but the right grid of M13 is held low from the RP of T4. A low cathode and low grid will not allow conduction so both the LP of M35 and RP of M13 are cutoff to allow the RK of IS3 to go high.

When a 9 is decoded the RK of IS9 is high. In order for the RK of IS9 to be high the RI of IS9 must also be high. The RI of IS9 is controlled by the LP of M9 and RP of MA9. M9 has a high cathode so this stage cannot conduct. MA9 has a low cathode but the grid of MA9 is low from the LP of TØ. A low cathode and low grid will not allow conduction so both the LP of M9 and RP of MA9 are cutoff to allow the RK of IS9 to go high.

A suggested method to follow in tracing this circuit is as follows:

1. Trace backward from the IS stage the line or lines which the 90 Column Code requires for the Accumulator value.

2. Determine whether the digit in the Accumulator is odd or even and then, from the ØT1 Trigger, condition the various cathode levels.

3. Keep in mind that when two plates are tied together conduction takes precedence. In other words, if two plates are tied together and only one tube is conducting the common plate level line will be a low level.

STORAGE

Plates 9C and 10C

The Computer has 12 independent Storage units; each has the capacity of a 10 digit number and its sign. In order to make each Storage independent, each unit has associated circuitry to provide for:

(a) Storage Set
(b) Storage Hold and Clear
(c) Storage Call (Read-Out into Accumulators)
(d) Storage Read-Out into Punch Actuators

Each digit requires 5 Storage Bits; all Bits of the same numeric value in the 12 units are driven from the Accumulator Decoder Output of the same value in parallel. Similarly, the Read-Out into Accumulator Output of each bit of the same numeric value of the 12 units, drives the Accumulator Input Decoder of the same value, in parallel. The sign of storage requires the use of one Bit for each Storage.

The Punch Actuators are connected to the Bit Actuator Output through patchcords located on the Computer Field Plugboard. This arrangement permits a number to be set into the Actuators of any desired Card Column.

The Storage Bit employs the Type 5823 cold-cathode glow-discharge triode. The 5823 triode is non-conducting until the starter to cathode voltage is made to exceed the breakdown level. When the plate to cathode voltage and the starter electrode current are sufficient, the glow will transfer to the plate. After sufficient time has been allowed for transfer, the starter electrode driving voltage may be removed without interrupting plate current flow. Once the tube is fired, it will remain conducting until plate current is interrupted for an interval of time sufficient for gas deionization. Breakdown may be observed as a glow on the cathode surface.

The average starter to cathode voltage necessary for breakdown is 80 Volts; the average anode-cathode voltage after breakdown is approximately 62 Volts. The time allowed for firing (breakdown and anode transfer) is 150 microseconds. For clearing, the plate voltage is reduced for a total interval of approximately 2.6 MS.

Storage Set Driver Operation

The actual circuit method used to select a specific Storage, say S(1), is as follows: The Storage Call Line of S(1) is lowered during the interval of ER. Through the 1 side of stages FA (1,2), and stage FC (1) the Storage Call Signal undergoes voltage level shifting, inversion and amplification. The output of stage FC (1), therefore, goes high when the Storage Call of S(1) is lowered. The output of FC (1) is connected to the control grid input of the 6AU5 Set Driver (a Cathode Follower) of Storage S(1). The cathode voltage of the 6AU5, however, changes only slightly at this time due to the low screen voltage. The Set Driver tube of the selected Storage is now in a ready condition. The output of FC (1) is also connected to the input of MKD (1) to call for the Storage Decimal Location.

The Storage Call Line is also connected to the Diode FD(1,2). This Diode is used to decrease the recovery time of the Storage Call Line by pulsing the line high

at the end of the call interval.

The WHEN signal required to set S(1) is initiated by the Flip-Flop MS, which is kicked after the Test RIG has been completed as shown on plate 15.

MS is connected through stages MSK, MSKA and MSKK to the screen grids of all of the Storage Set Driver tubes. These stages provide the necessary amplification, signal inversion, level shift and low impedance source required to drive the screen circuits. The WHEN signal, therefore, pulses the screen grids of all of the 6AU5 set tubes to a high positive value, which causes the set tube of the ready Storage S(1) to go into heavy conduction, thereby producing the Set Pulse. A combination of high cathode from both the IS stage and 6AU5 Tube results in raising the starter electrode sufficiently to fire the tube. If the IS cathode were low when the 6AU5 cathode is raised, Diode D1 conducts which keeps the starter electrode below the firing level and the 100K Resistor accommodates the voltage drop between the IS and 6AU5 cathodes.

Storage Hold and Clear Driver Operation

The Storage Hold Driver is required to normally maintain the plate voltage source of the Storage Bits near ground potential, so the Bits may be fired and held in conduction, if called for. The load current of the Hold Driver varies over a wide range, as it is dependent upon the number of Bits fired in a given Storage (maximum of 21).

A controlled voltage regulated power supply consisting of a 6AS7 for the regulator series dropping tube, and one stage of feedback amplification, stage ML (S(1,2)), is used for the Hold & Clear Driver. The grid of stage ML (S(1,2)), is connected to the Hold & Clear Line and the cathode is connected to ground. Since the stage is operated as a Class A Amplifier during Hold conditions, the Hold Voltage Level will be equal to the tube bias which will vary slightly with load conditions.

During the Clear interval, the Hold and Clear Line Voltage is reduced to a low level for a period of time sufficient to cause the 5823 (glow-discharge triode) to deionize. To clear Storage, it is necessary to designate: (a) Which Storage is to be cleared, (b) WHEN it is to be cleared.

1. The Keyboard Bias is used to select the Storage to be cleared. The output of stage FC(1) is connected to the control voltage input of Gate MZ(A); thus, the Keyboard Bias, selects the Storage to Zeroize, by opening the appropriate MZ Gate.

2. The WHEN signal is supplied at the beginning of each step, to Zeroize the particular Storage selected, for the result of that step. Each step is initiated by a signal which flips EZ and EZB5. The negative pulse generated at the left plate of EZB5, upon its return, is amplified, inverted (through the right side of EPG) and drives the Cathode Follower SZK. The output of SZK is connected in parallel to the grid inputs (RC and LC points) of all MZ stages. The signal from SZK is inverted through the open MZ(A) stage, to flip the designated Storage Zeroize Flip-Flop MZ(1).

MZ(1) may also be flipped from a signal through the left side of stage MC(1), which is driven when a Clear Step has been programmed. The Storage Clear Common is connected by patch cords on the Constant and Program Panel to the input control points

of stage MC(1) to supply the WHAT designation. Due to the possible Program Board plug connections, any or all of the Storages may be cleared at the same time during a Clear step. The WHEN signal (from the Storage Clear Pulse Bus) is connected to the signal input of stage MC(1) and is supplied by circuitry located in the Output Control Chassis as shown on plate 28 . The Manual Clear Line is common to the right capacitive input of all MZ Clear Flip-Flops. Thus, the Manual Clear Signal clears all Storages.

The output of MZ(1) is used to interrupt the action of the regulator stage ML (S(1,2)).

The signal from the left plate of MZ(1) is passed through stage MA(1,2) in order to shape the wave properly and to supply the proper driving source for stages M(S(1))A and M(S1). These stages are driven into conduction for the clear interval period. Stage M(S1) overrides the controlling signal fed to the grids of the 6AS7 from ML(S(1,2)) to greatly reduce the grid voltage. Stage M(S(1))A is used as a low impedance load on the 6AS7 to insure the rapid establishment and maintenance of the low voltage level required on the Hold and Clear Line during the clear interval.

Storage Read-Out Driver Operation

In order to read out information from Storage into the Accumulators (Storage Call), it is necessary to designate: (a) WHICH Storage is to be called, (b) WHEN it is to be called.

The WHAT information is controlled by patch cord connection on the Program Plugboard which connects a V1, V2 or R line to the appropriate Storage Call S(1). The Factor Call voltage level operates the Storage Read-Out Call Line through stages FA(1,2), FB(1,2), FK(1) and a 6AS7 Cathode Follower.

With one exception - when the Storage Call Line is lowered, the output of the Storage Read-Out Call Line drops. The exception to this occurs during the interval of EZ during which time the Storage Read-Out Call Line is held high by the action of the right section of FK(1). The right section grid is driven by the Storage Read-Out Blocking Bias Line. This Blocking Bias is provided to prevent the malfunctioning of the Double Input Detector circuit, which would be actuated if both the Storage Read-Out Call and Clear Lines were low at the same time.

The WHEN designation is in the form of an RIG cycle. The voltage at point 1 is governed by which of the 3 Diodes, D3, D4 or D5, is the least negative.

1. Assume the Thyratron is fired. D3 is -105, D4 is -30 and D5 is -60. D4, therefore, controls point 1 and the voltage there is -30. When the K-6AS7 goes low to -85, point 1 will also go to -85 and D5 conducts causing the IS stage to cut off, thereby raising the input to the Decoder Gate.

2. Assume the Thyratron is not fired (no value). D3 is -30 and D4 and D5 are as in #1. D3 conducting controls point 1 keeping it at a constant -30, even though the K-6AS7 goes to -85. D5 does not conduct, therefore, the IS stage remains conducting holding its Decoder Gate closed.

Actuator Set Driver Operation

To set the information retained in the Storage Bits into the Punch Actuators, the following must be designated: (a) WHAT information is to be set, (b) WHERE it is to be set, (c) WHEN it is to be set.

The WHAT information is given in terms of the Storage unit (s) to be set, S (1), etc. Any or all of the Storages may be set at the same time.

The WHERE positioning is controlled by patch-cord connections on the Field Plugboard. This permits the setting of S (1) in the desired Card Columns. The output of each Bit of a given Storage unit must be connected by patch-cords to the proper Actuator in the Card Column selected. The WHEN signal is generated during the interval of the Set Step. This operation raises the Actuator Set Line to ground potential, which increases the Actuator currents to a point sufficient to insure their operation during the allotted Set interval.

The current requirement of the Set Line is large during the Set interval. In order to switch this current, mercury relays are used. These relays possess the characteristic of making contact with unmade contact prior to breaking the contact with the made contact.

At the time of the Set Step, a positive pulse from AAK1 or AAK2 in the Output Control Chassis as shown on plate 28, feeds the Set I and Set II Commons. The commons are connected by patch-cords to the Storage desired to be set. This pulse drives stage SRC(1) into conduction, which causes the Actuator Set Relay of Storage S(1) to close. The stage SRC(A) is used to discharge the Set Line capacity at the completion of the Set interval and to maintain the proper Set Line Voltage thereafter.

ADDITION PROCESS

Work Sheet

The True Decimal Value represents the number of Accumulator Positions between the left of the decimal and the 6M/5M reference point. The Complement Value is the complement of the True Value with respects to 22. The True Value is placed in Accumulator 1M on the work sheet, for easy reference.

This work sheet shows the procedure the Computer follows in order to add two numbers together, store the result and prove the answer. The procedure will be the same in any Addition problem. The only variations will occur in the numerical values and decimal positions.

The problem used as an example has the following values:

Minidend -- V1	33.33	7/6 decimal
Subvisor -- V2	66.66	4/3 decimal
Result -- R		5/4 decimal

CALCULATOR ZEROIZE

Plate 11C

Procedure

Line 1

The Calculator is Zeroized. All Triggers are normalized including Accumulators, Counters and Control Triggers. Storage is Zeroized.

MINIDEND REGISTRATION

Plate 13C

Line 2

The Minidend ($M^{s}d$) Decimal Complement is registered in the Decimal Counter.

Line 3

The Minidend ($M^{s}d$) Numerical Registration is made (cycle of RIG). The $M^{s}d$ value is registered in the Accumulators.

SUBVISOR REGISTRATION

Plate 14C

Line 4

The Subvisor (S'r) True Decimal value is added in the Decimal Counter.

Line 5

The Minidend (M'd) value in the Accumulators is shifted so that the M'd Decimal aligns with the S'r Decimal. This alignment is indicated when the Decimal Counter reaches 22.

Line 6

The Subvisor (S'r) Decimal Complement is registered in the Decimal Counter.

NOTE: The Decimal Counter can only accumulate to a total of 22; 22 is the same as zero so the S'r Complement Value is added from zero.

Line 7

The Subvisor (S'r) Numerical Registration is made (cycle of RIG). The S'r value is added to the M'd value which is already present in the Accumulators.

RESULT TO STORAGE

Plate 15C

Line 8

The Storage True Decimal value is added in the Decimal Counter.

Line 9

The Result value in the Accumulators is shifted so that the S'r Decimal aligns with the Storage Decimal. This alignment is indicated when the Decimal Counter reaches 22.

Line 10

The Storage Numerical Registration is made (Test RIG). The Storage value at this time is zero because of the previous Zeroize Operation (Line 1). This is a check to make certain Storage is zero. The Accumulator numerical values should not change.

Line 11

The numerical value in Accumulators 1A to 10A only are now set in Storage.

The value is still left in the Accumulators but is also present in a Storage.

Line 12

A B-2 Zeroize Operation is initiated. The B-2 Operation will zeroize Accumulators 1A to 11A only, the Check Counter and M-D Counter. At this time the main B-2 effect is on the Accumulators.

PROOF MINIDEND - STORAGE REGISTRATION

Plate 16C

Line 13

The Proof Minidend (Storage) Decimal Complement is registered in the Decimal Counter.

Line 14

The Proof Minidend (Storage) Numerical Registration is made (cycle of RIG). The value in Storage is re-entered into the Accumulators.

PROOF SUBVISOR - SUBVISOR REGISTRATION

Plate 17C

Line 15

The Proof Subvisor (Subvisor) True Decimal value is added in the Decimal Counter.

Line 16

The Proof Minidend (Storage) value in the Accumulators is shifted so that the Proof M'd Decimal aligns with the Proof S'r Decimal. This alignment is indicated when the Decimal Counter reaches 22.

Line 17

The Proof Subvisor (Subvisor) Decimal Complement is registered in the Decimal Counter.

Line 18

The Proof Subvisor (Subvisor) Numerical Registration is made (cycle of RIG). The Proof Subvisor value is subtracted (Reverse process in proof) from the Proof Minidend value in the Accumulators.

MINIDEND SUBTRACTION

Plate 18C

Line 19

The Minidend True Decimal value is added in the Decimal Counter.

Line 20

The Proof Result value in the Accumulators is shifted so that the Proof Subvisor Decimal aligns with the Minidend Decimal. This alignment is indicated when the Decimal Counter reaches 22.

Line 21

The Minidend (M'd) Numerical Registration is made (cycle of RIG). The M'd value is subtracted from the Proof Result leaving all zeros in the Accumulators.

ZERO CHECK

Plate 19C

Line 22

A Zero Check is made of Accumulators 1A to 10A. All 10 Accumulators must be zero at this time or the problem is not correct.

Line 23

A total of 10 shifts are made at this time. These shifts are counted and controlled by the Check Counter. This moves the value (Zeros) from 2M to 11M into 1A to 10A Accumulators.

Line 24

Another Zero Check is made of Accumulators 1A to 10A. After this Zero Check a total of 20 Accumulator positions have been checked for zeros. All 10 Accumulators must be zero at this time or the problem is not correct.

PROCESS	M-SECTION CALC. DEC. REF. POINT											A-SECTION INPUT											COUNTER		
	11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	DEC	M-D	CCT
MINIDEND											10				3	3	3	3							
SUBVISOR											13							6	6	6	6				
STORAGE DECIMAL											12														
1. CALC. ZEROIZED																									
2. M'D DEC. COMPL.																							12		
3. M'D NUM. REG.															3	3	3	3					12		
4. S'R DECIMAL															3	3	3	3					3		
5. M'D SHIFTED DCR AT 22																		3	3	3	3		22		CT11
6. S'R DEC. COMPL.																		3	3	3	3		9		CT11
7. S'R NUM. REG.																		9	9	9	9		9		CT11
8. STOR. DECIMAL																		9	9	9	9		21		CT11
9. RES. SHIFTED DCR AT 22																	9	9	9	9			22		CT11
10. TEST RIG																	9	9	9	9			22		CT11
11. RESULT TO STORAGE																	9	9	9	9			22		CT11
12. B-2 ZEROIZE												0	0	0	0	0	0	0	0	0	0	0	22		CT11
13. PR. M'D DEC. COMPL.																							10		CT11
14. PR. M'D NUM. REG.																	9	9	9	9			10		CT11
15. PR. S'R DECIMAL																	9	9	9	9			1		CT11
16. PR. M'D SHIFTED DCR AT 22																		9	9	9	9		22		CT11
17. PR. S'R DEC. COMPL.																		9	9	9	9		9		CT11
18. PR. S'R NUM. REG.																		3	3	3	3		9		CT11
19. M'D DECIMAL																		3	3	3	3		19		CT11
20. PR. RES. SHIFTED DCR AT 22															3	3	3	3					22		CT11
21. M'D SUBTRACTION															0	0	0	0					22		CT11
22. ZERO CHECK																							22		CT11
23. SHIFT 10																							10		CT10
24. ZERO CHECK																							10		CT10

SUBTRACTION PROCESS

Work Sheet

The first Work Sheet is an example of a negative value causing Subtraction in an Addition Process. In this example the Minidend is a negative value and the Subvisor, a larger value, is added to the Minidend to give a positive result.

The step by step procedure is exactly the same as in Addition except the Minidend is first subtracted and then added in the Proof.

The problem used as an example has the following values:

Minidend --- V1	-.15	11/10 decimal
Subvisor --- V2	1.0	2/1 decimal
Result --- R		1/0 decimal

The second Work Sheet shows the procedure the Computer follows in order to subtract one number from another, store the result and prove the answer. This procedure will be the same in any Subtraction problem which ends in zero or a positive value. A negative result is shown on the Complementize sheet.

The step by step procedure is exactly the same as in Addition except the Subvisor value is subtracted and the Proof Subvisor value added.

The problem used as an example has the following values:

Minidend --- V1	66.66	7/6 decimal
Subvisor --- V2	2.15	10/9 decimal
Result --- R		1/0 decimal

PROCESS	M-SECTION CALC. DEC. REF. POINT											A-SECTION INPUT											COUNTER		
	11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	DEC	M-D	CCT
MINIDEND											6		1	5											
SUBVISOR											15										1	0			
STORAGE DECIMAL											16														
1. CALC. ZEROIZED																									
2. M'D DEC. COMPL	PAC-R																						16		
3. M'D NUM. REG.	9	9	9	9	9	9	9	9	9	9	9	9	8	4	9	9	9	9	9	9	9	9	16		
4. S'R DECIMAL	9	9	9	9	9	9	9	9	9	9	9	9	8	4	9	9	9	9	9	9	9	9	9		
5. M'D SHIFTED DCR AT 22	4	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	8	22		CT11
6. S'R DEC. COMPL.	4	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	8	7		CT11
7. S'R NUM. REG.	5																					8	7		CT11
8. STOR. DECIMAL	5												PAC-L									8	1		CT11
9. RES. SHIFTED DCR AT 22	8	5																					22		CT11
10. TEST RIG	8	5																					22		CT11
11. RES. to STOR.	8	5																					22		CT11
12. B-2 ZEROIZE	8	5																					22		CT11
13. PR. M'D DEC. COMPL.	8	5																					6		CT11
14. PR. M'D NUM. REG.	8	5																					6		CT11
15. PR. S'R DECIMAL	8	5																					21		CT11
16. PR. M'D SHIFTED DCR AT 22	5																					8	22		CT11
17. PR. S'R DEC. COMPL.	5												PAC-R									8	7		CT11
18. PR. S'R NUM. REG.	4	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	8	7		CT11
19. M'D DECIMAL	4	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	8	13		CT11
20. PR. RES. SHIFTED DCR AT 22	9	9	9	9	9	9	9	9	9	9	9	9	8	4	9	9	9	9	9	9	9	9	22		CT11
21. M'D NUM. REG.										+	1	+	1	5											CT11
21. M'D NUM. REG.	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	22		CT11
22. ZERO CHECK													PAC-L										22		CT11
23. SHIFT 10	1																						10		CT10
24. ZERO CHECK																							10		CT10

PROCESS	M-SECTION CALC. DEC. REF. POINT											A-SECTION INPUT											COUNTER		
	11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	DEC	M-D	CCT
MINIDEND											10				6	6	6	6							
SUBVISOR											7		2	1	5										
STORAGE DECIMAL											16														
1. CALC. ZEROIZED																									
2. M'D DEC. COMPL																							12		
3. M'D NUM. REG.															6	6	6	6					12		
4. S'R DECIMAL															6	6	6	6					19		
5. M'D SHIFTED DCR AT 22												6	6	6	6								22		3
6. S'R DEC. COMPL.												6	6	6	6								15		3
7. S'R NUM. REG.												6	4	5	1								15		3
8. STOR. DECIMAL												6	4	5	1								9		3
9. RES. SHIFTED DCR AT 22	5	1																			6	4	22		3
10. TEST RIG	5	1																			6	4	22		3
11. RESULT TO STOR.	5	1																			6	4	22		3
12. B-2 ZEROIZE	5	1										0	0	0	0	0	0	0	0	0	0	0	22		Ø
13. PR. M'D DEC. COMPL.	5	1																					6		
14. PR. M'D NUM. REG.	5	1																			6	4	6		
15. PR. S'R DECIMAL	5	1																			6	4	13		
16. PR. M'D SHIFTED DCR AT 22												6	4	5	1								22		
17. PR. S'R DEC COMPL												6	4	5	1								15		
18. PR. S'R NUM. REG.												6	6	6	6								15		
19. M'D DECIMAL												6	6	6	6								3		
20. PR. RES. SHIFTED DCR AT 22															6	6	6	6					22		
21. M'D SUBTRACTION															0	0	0	0					22		
22. ZERO CHECK																							22		
23. SHIFT 10																							10		CT10
24. ZERO CHECK																							10		CT10

CALCULATOR ZEROIZE

Plate 11C

This circuit is employed at the beginning of a Program or Program Step. The circuit controls the signal required to clear the Computer before beginning a new calculation. The circuit also shows the origination of the signals required to progress from one Program Step to another.

Operation

This circuit starts its operation when Cam A in the Punch is closed and a card is in the Sensing Section. Cam A closes at 334° and opens at 30°. The closing of Cam A is called the Start Pulse and is applied to the RC of EP. EP is a 5MS delay which is used to prevent contact bounce from creating more than one Start Pulse. The LP of EP goes high to the RI of ESB1. The RP of ESB1 goes low to the RC of ESD pulling it right for a delay of 150 us, and also to the RC of EP3 pulling it right. EP3 going right removes the cutoff clamp from the Timer.

The RP of ESD goes low to the RC of ESZA releasing a positive pulse from its RP to the RC of ESZ. Though not shown, the plates of ESZ are tied in parallel to two other tubes, EP' and EPX', to produce a stronger pulse. This pulse released from the plates of ESZ is called the ESZ or Step Zeroize Pulse. This pulse is released to the LC of all Step and Function Triggers and whichever one is right, will be returned left.

The LP of ESD going high pulses the RC of ESZ1. The RP of ESZ1 releases a negative pulse to the following:

1. The RC of EP4 for a 1200 us delay to charge the Timer condenser as shown on plate 34.

2. The RC of EZB5 which goes right for 300 us. Its RP goes low for the B5 Zeroize as shown on plate 36. The LP of EZB5 also goes high to the LC of EZG releasing a negative pulse at the LP of EZG to kick EZB2 right for 300 us. The RP of EZB2 goes low for the B2 Zeroize as shown on plate 36.

3. The RP of EZ which goes right for 450 us. The LP of EZ goes high to the LI of ERAZ. The LP of ERAZ goes low to the LI of ERK lowering its cathode which is called the ERK line. The operation of the ERK line is shown on Plate 38. The lowering of the ERK line will result, when a Step Trigger goes right (ESD left), in raising the result Storage Keyboard Bias. This opens a Storage Zeroize Gate, MZ.

The LP of EZ going high to the LI of ERAZ taps off the LD of ERAZ to the grids of EZB5' a cathode follower to set up the Clamp Circuits as shown on Plate 12.

The RP of EZ goes low to the LI of SKBH and the plates of SKBH go high to the LI of

SKBK. The cathode of SKBK goes high to the right grid of all FK stages. This prevents Storage Read-Out to the Input Decoder at this time. The circuit is shown on Plate 10.

The LP of ESD while still high raised the LI of ESB1 causing the LP of ESB1 to go low and lower the Start Line on the Plugboard. This Start Line can be plugged to the In hub of any step including Function Steps such as Clear, Set or Trip. Plate 11 shows the Start Line plugged to the In line of Step 1 which opens the left side of the Diode Gate 1,2 ED. The Diode Gate operation is shown on Plate 49.

After 150 us ESD returns to the left. The LP of ESD goes low to the LC of ESIA releasing a positive pulse from the LP of ESIA. The positive pulse from the LP of ESIA goes to the LC of ESI. Although not shown, the plates of ESI are tied in parallel to two other tubes, ESI2 and ESI3 to give a stronger pulse. This pulse released from the plates of ESI is called the ESI or Step Advance Pulse.

This negative pulse goes to the capacitive points of all ED Gates and Step Advance Diode Gates. Only one of these Gates is ever open at one given time and in this case it is the left side of 1,2 ED. This diode is still open, even though ESD returned left, and therefore releases a negative pulse from the LP of 1,2 ED to the RD of 1ES, triggering 1ES right. The LP of 1ES goes high to the LI of 1,2 ESF as shown on Plate 38. At this time the ERK line is low (EZ right) so the result Storage Zeroize Gate MZ is opened.

EZB2 and EZB5 return left completing their respective Zeroize operations. The LP of EZB5 goes low to the following:

> The RC of ESCG releasing a positive pulse on the RP of ESCG to the LC of ESCG Gate. This Gate is open as long as MC2 is left, no Complementize Operation. The negative pulse from the LP of ESCG goes to the RC of EPG and the RC of EMZ kicking EMZ right as a Storage Clear Guard Delay, this delay is approximately 5MS and its use is shown on plate 15. The positive pulse from the RP of EPG is fed to the LC of SZK. The positive pulse from the cathode of SZK hits all MZ Gates. One MZ Gate is opened, high Storage KB, and that Storage is Zeroized as shown on Plate 10.

EZ, after its full delay of 450 us, returns left. The LP of EZ returning low does the following;

1. Hits the RC of EM pulling EM right. See Plate 13 for this operation.

2. Goes low to the LI of ERAZ coming off the LP of ERAZ high raising the ERK line and lowering Storage KB.

3. Goes low to the LI of ERAZ coming off the LD of ERAZ low to grids of ØFZT and EZB5'. EZB5' removes the clamping action. ØFZT allows its RP to go high to the RC of ØC2. The RP of ØC2 releases a negative pulse to the RP of ØFD1. ØFD1 goes right for 25 us and while on the right the LP of ØFD1 goes high to the grids of ØLD1 and ØLD2. The cathodes of ØLD1 and ØLD2 go high to all KBR and FD stages, as shown on Plate 37. This operation is called the KB Recovery Operation and occurs also at each Control Ring Pulse Time.

CLAMP CIRCUITS

Plate 12C

There are certain stages in the Computer which must be held inoperative during a B-2, B-5 Zeroize. This clamping operation is necessary to prevent transient pulses, which may occur during Zeroize time, from causing more than one operation to occur once the Zeroize is completed.

This circuit shows all the clamped stages and their clamp tubes. Stage SM is not clamped during Zeroize but only whenever the Decimal Counter is being corrected. The LP of DCCD, during correction, is high to the LI of DN12'. The LD of DN12' taps off high to the LD of DCCL. The LP of DCCL goes low to the RD of SM which is the right grid of SM. This clamp prevents SM from conducting on the right whenever DCCD is right.

MINIDEND REGISTRATION

Plate 13C

This plate illustrates the controls required to enter the Minidend Decimal Complement into the Decimal Counter and the Minidend Numerical Value into the Accumulators. The circuits that do the actual registrations are not shown. Only the circuits required to control when the operations are to be performed are shown. This circuit is employed in every process and in every calculating step. The difference from step to step would be in the decimal or numerical values.

Operation

EZ returns left following the Zeroize operation shown on plate 11. The LP of EZ returns low to the RC of EM pulling EM right. The LP of EM goes high to the LI of EMA. The LD of EMA taps off high to the LD of DMP raising the LP of DMP to the following:

1. LI of DMG to open the Gate.

2. LP of diode EIA3 to prepare Sign Bias as shown on Plate 43.

3. LI of DMD causing the LP of DMD to go low to the RP of DEM and LI of DBC. The K-DBC goes low conditioning the Decimal Counter for a Decimal Complement Registration as shown on Plate 4. The LP of DEM goes high to the RC of DEA1 releasing a negative pulse from the RP of DEA1, kicking DEA to the right. DEA has a 150 us delay to allow KB to rise. The LP of DEA goes high to the RC of EBG releasing a negative pulse at the RP of EBG to kick ICL right. The LP of ICL goes high for 100 us which causes the 6AU5, VTIC, to conduct causing the Input Recovery Circuit to operate.

   NOTE: Every time DEA functions the Input Recovery Circuit functions. This is the only plate where this operation is shown. The Input Recovery Circuit lowers the input level of the Input Decoder to prevent the possibility of a Double Input occurring during the period of time it takes to change from one KB to another.

The LP of EM going high to the LI of EMA will lower the LP of EMA and the LI of EMK. The K-EMK goes low to all EMF stages, as shown on plate 38, and lowers the V1 position on the plugboard. V1 being lowered raises KB for the Minidend to condition the Decimal Counter and Input Decoder Gates, plates 4 and 6. The LP of EMA goes low to the LC of diode ENM. This pulses the K-ENM so that the LP of ENM releases a negative pulse to the RD of PAMD. PAMD has a 250 us delay for KB to rise and, on its return left, checks for (-) Factor as shown on plate 20.

DEA, after 150 us, returns left and its LP goes low to the RC of DP1 starting the Minidend Decimal Complement Registration as shown on plate 4.

The completion of this Decimal Registration is a negative pulse to the RC of DA1-16 whose plate releases a positive pulse to the LC of the opened Gate DMG. The LP of DMG releases a negative pulse to the RP of DRB, triggering DRB right. The RP of DRB goes low to raise Sign Bias as shown on plate 43 . Raising Sign Bias creates a cycle of RIG which now registers the value of the Minidend into the Accumulators.

The CX pulse to the LC of DRB signals the completion of the Numerical Registration and DRB returns left. The RP of DRB returns high to lower Sign Bias and pulse the LC of EPG. The negative pulse from the LP of EPG is a Control Ring Pulse and, as shown on plate 39 , returns EM left. The Control Ring Pulse also causes the KB Recovery Circuit to function through ØFD1, ØLD1 and ØLD2.

The return of EM left lowers the LP of EM which goes to the RC of ES and ES is brought right. The Computer now proceeds into the Subvisor Registration Control Circuit Operation.

SUBVISOR REGISTRATION

Plate 14C

This plate illustrates the controls required to perform the Subvisor functions in Addition or Subtraction. These functions are:

1. Subvisor True Decimal Registration.
2. Shift Operation to align the M'd Decimal with the S'r Decimal.
3. Subvisor Decimal Complement Registration.
4. Depending upon the process, the S'r is either added or subtracted.

Operation

Trigger EM is returned left by a Control Ring Pulse and the LP of EM going low to the RC of ES triggers ES right. The LP of ES goes high to the LI of ESA. The LP of ESA goes low to the LI of ESK. The K-ESK goes low to all ESF stages and the ESF stage with the high input has its plate lowered to pull down the V2 position on the Plugboard. V2 going low is plugged to a KB Call Line and KB for V2 is raised. KB conditions the Decimal Gates, Input Decoder Gates and checks for Minus Indication. The LD of ESA goes high to the RD of EMZ. The RP of EMZ' goes low to the LI of CGA. The LP of CGA goes high to the LI of CTSG to open the Check Counter to count the Subvisor shifts as shown on plate 41 . The RP of ES goes low to the LI of EP2 to check on the Process as shown on plate 40 . A high signal is returned from Process Control to raise the LI of DPG2 and pulse the LC of DEA2. The LP of DEA2 releases a negative pulse to the RP of DEA, kicking DEA right. DEA has a 150 us delay for KB to rise and while DEA is right the Input Recovery Circuit functions as shown on plate 13 . After 150 us DEA returns left and the LP of DEA goes low to the RC of DP1. This starts a cycle of Decimal Registration as shown on plate 4. This is the S'r Decimal because the S'r KB is raised. The decimal value will be the True value at this time because DAM and DEM are conducting on the left so the DBT line is low and the DBC line is high.

A negative pulse to the RC of DA1-16 from the RP of DIC signifies completion of a Decimal Registration. The RP of DA1-16 sends a positive pulse to the LC of the open Gate DPG2. The LP of DPG2 releases a negative pulse to the RC and LC of DAX to trigger DAX right. The RP of DAX goes low to the RC of DAS pulling DAS right. The LP of DAS goes high to the LP of diode SI-2. The K-SI-2 goes high to the LD of SMC to start the Shift Operation for decimal alignment as shown on plate 4.

Decimal alignment is achieved when the Decimal Counter reaches 22 and DCC goes right. The RP of DCC goes low to the LC of DAS returning DAS left. The LP of DAS going low stops the Shift Operation. The RP of DAS going high pulses the RC and LC of Gate DG. The RI of DG is high because EPP is left. The RP of DG releases a negative pulse to the RP of DAM pulling DAM right. The LP of DAM goes high to the LI of DEM. The RP of DEM going low to the LI of DBC lowers the K-DBC. The LP of DEM going high to the LI of DBT raises the K-DBT (Decimal Counter is conditioned for a Decimal Complement

Registration). The LP of DEM also goes high to the RC of DEA1. The RP of DEA1 releases a negative pulse to the RP of DEA, kicking DEA right. DEA has a 150 us delay, though not needed at this time, and also causes the KB Recovery to function. After 150 us DEA returns left and the LP of DEA goes low to the RC of DP1. This starts a cycle of Decimal Registration as shown on plate 4. This is the S'r Decimal because the S'r KB is still raised. The decimal value will be the Complement value as explained above.

A negative pulse to the RC of DA1-16 from the RP of DIC signifies completion of a Decimal Registration. The RP of DA1-16 sends a positive pulse to the LC of the open Gate DPG2. The LP of DPG2 releases a negative pulse to the RC and LC of DAX. Since DAX was right this negative pulse will return DAX left. This same negative pulse to the LC of DAM returns DAM left. The LP of DAM returns low to bring DEM left and to the RC of DRB, triggering DRB right.

The RP of DRB goes low to the RI of PSAC to unclamp Sign Bias and start a cycle of RIG as shown on plates 43 and 5. The completion of a Numerical Registration is signified by a CX Pulse. The CX Pulse to the LC of DRB returns DRB to the left. The RP of DRB returns high to lower SB and also to the LC of EPG. The LP of EPG releases a negative pulse onto the Control Ring. This Control Ring Pulse returns ES left. This Control Ring Pulse also causes the KB Recovery Circuit to function by kicking ØFD1 as shown on plate 37 . The Computer now proceeds into the Result to Storage Control Circuit Operation.

RESULT TO STORAGE

Plate 15C

This plate illustrates the controls required to perform the Result Storage functions. These functions are:

1. Storage True Decimal Registration.

2. Shift Operation to align the Subvisor Decimal with the Storage Decimal.

3. A Numerical Registration, Test RIG, of the value in Storage. If Storage is correctly cleared the value in Storage at this time is zero.

4. The value in Accumulators, 1A to 10A only, are placed in Storage.

5. 14 us Set Recovery Delay (EDPZ).

6. The 'A' section, M-D chassis, and CCT Triggers are Zeroized. (EPZ and EZB2).

This circuit is employed in every Process.

Operation

Trigger ES is returned left by a Control Ring Pulse and the RP of ES goes high to the RC and LC of Gate MC1. The condition of MC1, in + or - process, is controlled by the condition of Trigger PAC. The control of PAC is shown on plate 20. If PAC is right then the left side of MC1 is open for Complementize. If PAC is left, as this circuit assumes, then the right side of MC1 is open. A negative pulse from the RP of MC1 triggers ER to the right. The RP of ER goes low to the LC of EBS, (-) Branch Trigger. This is the only means by which EBS is Zeroized. This method is necessary because use of the PTP prevents EBS being Zeroized by B2 or B5. The LP of ER goes high to the LI of ERA. The LP of ERA goes low to the LI of ERK. The K-ERK goes low to all ERF stages and the ERF stage with the high input has its plate lowered to pull down the R position on the Plugboard. R going low is plugged to a Storage KB Call. This lowers the input to an FA stage as shown on plate 10.

The LD of ERA taps off high to the LD of DRP. The LP of DRP goes high to the RI of DMG, to open this Gate, and high to the RC of DPG1. The RP of DPG1 releases a negative pulse to the RP of DEA, kicking DEA right. DEA has a 150 us delay for KB to rise and while DEA is right the Input Recovery Circuit functions as shown on plate 13. After 150 us DEA returns left and the LP of DEA goes low to the RC of DP1. This starts a cycle of Decimal Registration as shown on plate 4. This is the Result Decimal because the Result or Storage KB is raised. The decimal value will be the True value because the DBT cathode line is low as conditioned during the ES operation.

A negative pulse to the RC of DA1-16 from the RP of DIC signifies completion of a Decimal Registration. The RP of DA1-16 sends a positive pulse to the RC of the open Gate DMG. The RP of DMG releases a negative pulse to the RP of DRS triggering DRS right. The LP of DRS goes high to the RP of diode SI-2. The K-SI2 goes high to the LD of SMC to start the Shift Operation for decimal alignment as shown on plate 4.

Decimal alignment is achieved when the Decimal Counter reaches 22 and DCC goes right. The RP of DCC goes low to the LC of DRS returning DRS left. The LP of DRS going low stops the Shift Operation. The LP of DRS also goes low to the RC of MST, triggering MST right. The RP of MST goes low to the LI of MSI. The plates of MSI are tied together so both inputs of MSI must be low in order for the plates of MSI to go high. The RI of MSI is controlled by the LP of EMZ. EMZ is a Flip Flop of 5MS delay which was kicked by the return of EZB5, plate 11 . The purpose of EMZ delay is to delay the Test RIG Operation until the Storage Clear Operation is completed. When EMZ returns left the LP of EMZ goes low to the RI of MSI so now both sides of MSI are cutoff. The plates of MSI are free to go high. The high from MSI raises the LI of MSA. The LP of MSA goes low to the RC of MZT, triggering MZT right. The LP of MZT goes high to the LI of MZR. The LP of MZR goes low to the LI of PABA to raise the Add Bias and call for the Test RIG as shown on plate 43.

The completion of a Numerical Registration is signified by a CX Pulse. The CX Pulse to the LC of MZT returns MZT left. The LP of MZT going low lowers SB.

The LP of MZT goes low to the RC of MS, kicking MS right. MS is a 150 us delay Flip Flop which originates the Storage Set Signal. The RP of MS goes low to the LI of MSK. The K-MSK goes low to the LC of MSKA as shown on plate 10 . The result, in Accumulators 1A-10A, is now placed in Storage. The LP of MS goes high to the LC of EBG to check for (-) Branching as shown on plate 38.

After 150 us, MS returns left to complete the Storage Set Pulse. The RP of MS returns high to the RC of DPG2. The RP of DPG2 releases a negative pulse onto the Control Ring and ER is returned left. This is a Control Ring Pulse so the KB Recovery Circuit again functions as shown on plate 37.

The LP of ER returns low to the RC of EDPZ. EDPZ is a 14 us delay to allow the Storage Set Lines time to recover.

After 14 us, EDPZ returns left. The LP of EDPZ returns low to the RC of EPZ, kicking EPZ right. EPZ is a 450 us delay to allow sufficient time for the B2 Zeroize. The LP of EPZ goes high to the RC of EZG. The RP of EZG releases a negative pulse to trigger EZB2 right. The RP of EZB2 goes low to initiate the B2 Zeroize as shown on plate 36. EZB2 has a 300 us delay.

After 450 us, EPZ returns left. The LP of EPZ returns low to the RC of EPM, triggering EPM right. The Computer now proceeds into the Proof Minidend Control Circuit Operation.

PROOF MINIDEND - STORAGE REGISTRATION

Plate 16C

This plate illustrates the controls required to perform the Proof Minidend functions which are:

1. Proof Minidend (Storage) Decimal Complement Registration.

2. Proof Minidend (Storage) Numerical Registration.

This circuit is employed in every Process. The control circuits from this circuit through and including Zero Check are employed for proof purposes only. The answer for the step has been calculated and placed in Storage. The following sequence of control circuits are an automatic check on the calculation.

Operation

Flip Flop EPZ returning left goes low to the RC of EPM, triggering EPM right. The RP of EPM goes low to the diode ENM1 to check for Minus Factor as shown on plate 20.

The LP of EPM goes high to the RI of ERA. The RP of ERA goes low to the LI of ERK. The K-ERK goes low to all ERF stages and the ERF stage with the high input has its plate lowered to pull down the R position on the Plugboard. R going low is plugged to a Storage KB Call. This lowers the input to a FA stage as shown on plate 10.

The LP of EPM goes high to the LI of EPMA. The LP of EPMA goes low to the RP of DMP. The LP of DMP goes high to the following:

1. LP of diode EIA3 raising its left cathode to prepare SB.

2. LI of Gate DMG to condition this Gate open for future use.

3. LI of DMD lowering the LP of DMD.

The LP of DMD goes low to the RP of DEM, pulling DEM right. The RP of DEM goes low to the LI of DBC conditioning the Decimal Complement Gates in the Decimal Counter as shown on plate 4. The LP of DEM goes high to the RC of DEA1. The RP of DEA1 releases a negative pulse to the RP of DEA, kicking DEA right. DEA has a 150 us delay for KB to rise and while DEA is right the Input Recovery Circuit functions as shown on plate 13. After 150 us DEA returns left and the LP of DEA goes low to the RC of DP1. This starts a cycle of Decimal Registration as shown on plate 4. This is the Storage Decimal because the Storage KB is raised at this time. The decimal value will be the Complement as explained above.

A negative pulse to the RC of DA1-16 from the RP of DIC signifies completion of Decimal Registration. The RP of DA1-16 sends a positive pulse to the LC of the open Gate DMG. The LP of DMG releases a negative pulse to the RP of DRB, triggering DRB right.

The RP of DRB goes low to the RI of PSAC to unclamp SB and start a cycle of RIG as shown on plates 43 and 5. The Add Bias will always be raised at this time. The

completion of a Numerical Registration is signified by a CX Pulse. The CX Pulse to the LC of DRB returns DRB to the left. The RP of DRB returns high to lower SB and also high to the LC of EPG. The LP of EPG releases a negative pulse to the Control Ring. This Control Ring Pulse returns EPM left. This Control Ring Pulse also causes the KB Recovery Circuit to function by kicking ØFD1 as shown on plate 37 . The Computer now proceeds into the Proof Subvisor Control Circuit Operation.

PROOF SUBVISOR - SUBVISOR REGISTRATION

Plate 17C

This plate illustrates the controls required to perform the Proof Subvisor (Subvisor) functions in Addition or Subtraction. These functions are:

1. Proof Subvisor (Subvisor) True Decimal Registration.
2. Shift Operation to align the Proof M'd Decimal with the Proof S'r Decimal.
3. Proof Subvisor (Subvisor) Decimal Complement Registration.
4. Depending upon the Process the Proof S'r is either added or subtracted.

Operation

Trigger EPM is returned left by a Control Ring Pulse and the LP of EPM going low to the RC of EPS triggers EPS right.

The circuit operation is identical to the Subvisor Registration on plate 14. There are only two exceptions which are:

1. The right side of ESA is used.
2. The Check Counter is not opened to shifts because the right side of ESA is used.

The Control Ring Pulse from the LP of EPG returns EPS left. This Control Ring Pulse also causes the KB Recovery Circuit to function by kicking ØFD1 as shown on plate 37. The Computer now proceeds into the Minidend Subtraction Control Circuit Operation.

MINIDEND SUBTRACTION

Plate 18C

This plate illustrates the controls required to perform Minidend Subtraction functions in the various Processes. The functions are as follows:

1. Minidend True Decimal Registration.

2. Shift Operation to align the Proof S'r Decimal with the M'd Decimal.

   NOTE: In x or ÷ Process the Shift Pulses are also counted in the Check Counter.

3. The Minidend Numerical Registration is made, generally subtraction.

   NOTE: In x or ÷ Process a Carry Block is established between Accumulators 1M and 2M. In + or - process if Trigger PAC is right a one is added in Accumulator 1M.

Operation

Trigger EPS is returned left by a Control Ring Pulse and the LP of EPS going low to the RC of EPP triggers EPP right. The LP of EPP goes high to the LI of ECB1. The LD of ECB1 taps off high to the RD of EMA. The RP of EMA goes low to the LI of EMK. The K-EMK goes low to all EMF stages, as shown on plate 38, and lowers the V1 position on the Plugboard. V1 being lowered raises KB for the M'd. KB conditions Input Decoder Gates, Decimal Gates and checks for Minus Indication.

The RP of EPP goes low to the RI of ECB1. The RP of ECB1 goes high to the following:

1. LI of Gate DG to open this Gate for future use.

2. Plates of diode EPPM to raise its cathodes to prepare SB and open Gate DPG2 for future use.

3. The RC of MSA.

The RP of MSA releases a negative pulse to the RP of DEA, kicking DEA right. DEA has a 150 us delay for KB to rise and while DEA is right the Input Recovery Circuit functions as shown on plate 13. After 150 us DEA returns left and the LP of DEA goes low to the RC of DP1. This starts a cycle of Decimal Registration as shown on plate 4. This is the M'd Decimal because the M'd KB is raised. The decimal value will be the True value because the DBT cathode will be low as conditioned during the EPS operation.

A negative pulse to the RC of DA1-16 from the RP of DIC signifies completion of a Decimal Registration. The RP of DA1-16 sends a positive pulse to the LC of the open

Gate DPG2. The LP of DPG2 releases a negative pulse to the RC and LC points of Trigger DAX to kick DAX right. The RP of DAX goes low to the RC of DAS pulling DAS right. The LP of DAS goes high to the LP of diode SI-2. The K-SI-2 goes high to the LD of SMC to start the Shift Operation for decimal alignment as shown on plate 4.

NOTE: In X or ÷ Process only, the Check Counter is opened to count shifts as shown on plate 41 . The X or ÷ Process from the LD of PPI goes low to the RD of CPMD. This cuts off the RP of CPMD. The RP of EPP is low to the RI of ECB1. The LD of ECB1 taps off low to the LD of EMZ'. The LP of EMZ' is cut off. The LP of EMZ' and RP of CPMD are free to go high to the LI of CPMD. The LP of CPMD goes low to the LI of CGA. The LP of CGA is cut off. CT10 and CT11 are both always left at this time. The RP of CT11 is high to the RD of DCK2. The RP of DCK2 is low to the RI of CCM. The RP of CCM is cut off. The LP of CGA and RP of CCM are free to go high to the LI of CTSG, opening this Gate. The Shift Pulses occurring during EPP in X or ÷ Process will pass through the open CTSG Gate and accumulate in the CCT.

Decimal alignment is achieved when the Decimal Counter reaches 22 and DCC goes right. The RP of DCC goes low to the LC of DAS returning DAS left. The LP of DAS going low stops the Shift Operation. The RP of DAS going high pulses the RC and LC of Gate DG. The LI of DG is high since EPP is right. The LP of DG releases a negative pulse to the RP of DRB, pulling DRB right.

The RP of DRB goes low to the RI of PSAC to raise SB and call for a cycle of RIG as shown on plates 43 and 5.

NOTE: In + or - Process PAC may be right. PAC would go right if an overcarry at 11A or 11M occurs during EPS Control Circuit time. Whenever this overcarry occurs, legitimately, the Add Bias will be raised during EPP Numerical Registration. The RP of PAC being low cuts off the left side of CØDE. The right side of CØDE is cut off from the low level off the RD of ECB1. The plates of CØDE are free to go high to the RP of diode C9R. This raises the right cathode of diode C9R and raises the LI of Gate I1-11. The RIG1' Pulse occurring during the EPP Numerical Registration passes through this open I1-11 Gate to put a negative pulse on the 1M Odd Line. The M Section would be all nines so a series of overcarries would result leaving the A Section zero and a 1 in the Accumulator 1M when all carries are satisfied.

In X or ÷ Process the LP of EMZ and RP of CPMD are free to go high as previously shown. The LI of CPMD goes high and the LD of CPMD taps off high to the LD of ECB2. The LP tap point, pin 8, goes low to the left bias of Accumulator 1M AC stage. This blocks carries from Accumulator 1M to 2M.

The completion of a Numerical Registration is signified by a CX Pulse. The CX Pulse to the LC of DRB returns DRB to the left. The RP of DRB returns high to lower SB and also high to the LC of EPG. The LP of EPG releases a negative pulse to the Control Ring. This Control Ring Pulse returns EPP to the left. At this time the Accumulators

1A to 10A must be zero in + or - and may be zero or all nines in x or ÷ in order to be able to prove a good calculation. This check is indicated in the Zero Check. Zero Check is the next control circuit operation.

ZERO CHECK

Plate 19C

This plate illustrates the controls required, in all processes, to determine if a calculation has been successfully performed. Addition and Subtraction controls vary, somewhat, from the Multiplication and Division controls.

I Addition and Subtraction

A. Zero Check (1A-10A)

B. 10 Shifts

C. Zero Check (1A-10A)

D. EGD (Step Advance and Step Zeroize)

NOTE: If either Zero Check is unsuccessful the Computer does not continue until that step has been repeated and successful Zero Checks made.

II Multiplication and Division

A. Shift to bring CCT to count of 10 (if necessary)

B. Zero Check

1. Successful

a. EGD

2. Unsuccessful

a. Adds a one to Accumulator 1A.

b. Zero Check

(1) Successful

(a) EGD

(2) Unsuccessful

(b) Computer cannot continue. Step repeat.

Zero Check Control Operation

Each IO Chassis has an Output Decoder Section and it is from this section that the Zero or non-zero indication is derived. Each Accumulator, 1A through 10A, has its TØ and T1 Trigger indication fed to the Output Decoder. When T1 is left and TØ right the Accumulator is at zero.

Trigger T1 being left is low to M0 and the K-M0 is low to the K-MA9. Trigger TØ being right is high to MA9. MA9 now has a high grid and low cathode so the LP of MA9 is free to conduct and lower the right grid of MØCC. The above control is present in each I0 Chassis. The right cathodes of the MØCC stage of each I0 Chassis are tied together. When all 10 I0 Chassis are zero this cathode line is low but any one I0 Chassis decoding a value will raise this cathode line.

The right cathodes of all MØCC stages, Zero Check (1A-10A), are fed low to the LI of Ø9C. Ø9C and Ø9C1 are in parallel so both stages are cutoff. The plates of Ø9C and Ø9C1 go high to the LI of Ø9M. The LP of Ø9M is low to the LI of Ø9SM and Ø9SM1. The left sides of Ø9SM and Ø9SM1 are cutoff. The right sides of Ø9SM and Ø9SM1 are also cutoff by the low level from the LP of PAT. (PAT is the Sign Check Trigger used in x or ÷. See plate 20). The plates of Ø9SM and Ø9SM1 are free to go high. This is always the case when a true Zero Check occurs. Whenever a Zero Check occurs the high level from the plates of Ø9SM and Ø9SM1 will open the following Gates:

1. CØPG - left side
2. C9G - left side
3. CØG - right side

Regardless of the process the preceding controls and operations are the same.

Addition and Subtraction Zero Check Operation

This explanation is given with the assumption a Zero Check occurs.

Trigger EPP is returned left by a Control Ring Pulse. The LP of EPP returns low to the RC of CØD. CØD goes right for 100 us. The purpose of this 100 us delay is to allow time for the Zero Check lines to stabilize. After 100 us CØD returns left. The RP of CØD goes high to the RC and LC of Gate CØPG. The right side of CØPG is closed by x and ÷ Process. The left side of CØPG is opened by Zero Check. The LP of CØPG releases a negative pulse to the RC and LC of the Diode Gate CØDG. Gate CØDG is controlled by the condition of CT10 in the Check Counter.

NOTE: The count in the Check Counter at this time is always zero in a + or - Process. CT10 is left so the LP of CT10 is low to RI of CGA. The RP of CGA is high to the LI of CØDD and RI of CØDG. The LP of CØDD is low to the LI of CØDG. The left side of CØDG is open and the right side closed.

The LP of CØDG releases a negative pulse to the RD of CØCS, triggering CØCS right. The LP of CØCS goes high to the LP of diode ENM1. The left cathode of ENM1 raises the LD of SMC to start a Shift Operation.

NOTE: The purpose of this Shift Operation is to shift exactly 10 times. These 10 shifts bring the values of Accumulators 2M to 11M into Accumulators 1A to 10A. The values are zero when the step is correct. The Decimal Counter is of no value to indicate a total of 10 so the Check Counter and Trigger CT10 is employed.

The RP of CØCS goes low to the RI of CØDD. The RP of CØDD goes high to the RI of CTSG to open the Gate. This Gate is pulsed by Shift Pulses and the output of the Gate goes to CT1 which is part of the Check Counter. The Check Counter counts each Shift Pulse. At the 10th Shift Pulse CT10 is pulled right. The LP of CT10 goes high to the RI of CGA. The RP of CGA goes low to the LC of CØCS, triggering CØCS left. CØCS returning left stops the Shift Operation and closes Gate CTSG. Exactly 10 shifts have occurred.

The LP of CØCS returns low to the RC of CØDA, kicking CØDA right. CØDA has a 100 us delay to allow the Zero Check lines to stabilize. After 100 us CØDA returns left. The LP of CØDA goes low to the RC of C9G. The RP of C9G releases a positive pulse to the RC and LC of CØG. The left side of CØG is closed by x and ÷ Process. The right side of CØG is opened by Zero Check. The RP of CØG releases a negative pulse to the RP of EGD. EGD being pulsed advances the Computer into the next Program Step (as shown on plate 11 .)

In Addition or Subtraction both Zero Checks must be present in order for the circuits to continue functioning. Lack of either Zero Check will cease circuit operation until a repeat signal is given from the Timer Circuit.

Multiplication and Division Zero Check Operation

Trigger EPP is returned left by a Control Ring Pulse. The LP of EPP returns low to the RC of CØD. CØD goes right for 100 us. The purpose of this 100 us delay is to allow time for the Zero Check lines to stabilize. After 100 us CØD returns left. The RP of CØD goes high to the RC and LC of Gate CØDG.

NOTE: Both sides of CØPG are open. The left side is opened by Zero Check. The right side is opened by x or ÷ Process. The x or ÷ Process Line is low to the RD of ERAZ. The RP of ERAZ is high to the RI of CØPG opening the Gate. In this particular example both sides are open but only the right side is always open in x or ÷ Process.

The plates of CØPG release a negative pulse to the RC and LC of the Diode Gate CØDG.

NOTE: The Diode Gate CØDG is conditioned on both sides by the Check Counter Trigger CT10. If CT10 is left the left side of CØDG is open and if CT10 is right the right side of CØDG is open as shown on plate 19. The CCT is opened to count shifts during EPP in x or ÷ only. As shown on the problem sheet, the Proof Result always has its first digit in 11 M when shifting starts during EPP. The number of shifts required during EPP can vary from zero (22) up to a total of 10. The object of this proof system is to have the Proof Result shifted a total of 10 times before a Zero Check is attempted. This total of 10 is indicated when CT10 goes right. If CT10 is right, the total of 10 shifts has occurred so the right side of CØDG being open pulses CØDA directly. The following is an explanation assuming CT10 is still to be left.

The left side of the Diode Gate CØDG is open so the LP of CØDG releases a negative pulse to the RD of CØCS, triggering CØCS right. The LP of CØCS goes high to the LP of diode ENM1. The left cathode of ENM1 raises the LD of SMC to start a Shift

Operation.

NOTE: This time the CCT may have some count already present so the number of shifts required will vary depending upon the M'd value and M'd decimal position.

The RP of CØCS goes low to the RI of CØDD. The RP of CØDD goes high to the RI of the Gate CTSG. This open Gate, CTSG, passes the Shift Pulses into the CCT. A count of 10 in the CCT is indicated by CT10 going right. The LP of CT10 goes high to the RI of CGA. The RP of CGA goes low to the LC of CØCS, triggering CØCS left. CØCS returning left stops the Shift Operation and closes Gate CTSG.

The LP of CØCS returns low to the RC of CØDA, kicking CØDA right. CØDA has a 100 us delay to allow the Zero Check lines to stabilize. After 100 us, CØCS returns left. The LP of CØDA goes low to the RC of C9G. The RP of C9G releases a positive pulse to the RC and LC of Gate CØG.

Up to this point the circuitry has made no definite attempt to differentiate because of lack of a Zero Check. At Gate CØG this attempt is made.

First, assume the 1A-10A Accumulators are zero and the right side of CØG is open. The left side of CØG is also opened by the X or ÷ Process. The negative pulse released from the RP of CØG kicks EGD to bring about Step Advance and Step Zeroize. The EGD operation will nullify any operations begun by a pulse from the LP of CØG.

Secondly, assume the A Section does not indicate all zeros. The right side of CØG is closed so EGD cannot be pulsed. The negative pulse released from the LP of CØG is effective and kicks C9T right. The LP of C9T goes high and the following results occur:

1. A neon in SK2 is fired to raise the RD of DCCL and lower the cathode of CX as shown on plate 48. This will nullify the KB Detector Circuit. C9T does not raise a KB so a false KB, via SK2 is required to open CX.

2. The grids of EØCB are raised so both plates of EØCB conduct. The LP of EØCB lowers the left bias of Accumulator 1M AC stage to prevent Carry Out to Accumulator 2M. The RP of EØCB lowers the LI of PABA to raise Add Bias and call for a cycle of RIG.

3. The left bias of EØCB taps off high to the LD of EØCA to open the Gate. The RIG1' Pulse from the cycle of RIG goes through this open Gate to put a negative pulse on the 1A Odd Line.

Assuming the A Section to be all nines the negative pulse to Accumulator 1A will bring these nines to zero. The completion of a Numerical Registration is signified by a CX Pulse. The CX Pulse to the RC of C9D pulls C9D right. C9D has a 100 us delay to allow the Zero Check lines to stabilize.

After 100 us C9D returns left, the LP of C9D goes low to the LC of C9T, triggering C9T left. The RP of C9T returns high to the LC of Gate C9G. The LI of C9G is controlled by the Zero Check Line. Assuming Accumulators 1A-10A to be zero this Gate is open. The LP of C9G releases a negative pulse to the RP of EGD. EGD being pulsed advances the Computer into the next Program Step as shown on plate 11.

In the event Gate C9G has been closed because of a Non-Zero Check the circuit operation would cease until a repeat signal occurs from the Timer Circuit.

COMPLEMENTIZE

Plate 20C

Complementize is the term employed, in an Addition or Subtraction Process, when the numerical result is negative. The actual value, not the complement, must be placed in Storage. Whenever the answer is negative, because of a subtraction, the normal Computer operation gives a complement answer. A subtraction is the difference between two numbers. For example: 8-5 = 3 or 5-8 = -3. The difference between the two subtractions is the sign of the answer. In Complementize this fact is used so that when an answer is negative the signs of the two numbers are reversed giving a true value instead of a complement value. The negative sign of the answer is retained to go with the true value.

Operation

The operation of this circuit covers the entire control circuit time from EM to EPP. To assist in tracing this circuit the Work Sheet problem will be used as a typical example of the circuit operation.

Line 1

Calculator Zeroize - All Triggers on this circuit are Zeroized left.

Line 2

Minidend Decimal Complement - At this time EM is right so the LP-EM is high to the LI-EMA. The LP-EMA goes low through the diode ENM to pull PAMD right. PAMD is a 250 us delay for KB to rise.

KB conditions the Minus Neon Common Line low (no negative value). MC4 is cut off because of this low line. The LP-MC4 is high to LI-MC5 so the plates of MC5 are low to the RP-MCX. The RP-MC4 is tied to the LP-MC6. MC6 has a low plate since the RP of MC2 is high to the LI of MC6. This holds the LP-MCX low. Both plates of diode MCX are low so the cathodes of MCX are low to Gate PSIG, holding this Gate closed. After 250 us PAMD returns left sending its RP high to the LC of the closed Gate PSIG. PSIG being closed stops the circuit operation at this point.

Line 3

Minidend Numeric Registration - This registration has no function in this circuit at this time.

Line 4

Subvisor Decimal - This operation is the same as line 2 except ES and ESA are used instead of EM and EMA. The subvisor is a positive number even though it is to be subtracted (Subtract Process).

Line 5

Minidend Shifted until the Decimal Counter reaches 22 - This Shift

Operation requires 21 shifts, according to the work sheet. The first 16 of these shifts are counted in the Check Counter (see plate 41). These shifts will cause CT11 to go right. CT11 controls the conditioning of Gate PSOC. CT11 will be right, and will open the left side of PSOC and close the right side of PSOC.

Line 6

Subvisor Decimal Complement - This operation has no function in this circuit.

Line 7

Subvisor Numeric Registration - The Subvisor value is larger than the Minidend Value so when the subtraction takes place a series of overcarries will occur. Accumulator 11A goes into overcarry and when the TC Trigger in 11A is returned left the RP-AC returns high to the LI of PS11. The RP-PS11 returns low to the RC and RI points of P11C. The RP of P11C releases a positive pulse to pin 6 and out pin 5 to the LC of PSOC. This Gate was previously conditioned open. The LP-PSOC releases a negative pulse to the RC and LC of PAC, triggering PAC right. PAC going right closes the right side of MC1 and opens the left side of MC1.

The overcarries continue around to Accumulator 11M. The TC Trigger in 11M goes right and the RP-AC goes low to the LI of C11M. The RP-C11M goes high to the RC of PSOC. The right side of PSOC was previously conditioned closed (CT11 is right).

The S'r Numerical Registration is completed (CX Pulse) and a Control Ring Pulse is released. The Control Ring Pulse returns ES left. The RP-ES returns high to the RC and LC of Gate MC1. As previously stated, the left side of MC1 is open (PAC right). The LP-MC1 releases a negative pulse to the RP of MC2, triggering MC2 right.

Line 8

Calculator Zeroize - MC2 goes right and the LP-MC2 goes high to the RC of MC6. The RP-MC6 releases a negative pulse to the RP of EZ. When EZ is pulsed the step is started over and all Triggers, except MC2, in this circuit are Zeroized left.

Line 9

Minidend Decimal Complement - As stated under line 2 PAMD is pulsed right for 250 us. The Minus Neon Common Line is still low which holds the RP of MC4 cutoff. MC2 being on the right holds the LP of MC6 cutoff. The high from the RP-MC4 and LP-MC6 raises the LP of diode MCX. The cathodes of MCX go high to the LI of PSIG and open this Gate.

After 250 us PAMD returns left and the RP-PAMD goes high to the LC of the open Gate PSIG. The LP-PSIG releases a negative pulse to the RC-PSIG. The RP-PSIG releases a positive pulse to the RC and LC of Gate PS.

NOTE: The Process is Subtraction so the RK-PIAS is low. The RP-PIAS is low to the RI-PPI. The RP-PPI is high to the LI-PS opening this side of the Gate. The right side of PS is closed because of no x or ÷ Process

The LP-PS releases a negative pulse to the RC of PAM, triggering PAM right. PAM being on the right will reverse the normal SB procedure as shown on plate 44.

Line 10

Minidend Numeric Registration - The M'd is normally added but because PAM is right, as explained under line 9, the Subtract Bias will be raised. The Accumulators were zero so when the M'd was subtracted a series of overcarries will occur. Accumulator 11A goes into overcarry and when the TC Trigger in 11A is returned left the RP-TC returns high to the LI of PS11. The RP-PS11 returns low to the RC, RI points of P11C. The RP-P11C releases a positive pulse to pin 6 and out pin 5 to the LC of PSOC. The Gate is closed.

NOTE: CT11 was Zeroized left on line 8. This opens the right side of PSOC and closes the left side.

The overcarries continue around to Accumulator 11M. The TC Trigger in 11M goes right and the RP-TC goes low to the LI of C11M. The RP-C11M goes high to the RC of PSOC. This side of the Gate is open so the RP-PSOC releases a negative pulse to the RC and LC of PAC, triggering PAC right.

The M'd Numerical Registration is completed (CX Pulse) leaving the M'd complement value in the Accumulators. DRB returns left to kick PDAM right for 25 us. PDAM returns left sending its LP low to return PAM left.

Line 11

Subvisor Decimal - This operation is the same as line 9. PAM again will be triggered right.

Line 12

Minidend Shifted until the Decimal Counter reaches 22 - This operation is the same as line 5. CT11 again will be triggered right.

Line 13

Subvisor Decimal Complement - This operation has no function in this circuit.

Line 14

Subvisor Numerical Registration - The S'r value is larger than the M'd value so when the addition takes place (PAM is right) another series of overcarries will occur. Accumulator 11A goes into overcarry and when the TC Trigger in 11A is returned left the RP-TC returns high to the LI of PS11. The RP-PS11 returns low the RI, RC points of P11C. The RP of P11C releases a positive pulse to pin 6 and out pin 5 to the LC of PSOC. This Gate was conditioned open on line 12 when CT11 went right. The LP-PSOC releases a negative pulse to the RC and LC of PAC,

triggering PAC back left (went right on line 10). PAC returning left opens the right side of MC1 and closes the left side of MC1.

The overcarries continue around to Accumulator 11M. The TC Trigger in 11M goes right and the RP-TC goes low to the LI of C11M. The RP-C11M goes high to the RC of PSOC. The right side of PSOC was previously conditioned closed (CT11 is right).

The S'r Numerical Registration is completed (CX Pulse) and a Control Ring Pulse is released. At this same time DRB kicks PDAM right for 25 us. PDAM, on its return, goes low to the LC of PAM returning PAM left. The Control Ring Pulse returns ES left. The RP-ES returns high to the RC and LC of Gate MC1. As previously stated, the right side of MC1 is open (PAC is left). The RP-MC1 releases a negative pulse to the RP of ER, triggering ER right.

Line 15

Storage Decimal - This operation has no function in this circuit.

Line 16

Result is shifted until the Decimal Counter reaches 22 - This operation has no function in this circuit.

Line 17

Test RIG - This operation has no function in this circuit.

Line 18

Result is placed in Storage - The numerical value has been aligned with the Storage Decimal and is held in the Accumulators ready to be set in Storage. Flip Flop MS goes right to set Storage. The value is correct in the Accumulators but a negative sign must accompany this value. MC2 is right and the RP-MC2 is low to the LI-MC6. The LD of MC6 goes low to the RD of MC7. The RP of MC7 is cutoff but is connected to the LP of ØC2 which must also be cutoff in order for this line to be free to go high. The result has a numerical value so the Zero Check lines to the grids of Ø9C will be high. The plates of Ø9C are low to the LI of Ø9M, tapping off low to the LD of ØC2. ØC2 is cutoff so the LP-ØC2 and RP-MC7 are free to go high to the LI of MC8. The LP-MC8 goes low to the LI of SSRO to condition firing the Minus Bit as shown on plate 46. The LP-MC8 also goes low to the LI of MC7. The LP-MC7 goes high to open the Minus Branch Gate EBG as shown on plate 38.

NOTE: In the event the result, in the A Section, is zero at this time, both Minus Branching and conditioning the Minus Bit would be defeated. Any zero answer will always be a positive indication.

Line 19

B-2 Zeroize - This operation has no function in this circuit.

NOTE: CT11 is <u>not</u> B-2 Zeroized.

Line 20

Proof Minidend Decimal Complement - This operation is the same as line 9 except EPM and ENM1 are employed to kick PAMD. PAM is again triggered right.

Line 21

Proof Minidend Numerical Registration - The result is a negative value but PAM is left so the Add Bias will be raised and the Result value added into the Accumulators. When the cycle of RIG is completed (CX Pulse) DRB returns left to kick PDAM. PDAM returns left after 25 us to return PAM left.

Line 22

Proof Subvisor Decimal - Same as line 11.

Line 23

Proof Minidend shifted until the Decimal Counter reaches 22 - This operation has no function in this circuit.

Line 24

Proof Subvisor Decimal Complement - Same as line 13.

Line 25

Proof Subvisor Numerical Registration - The Proof Subvisor value will be subtracted since PAM is on the right. The Proof S'r value is larger than the Result value so a series of overcarries will result. Accumulator 11A goes into overcarry and when the TC Trigger in 11A is returned left the RP-TC returns high to the LI of PS11. The RP-PS11 returns low to the RI, RC points of P11C. The RP-P11C releases a positive pulse to pin 6 and out pin 5, to the LC of PSOC. This Gate was conditioned open on line 12 when CT11 went right. The LP-PSOC releases a negative pulse to the RC and LC of PAC, triggering PAC right.

The overcarries continue around to Accumulator 11M. The TC Trigger in 11M goes right and the RP-TC goes low to the LI of C11M. The RP-C11M goes high to the RC of PSOC. The right side of PSOC was previously conditioned closed (CT11 is right).

The completion of the Proof S'r Numerical Registration (CX Pulse) returns DRB left to kick PDAM. After 25 us PDAM returns left to kick PAM back left.

Line 26

Minidend Decimal - This operation is the same as line 9 except EPP is used instead of EM.

Line 27

Proof Result Shifted until the Decimal Counter reaches 22 - This operation has no function in this circuit.

Line 28

Minidend Numerical Registration - This operation does not have a direct bearing on this circuit but some explanation will be given to show how the Accumulators become zero. As shown on plate 18 , the fact that PAC and EPP are both right, allows the RIG1' Pulse to be released onto the 1M Odd Line. 1M has a nine value so the addition of the one creates an overcarry. All other Accumulators are nines so this overcarry is extended to all other Accumulators. The carries are finally satisfied when 11A completes its carry-out to put a one in 1M. This enables the Accumulators to be zero when the Zero Check Operation is called for.

Line 29

Zero Check - This operation has no function in this circuit.

Line 30

Shift 10 - This operation has no function in this circuit.

Line 31

Zero Check - This operation has no function in this circuit.

PROCESS	M-SECTION CALC. DEC. REF. POINT											A-SECTION INPUT											COUNTER		
	11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	DEC	M-D	CCT
MINIDEND											12				1	1	1	1							
SUBVISOR											13					3	3	3	3						
STORAGE DECIMAL											16														
1. CALC. ZEROIZE																									
2. M'D DEC. COMPL.																							10		
3. M'D NUM. REG.															1	1	1	1					10		
4. S'R DECIMAL															1	1	1	1					1		
5. M'D SHIFTED DCR AT 22																1	1	1	1				22		
6. S'R DEC. COMPL.							PAC-R									1	1	1	1				9		CT11
7. S'R NUM. REG.	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	7	7	7	7	9	9	9	9		CT11
8. CALC. ZEROIZE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0
9. M'D DEC. COMPL.		PAC-R																					10		0
10. M'D NUM. REG.	9	9	9	9	9	9	9	9	9	9	9	9	9	9	8	8	8	8	9	9	9	9	10		0
11. S'R DECIMAL	9	9	9	9	9	9	9	9	9	9	9	9	9	9	8	8	8	8	9	9	9	9	1		0
12. M'D SHIFTED DCR AT 22	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	8	8	8	8	9	9	9	22		CT11
13. S'R DEC. COMPL.	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	8	8	8	8	9	9	9	9		CT11
14. S'R NUM. REG.								PAC-L								2	2	2	2				9		CT11
15. STOR. DECIMAL																2	2	2	2				3		CT11
16. RES. SHIFTED DCR AT 22																			2	2	2	2	22		CT11
17. TEST RIG																			2	2	2	2	22		CT11
18. RES. TO. STOR.																			2	2	2	2	22		CT11
19. B-2 ZEROIZE												0	0	0	0	0	0	0	0	0	0	0	22		CT11
20. PR. M'D. DEC. COMPL.																							6		CT11
21. PR. M'D NUM. REG.																			2	2	2	2	6		CT11
22. PR. S'R DECIMAL																			2	2	2	2	19		CT11
23. PR. M'D SHIFTED DCR AT 22																2	2	2	2				22		CT11
24. PR. S'R DEC. COMPL.							PAC-R									2	2	2	2				9		
25. PR. S'R NUM. REG.	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	8	8	8	8	9	9	9	9		CT11
26. M'D DECIMAL	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	8	8	8	8	9	9	9	21		CT11
27. PR. RES. SHIFTED DCR AT 22	9	9	9	9	9	9	9	9	9	9	9	9	9	9	8	8	8	8	9	9	9	9	22		CT11
28. M'D NUM. REG.											1				1	1	1	1					22		CT11
28. M'D NUM. REG.	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	22		CT11
29. ZERO CHECK											1												22		CT11
30. SHIFT 10	1																						10		CT10
31. ZERO CHECK	1																						10		CT10

MULTIPLICATION PROCESS

Work Sheet

This work sheet shows the procedure the Computer follows in order to multiply two numbers together, store the result and prove the answer. The procedure will be the same in any Multiplication Problem where both the multiplier and multiplicand are values other than zero. The only variations will occur in the numerical values and decimal position.

The problem used as an example has the following values:

Minidend	V1	-33.33	6/5 Decimal
Subvisor	V2	33.88	4/3 Decimal
Result	R		1/0 Decimal

CALCULATOR ZEROIZE

Plate 11C

Line 1

Calculator Zeroized - All Triggers are normalized including Accumulators, Counters and Control Triggers. Storage is Zeroized.

MINIDEND REGISTRATION

Plate 13C

Line 2

Minidend Decimal Complement is registered in the Decimal Counter.

Line 3

Minidend Numerical Registration is made (cycle of RIG). The M'd value is registered in the Accumulators.

MULTIPLICATION PROCESS CALL

Plate 22C

Line 4

Subvisor Decimal Complement is added in the Decimal Counter.

Line 5

The M-D Constant of 17 is added in the Decimal Counter.

MULTIPLICATION PROCESS

Plate 23C

Line 6

The Minidend is shifted until its first digit reaches Accumulator 11M. All shifts are counted in the Decimal Counter. Only the first 11 shifts are counted in the M-D Counter.

Line 7

First Subvisor Addition is made. The S'r Numerical Registration is made (cycle of RIG). A one is subtracted from the M'd digit in 11M.

Line 8 and 9

The Subvisor Additions continue until the digit in 11M reaches zero.

Line 10

Shift until a digit reaches 11M. This shift is counted in both the Decimal and M-D Counter.

Line 11, 12 and 13

The Subvisor is added until the digit in 11M reaches zero.

Line 14 to 21

Shifts occur until a digit reaches 11M. The S'r is added until 11M reaches zero. This operation of shifts and S'r Additions will continue until the M-D Counter reaches 22. Any number that reaches 11M after the M-D Counter reaches 22 must be a Result digit.

Line 22

Shift until a digit reaches 11M. By this time the M-D Counter has reached 22 so the digit that arrives in 11M must be a Result digit. This is the completion of Multiplication.

Line 23

B-2 Zeroize. The A Section and M-D Counter are Zeroized leaving a maximum of 11 Result digits.

RESULT TO STORAGE

Plate 15C

Line 24

The Storage Decimal is added in the Decimal Counter.

Line 25

The Result is shifted to align with the Storage Decimal. This alignment is indicated by the Decimal Counter reaching 22.

Line 26

Test RIG. A numerical registration (cycle of RIG) of Storage is made. This value is zero.

Line 27

Result to Storage. Any digits in Accumulators 1A to 10A will be set in Storage.

Line 28

B-2 Zeroize. Accumulators 1A-11A are Zeroized leaving the Result in Storage.

PROOF MINIDEND REGISTRATION

Plate 16C

Line 29

Proof Minidend Decimal Complement is registered in the Decimal Counter.

Line 30

Proof Minidend Numerical Registration is made (cycle of RIG). The Result value is added in the A Section.

DIVISION PROCESS CALL

Plate 24C

Line 31-96

See Division Work Sheet for this operation from line 4-61 for theory of operation.

MINIDEND SUBTRACTION

Plate 18C

Line 97

Minidend Decimal is added in the Decimal Counter.

Line 98

Proof Result is shifted to align with the M'd Decimal. This alignment is indicated by the Decimal Counter reaching 22. These shifts are also counted in the Check Counter.

Line 99

Minidend Numerical Registration is made (cycle of RIG). The value in the Accumulators is now zero in this problem. It is possible, in some problems, for the Accumulators to have a value of nines.

ZERO CHECK

Plate 19C

Line 100

A Shift Operation occurs to bring the count in the Check Counter to 10. In this particular problem 3 shifts are required. The number of shifts will vary from zero to ten depending upon the problem.

Line 101

A Zero Check is now made in Accumulators 1A to 10A. In this particular problem the Zero Check is successful. If the Zero Check is not successful, because of nines, a one is added to 1A to create a Zero Check condition.

PROCESS	M-SECTION CALC. DEC. REF. POINT											A-SECTION INPUT											COUNTER		
	11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	DEC	M-D	CCT
MINIDEND											11				-	3	3	3	3						
SUBVISOR											13							3	3	8	8				
STORAGE DECIMAL											16														
1. CALC. ZEROIZED																									
2. M'D DEC. COMPL.																							11		
3. M'D NUM. REG.																3	3	3	3				11		
4. S'R DEC COMPL.																3	3	3	3				20		
5. CONSTANT 17																3	3	3	3				15		
6. SHIFT 1st DIGIT IN 11M	3	3	3	3																			8	11	CT11
7. 1st S'R ADD	2	3	3	3														3	3	8	8		8	11	CT11
8. 2nd S'R ADD	1	3	3	3														6	7	7	6		8	11	CT11
9. 3rd S'R ADD	0	3	3	3													1	0	1	6	4		8	11	CT11
10. SHIFT-DIGIT IN 11M	3	3	3													1	0	1	6	4			9	12	CT11
11. 1st S'R ADD	2	3	3													1	0	5	0	2	8		9	12	CT11
12. 2nd S'R ADD	1	3	3													1	0	8	4	1	6		9	12	CT11
13. 3rd S'R ADD	0	3	3													1	1	1	8	0	4		9	12	CT11
14. SHIFT-DIGIT IN 11M	3	3													1	1	1	8	0	4			10	13	CT11
15. 1st S'R ADD	2	3													1	1	2	1	4	2	8		10	13	CT11
16. 2nd S'R ADD	1	3													1	1	2	4	8	1	6		10	13	CT11
17. 3rd S'R ADD	0	3													1	1	2	8	2	0	4		10	13	CT11
18. SHIFT-DIGIT IN 11M	3													1	1	2	8	2	0	4			11	14	CT11
19. 1st S'R ADD	2													1	1	2	8	5	4	2	8		11	14	CT11
20. 2nd S'R ADD	1													1	1	2	8	8	8	1	6		11	14	CT11
21. 3rd S'R ADD	0													1	1	2	9	2	2	0	4		11	14	CT11
22. SHIFT-DIGIT IN 11M	1	1	2	9	2	2	0	4															2	22	CT11
23. B-2 ZEROIZE	1	1	2	9	2	2	0	4															2	0	Ø
24. STOR. DECIMAL	1	1	2	9	2	2	0	4															18	0	
25. RES. SHIFT DCR AT 22	2	2	0	4															1	1	2	9	22		
26. TEST RIG	2	2	0	4															1	1	2	9	22		
27. RES. TO STOR.	2	2	0	4															1	1	2	9	22		
28. B-2 ZEROIZE	2	2	0	4								0	0	0	0	0	0	0	0	0	0	0	22		
29. PR. M'D DEC. COMPL.	2	2	0	4																			6		
30. PR. M'D NUM. REG.	2	2	0	4															1	1	2	9	6		
31. PR. S'R DECIMAL	2	2	0	4															1	1	2	9	19		
32. CONSTANT 17	2	2	0	4															1	1	2	9	14		

PROCESS	M-SECTION CALC. DEC. REF. POINT											A-SECTION INPUT											COUNTER		
	11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	DEC	M-D	CCT
MINIDEND											11				-	3	3	3	3						
SUBVISOR											13							3	3	8	8				
STORAGE DECIMAL											16														
33. SHIFT DIGIT IN 11M	1	1	2	9	2	2	0	4															10	12	
34. 1st PR. S'R TRIAL SUB'T.	1	1	2	9	2	2	0	4			2	9	9	9	9	9	9	6	6	1	2		10	12	
35. PR. S'R ADD BACK	1	1	2	9	2	2	0	4															10	12	
36. SHIFT 1 POSITION	1	2	9	2	2	0	4															1	11	12	
37. 1st PR. S'R TRIAL SUBT.	1	2	9	2	2	0	4				2	9	9	9	9	9	9	6	6	1	2	1	11	12	
38. PR. S'R ADD BACK	1	2	9	2	2	0	4															1	11	12	
39. SHIFT 1 POSITION	2	9	2	2	0	4															1	1	12	12	
40. 1st PR. S'R TRIAL SUB'T	2	9	2	2	0	4					2	9	9	9	9	9	9	6	6	1	3	1	12	12	
41. PR. S'R ADD BACK	2	9	2	2	0	4															1	1	12	12	
42. SHIFT 1 POSITION	9	2	2	0	4															1	1	2	13	12	
43. 1st PR. S'R TRIAL SUBT.	9	2	2	0	4						2	9	9	9	9	9	9	6	6	2	3	2	13	12	
44. PR. S'R ADD BACK	9	2	2	0	4															1	1	2	13	12	
45. SHIFT 1 POSITION	2	2	0	4															1	1	2	9	14	12	
46. 1st PR. S'R TRIAL SUB'T.	2	2	0	4							2	9	9	9	9	9	9	6	7	2	4	9	14	12	
47. PR. S'R ADD BACK	2	2	0	4															1	1	2	9	14	12	
48. SHIFT 1 POSITION	2	0	4															1	1	2	9	2	15	12	
49. 1st PR. S'R TRIAL SUB'T.	2	0	4								2	9	9	9	9	9	9	7	7	4	1	2	15	12	
50. PR. S'R ADD BACK	2	0	4															1	1	2	9	2	15	12	
51. SHIFT 1 POSITION	0	4															1	1	2	9	2	2	16	12	
52. 1st PR. S'R TRIAL SUB'T	0	4									1							7	9	0	4	2	16	12	
53. 2nd PR. S'R TRIAL SUB'T	0	4									2							4	5	1	6	2	16	12	
54. 3rd PR. S'R TRIAL SUB'T	0	4									3							1	1	2	8	2	16	12	
55. 4th PR. S'R TRIAL SUB'T	0	4									5	9	9	9	9	9	9	7	7	4	0	2	16	12	
56. PR. S'R ADD BACK	0	4									3							1	1	2	8	2	16	12	
57. SHIFT 1 POSITION	4									3							1	1	2	8	2	0	17	13	
58. 1st PR. S'R TRIAL SUB'T	4									3	1							7	8	9	4	0	17	13	
59. 2nd PR. S'R TRIAL SUB'T	4									3	2							4	5	0	6	0	17	13	
60. 3rd PR. S'R TRIAL SUB'T	4									3	3							1	1	1	8	0	17	13	
61. 4th PR. S'R TRIAL SUB'T	4									3	5	9	9	9	9	9	9	7	7	3	0	0	17	13	
62. PR. S'R ADD BACK	4									3	3							1	1	1	8	0	17	13	
63. SHIFT 1 POSITION									3	3							1	1	1	8	0	4	18	14	
64. 1st PR. S'R TRIAL SUB'T									3	3	1							7	7	9	2	4	18	14	

PROCESS	M-SECTION CALC. DEC. REF. POINT											A-SECTION INPUT											COUNTER		
	11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	DEC	M-D	CCT
MINIDEND											11				-	3	3	3	3						
SUBVISOR											13							3	3	8	8				
STORAGE DECIMAL											16														
65. 2nd PR. S'R TRIAL SUB'T.									3	3	2							4	4	0	4	4	18	14	
66. 3rd PR. S'R TRIAL SUB'T									3	3	3							1	0	1	6	4	18	14	
67. 4th PR S'R TRIAL SUB'T									3	3	5	9	9	9	9	9	9	7	6	2	8	4	18	14	
68. PR S'R ADD BACK									3	3	3							1	0	1	6	4	18	14	
69. SHIFT 1 POSITION								3	3	3							1	0	1	6	4		19	15	
70. 1st PR S'R TRIAL SUB'T								3	3	3	1							6	7	7	6		19	15	
71. 2nd PR S'R TRIAL SUB'T								3	3	3	2							3	3	8	8		19	15	
72. 3rd PR S'R TRIAL SUB'T								3	3	3	3							0	0	0	0		19	15	
73. 4th PR S'R TRIAL SUB'T								3	3	3	5	9	9	9	9	9	9	6	6	1	2		19	15	
74. PR S'R ADD BACK								3	3	3	3												19	15	
75. SHIFT 1 POSITION							3	3	3	3													20	16	
76. 1st PR S'R TRIAL SUB'T							3	3	3	3	2	9	9	9	9	9	9	6	6	1	2		20	16	
77. PR S'R ADD BACK							3	3	3	3													20	16	
78. SHIFT 1 POSITION						3	3	3	3														21	17	
79. TRIAL SUB'T						3	3	3	3		2	9	9	9	9	9	9	6	6	1	2		21	17	
80. ADD BACK						3	3	3	3														21	17	
81. SHIFT					3	3	3	3															22	18	
82. TRIAL SUB'T					3	3	3	3			2	9	9	9	9	9	9	6	6	1	2		22	18	
83. ADD BACK					3	3	3	3															22	18	
84. SHIFT				3	3	3	3																1	19	
85. TRIAL SUB'T				3	3	3	3				2	9	9	9	9	9	9	6	6	1	2		1	19	
86. ADD BACK				3	3	3	3																1	19	
87. SHIFT			3	3	3	3																	2	20	
88. TRIAL SUB'T			3	3	3	3					2	9	9	9	9	9	9	6	6	1	2		2	20	
89. ADD BACK			3	3	3	3																	2	20	
90. SHIFT		3	3	3	3																		3	21	
91. TRIAL SUB'T		3	3	3	3						2	9	9	9	9	9	9	6	6	1	2		3	21	
92. ADD BACK		3	3	3	3																		3	21	
93. SHIFT 1 POSITION	3	3	3	3																			4	22	
94. TRIAL SUB'T	3	3	3	3							2	9	9	9	9	9	9	6	6	1	2		4	22	
95. ADD BACK	3	3	3	3																			4	22	
96. B-2 ZEROIZE	3	3	3	3																			4	0	

PROCESS	M-SECTION CALC. DEC. REF. POINT											A-SECTION INPUT											COUNTER		
	11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	DEC	M-D	CCT
MINIDEND											11				-	3	3	3	3						
SUBVISOR											13							3	3	8	8				
STORAGE DECIMAL											16														
97. M'D DECIMAL	3	3	3	3																			15		
98. PR. RES. SHIFTED DCR AT 22																3	3	3	3				22		7
99. M'D NUM. REG.																0	0	0	0				22		7
100. SHIFT 3 CCT=10																							3		CT10
101. ZERO CHECK																									

MULTIPLICATION DIVISION COUNTER

Plate 21C

This Counter is employed in the Multiplication or Division processes only. The method of reading the Counter is the same as the Decimal Counter. The Counter receives its count from Shift Pulses and is conditioned opened or closed to accept these pulses. The actual operation of this Counter will be explained when it is used in Multiplication or Division, see plates 23 or 25 . The main purpose of the Counter is to keep track of the Result value so the Computer knows when the actual Multiplication or Division process is completed.

General Operation

Gate PGMD controls the admission of Shift Pulses into the M-D Counter. This Gate has a cathode control which is conditioned by the Multiplication or Division Process. The left input to the Gate is controlled by the RP of Trigger PDB so that the Gate can be opened or closed during the Process. The M-D Counter has a capacity of 22.

MULTIPLICATION PROCESS CALL

Plate 22C

This circuit is the prelude to the actual Multiplication Process. The Process Call Circuit prepares Gates, KB and makes the proper Decimal Registrations. This circuit is the preliminary for plate 23.

Operation

Trigger EM is returned left by a Control Ring Pulse. The LP of EM returns low to the RC of ES, triggering ES right. The LP of ES goes high to the LI of ESA. The LP of ESA goes low to LI of ESK and to diode ENM to check for Minus Factor. The K of ESK goes low to all ESF stages finding one stage which conducts to raise KB as shown on plate 38.

The RP of ES goes low to the LI of EP2 to check on Process. The LP of EP2 is cutoff and connected to the LP of EIM which is also cutoff (X Process). The LP of EP2 and LP of EIM raise the plates of diode EIM1. The LK of EIM1 raises the LI of DPG1, opening the Gate. The RK of EIM1 raises the RI of DMD, tapping off the RD of DMD to the LD of PMP as shown on plate 23 . The RP of DMD goes low to the RP of DEM. The RP of DEM going low lowers the DBC cathode line to condition for a Decimal Complement Registration. The LP of DEM goes high to the RC of DEA1 and also high to DBT raising the DBT cathode line. The RP of DEA1 releases a negative pulse to the RP of DEA, kicking DEA right.

After 150 us DEA returns left and the LP of DEA returns low to the RC of DP1 starting a cycle of Decimal Registration. This will be a Decimal Complement Registration since the DBC cathode line is low.

After 25 us DP1 returns left and the LP of DP1 goes low to the LC of DA1-16. The LP of DA1-16 releases a positive pulse to the LC and RC points of Gate DKG. DKG is open on the right since Trigger DK is left at this time. The RP of DKG releases a negative pulse to the RP of DP2 to continue the Decimal Registration.

The completion of a Decimal Registration is signaled by a negative pulse from the RP of DIC to the RC of DA1-16. The RP of DA1-16 releases a positive pulse to the LC of the open Gate DPG1. The LP of DPG1 releases a negative pulse to the RC and LC points of DK, triggering DK right. The RP of DK goes low to the RI of DKG, closing the right Gate. The LP of DK goes high to the LI of DKG, opening the left Gate. The LD of DKG taps off high to open DI1 and DB16, as shown on plate 4, to condition the Decimal Counter Gates for a Constant 17 Registration. The LP of DK also goes high to the LC of DEA1. The LP of DEA1 releases a negative pulse to the RP of DEA, kicking DEA right.

After 150 us DEA returns left and the LP of DEA returns low to the RC of DP1 starting a cycle of Decimal Registration. This registration will be to register the M-D Constant of 17. The value of 17 is a correction factor needed because of the Calculator Decimal Reference Point Location.

After 25 us DP1 returns left sending the LP of DP1 low to the LC of DA1-16. The LP of DA1-16 releases a positive pulse to the RC and LC points of Gate DKG. The left side of DKG is open (DK is right). The LP of DKG releases a negative pulse to the RP of DP16. The only decimals registered were the 1 and 16 for a total of 17.

The completion of a Decimal Registration is signaled by a negative pulse from the RP of DIC to the RC of DA1-16. The RP of DA1-16 releases a positive pulse to the LC of the open Gate DPG1. The LP of DPG1 releases a negative pulse to the RC and LC points of DK, returning DK left. DK returning left reconditions DKG open on the right and closed on the left. The RP of DK returns high to the LC of PMM to start shifting the M'd to 11M. This operation is shown on plate 23.

MULTIPLICATION PROCESS

Plate 23C

This circuit shows the controls required to perform the Multiplication Operation. The Computer does this operation as follows:

1. Shift the first M'd digit to 11M.
2. Add the S'r in the A Section and for each addition decrease the 11M digit by one.
3. When the 11M digit reaches zero, shift the next digit into 11M.
4. Add the S'r in the A Section as before.
5. Continue this process counting each shift in the M-D Counter.
6. When a digit arrives in 11M and the M-D Counter has reached or exceeded 22 the Multiplication Operation has been completed.
7. Zeroize the A Section so only a maximum of 11 Result digits remain.

Operation

This circuit is best explained when a specific problem is employed as an example.

The Work Sheet problem, line at a time, will be this example.

Lines 1 to 3 are not shown in this circuit.

Line 4

Subvisor Decimal Complement Registration - This operation is shown on plate 22. The preparation on plate 22 will raise the LD of PMP. The LP of PMP goes high to the following.

1. The RI of PSG - The RP of PSG goes low to the LI of PSGK. The K of PSGK goes low to the K of PGMD, opening this Gate.

2. The RI of PMG opening this Gate. The RD of PMG taps off high to RD of PDX, RD of PDMS and the right bias of PZG. PDX and PZG are now opened but PDMS still has a high cathode.

These Gates will remain open all during the ES Control Circuit Operation.

Line 5

Constant 17 is registered in the Decimal Counter. This operation is not shown on this circuit (DK right).

Line 6

Shift Operation until the first M'd digit arrives in 11M. Trigger DK returns left sending the RP of DK high to the LC of PMM. The LP of PMM releases a negative pulse to the RP of PMD2, kicking PMD2 right. PMD2 has a 25 us delay which at this time serves no purpose.

After 25 us PDM2 returns left. The LP of PMD2 returns low to the RC of PM1, triggering PM1 right. The LP of PM1 goes high to the LP of diode SI-1. The cathodes of SI-1 go high to the LD of SMC, starting the Shift Operation.

On line 4 it was stated that the M-D Counter Gate PGMD was opened to receive shifts into this Counter. The entire Counter is shown on plate 21 but in this circuit enough is shown to represent the control it employs.

After 6 shifts PC16 goes right and the RP of PC16 goes low to trigger PDT right. At a count of 10, PC4 goes right and the LP of PC4 goes high to open the left side of PCG. At a count of 11, PC1 again goes right sending the LP of PC1 high to the LC of the open Gate PCG. The LP of PCG releases a negative pulse to the LC of PDT, triggering PDT back left. The LP of PDT going low does the following:

1. Triggers P11S right. The RP of P11S lowers the LI of P11G. The K of P11G goes low to the K of PDMS. PDMS is now fully open.

   NOTE: The cathode control on PDMS is necessary to prevent the Shift Operation from being stopped too soon. This condition could arise in the proof. Shifting is to be stopped when the first digit reaches 11M. In the

proof, some digits may already be in the M Section when shifting starts. These digits should not stop shifts. Since the Result is never larger than 11 digits the Gate PDMS doesn't open until 11 shifts are completed.

2. Triggers PDB right. The RP of PDB goes low to the LI of PGMD. This low level closes the M-D Counter to prevent counting any more shifts at this time.

Shifting continues until the first M'd digit arrives in 11M. This digit will, in the work sheet, trigger T1 right and TØ left in Accumulator 11M. The RP of TØ and LP of T1 go high to the inputs of PMS. The plates of PMS go low to the LI of PMØ. The LP of PMØ goes low to the LI of PM12 closing the left side of this Gate. The RP of PMØ goes high to the RC of the open Gates PDX and PDMS. The RP of PDX releases a negative pulse to the LP of PDB, triggering PDB back left. The RP of PDB returning high to the LI of PGMD reopens the M-D Counter to count shifts. The RP of PDMS releases a negative pulse to the LP of PM1, returning PM1 left. The LP of PM1 returns low through SI-1 stopping shifts.

Line 7

The First Subvisor Addition is made. The RP of PM1 returns high to the RC of PMG. Gate PMG was opened by the Process so the RP of PMG releases a negative pulse to the RP of PMD1, kicking PMD1 right. The LP of PMD1 goes high to the LC of the open Gate PMG. The LI of PMG is high from the LP of PC16 since PC16 is right. The LP of PMG releases a negative pulse to the RP of PMBT, triggering PMBT right. The LP of PMBT goes high to the RI of PM12 opening the right side of this Gate.

After 14 us PMD1 returns left and sends the LP of PMD1 low to the LC of PDM3. The LA of PDM3 releases a positive pulse to the RC of the open Gate PM12 (PMBT is right). The RP of PM12 releases a negative pulse to the RP of PM2, triggering PM2 right.

The RP of PM2 goes low to the LI of PM23. The LP of PM23 goes high to raise SB and call for a cycle of RIG. The SB operation is shown on plate 45 , The LP of PM2 goes high to the LI of PMDR to open the left side of this Gate. The LD of PMDR taps off high to the RI of Gate I1-11 to allow the RIG 1' Pulse to enter Accumulator 11M as shown on plate 5.

Line 8

The Second Subvisor Addition is made. The completion of the first S'r Addition is signified by a CX Pulse to the RC of PM3, kicking PM3 right. The LA of PM3 goes high to the LC of the closed Gate PM12 (digit in 11M so the LP of PMØ is low).

After 25 us PM3 returns left and the LP of PM3 returns low to the RC of PM23. The RA of PM23 releases a positive pulse to the LC of the open Gate PMDR (PM2 is right). The LP of PMDR releases a negative pulse to the RP of RS to start another cycle of RIG. SB is still high since PM2 is right.

Line 9

The Third Subvisor Addition is made. This operation is identical to line 8.

Line 10

Shift until a digit arrives in 11M. The completion of the third S'r Addition is signified by a CX Pulse to the RC of PM3, kicking PM3 right. The LA of PM3 goes high to the LC of the now opened Gate PM12. Accumulator 11M is now zero so both inputs of PMS are low cutting off both plates of PMS. The plates of PMS go high to the LI of PMØ. The LP of PMØ goes high to the LI of PM12, opening this Gate. The LP of PM12 releases a negative pulse to the LP of PM2, triggering PM2 back left. The LP of PM2 returns low to close Gates PMDR and I1-11. The RP of PM2 returns high to lower SB.

The RP of PM2 also goes high to the RC of PMM. The RP of PMM releases a negative pulse to the RP of PMD2, kicking PMD2 right. PMD2 has a 25 us delay to give SB time to lower. After 25 us PMD2 returns left and the LP of PMD2 goes low to the RC of PM1, triggering PM1 right. The LP of PM1 goes high to the LP of diode SI-1. The cathodes of SI-1 go high to the LD of SMC starting the Shift Operation.

The next digit arrives in 11M. The shifts are counted in both the M-D and Decimal Counters. The Input to PMS goes high causing the plates of PMS to go low. The plates of PMS go low to the LI of PMØ. The LP of PMØ goes low to the LI of PM12 closing the left side of this Gate. The RP of PMØ goes high to the RC of the open Gate PDMS. The RP of PDMS releases a negative pulse to the LP of PM1, returning PM1 left. The LP of PM1 returns low through SI-1 stopping shifts.

Line 11

First Subvisor Addition is made. This operation is identical to line 7.

Line 12

Second Subvisor Addition is made. This operation is identical to line 8.

Line 13

Third Subvisor Addition is made. This operation is identical to line 8.

Line 14

Shift until a digit arrives in 11M. This operation is identical to line 10.

Lines 15 through 21

Follow identical patterns which have been explained on lines 7, 8 and 10.

Line 22

Shift until a digit arrives in 11M. At this time the M-D Counter has

reached a count of 22. When the count of 22 was reached Trigger PC16 returned left. The LP of PC16 going low does the following:

1. PMDZ is kicked right.
2. Gate PMG is closed on the left side.
3. PMBT is returned left. LP of PMBT goes low to the RI of PM12 closing the right side of this Gate.

Even though the M-D Counter reaches 22, shifting can continue since the Shift Operation is controlled only by a digit arriving in 11M. At this time the digit that will now arrive in 11M will be a Result digit as proven by the fact that the M-D Counter has reached 22. The digit in 11M causes the plates of PMS to go low. The low from PMS lowers the LI of PMØ. The RP of PMØ goes high to the RC of the open Gate PDMS. The RP of PDMS releases a negative pulse to the LP of PM1, returning PM1 left stopping shifts.

The RP of PMØ also goes high to the RC of the open Gate Amplifier PZG. The RP of PZG releases a negative pulse to the RP of PMØD, kicking PMØD right. PMØD has a 25 us delay to allow PMDZ time to operate if the Result digit arrives in 11M at the same time the M-D Counter reaches 22. After 25 us PMØD returns left sending its LP low to the LC of PMDZ, returning PMDZ left.

NOTE: Stage PM22 clamps PMBT left when the M-D Counter reaches 22. The clamping action on PMBT prevents retriggering PMBT back right in the event the left side of Gate PMG is slow in closing at the time the M-D Counter reaches 22 when the first Result digit arrives in 11M. If PMBT were retriggered an additional RIG and shift would occur and the first Result digit would be lost.

Line 23

B-2 Zeroize. After PMDZ returns left the RP of PMDZ goes high to the LC of the open Gate EMDC (EZB2 is left). The LP of EMDC releases a negative pulse to the RP of EMDZ, kicking EMDZ right. The LP of EMDZ goes high to the RC of ECS. The RP of ECS releases a negative pulse to the RP of EZB2, kicking EZB2 right. The RP of EZB2 goes low to perform the B2 Zeroize as shown on plate 36 . This operation will Zeroize the A Section of the Accumulators, M-D Counter and the Check Counter. The B-2 Zeroize is completed when EZB2 returns left after a 300 us delay.

After 450 us EMDZ returns left. The RP of EMDZ returns high to the RC of EMDC. The RP of EMDC releases a negative pulse onto the Control Ring. This Control Ring Pulse returns ES left and pulls ER right. The ER or Result Operation is shown on plate 15.

SIGN COMPUTATION

Plate 20C

The writeup for Complementize explains the method used to determine the sign of the answer in Addition or Subtraction Process. In Multiplication or Division the sign of the Result is minus if only one of the factors is negative. If both factors are negative the sign of the result will be positive.

Operation

The example on the Multiplication Process Work Sheet uses a negative M'd in the calculation resulting in a negative answer. This problem will be used as an example.

Trigger EM goes right to raise the M'd Keyboard Bias. The M'd is a negative number so the Minus Neon Common Line comes high to raise the grids of MC4. The LP of MC4 goes low to the LI of MC5. The RI of MC5 is also low since MC2 is left. The plates of MC5 going high raise the RP of MCX. The cathodes of MCX go high to the LI of PSIG, opening the Gate.

The LP of EM goes high to the LI of EMA causing the LP of EMA to go low to the LC of diode ENM. The LP of ENM releases a negative pulse to the RD of PAMD, kicking PAMD right. PAMD has a time delay to give KB time to rise. PAMD returning left sends its RP high to the LC of the open Gate PSIG. The LP of PSIG releases a negative pulse to the RC of PSIG. The RP of PSIG releases a positive pulse to the RC and LC of Gate PS.

NOTE: The Process is Multiplication so the LK of diode PIMD is low. The plates of PIMD go low to the LI of PPI. The LP of PPI goes high to the RI of PS opening the Gate.

The RP of PS releases a negative pulse to the RC and LC of PAT, triggering PAT right.

The return of EM kicks ES right to raise the S'r KB. The S'r is a positive number so the Minus Neon Common is not raised and Gate PSIG is closed. During ES time, therefore, PAT remains on the right.

PAT, being right during ER time, indicates a negative answer. The Result Storage Minus Bit and Minus Branch Gate are conditioned as follows. The LP of PAT goes high to the RI of MC8. The RP of MC8 goes low to:

1. The LI of SSRO to condition the Minus Bit as shown on plate 46.
2. The LI of MC7 causing the LP of MC7 to go high and raise the LI of EBG, the Minus Branch Gate.

DIVISION PROCESS

Work Sheet

This work sheet shows the procedure the Computer follows in order to divide one number by the other, store the result and prove the answer. The procedure will be the same in any Division problem where both the divisor and dividend are values other than zero. The only variations will occur in the numerical values and decimal position. The problem used as an example has the following values:

Minidend	V1	44.44	5/4 Decimal
Subvisor	V2	2.2	6/5 Decimal
Result	R		1/0 Decimal

CALCULATOR ZEROIZE

Plate 11C

Line 1

Calculator Zeroized. All Triggers are normalized including Accumulators, Counters and Control Triggers. Storage is Zeroized.

MINIDEND REGISTRATION

Plate 13C

Line 2

Minidend Decimal Complement is registered in the Decimal Counter.

Line 3

Minidend Numerical Registration is made (cycle of RIG). The M'd is registered in the Accumulators.

DIVISION PROCESS CALL

Plate 24C

Line 4

Subvisor Decimal is added in the Decimal Counter.

Line 5

The M-D Constant of 17 is added in the Decimal Counter.

Line 6

The Minidend is shifted until its first digit reaches Accumulator 11M. All shifts are counted in the Decimal Counter. Only the first 11 shifts and one extra count (total of 12) are counted in the M-D Counter.

Line 7

First Subvisor Trial Subtraction is made. The S'r Numerical Registration is made (cycle of RIG). This Trial Subtraction is unsuccessful and so indicated by an overcarry in Accumulator 11A. A one is also added in Accumulator 1M from RIG 1'. A Section raises Subtract Bias, M Section raises Add Bias. 1M Accumulator has a value of 2.

Line 8

Subvisor is Added Back. The S'r Numerical Registration is made (cycle of RIG). The A Section is returned to zero. 1M is returned to zero. A Section raises Add Bias, M Section raises Subtract Bias.

Line 9

Minidend is shifted one position. The Decimal Counter counts this shift. The M-D Counter remains closed to shifts.

Line 10

Same as line 7.

Line 11

Same as line 8.

Line 12

Same as line 9.

Lines 13 through 24 inclusive continue in a similar sequence.

Line 25

First Subvisor Trial Subtraction is made. The S'r Numerical Registration is made (cycle of RIG). The M'd has been shifted into a position so that when the S'r is subtracted no 11A overcarry occurs. A one is added in Accumulator 1M by the RIG1' Pulse. The M-D Counter is now opened to count shifts.

Line 26

Second Subvisor Trial Subtraction is made. The S'r Numerical Registration

is again made (cycle of RIG). Again no 11A overcarry occurs. Another one is added to Accumulator 1M making a total of 2.

Line 27

Third Subvisor Trial Subtraction is made. Another S'r Numerical Registration is made (cycle of RIG). An 11A overcarry occurs indicating an Unsuccessful Trial Subtraction. A one is added to 1M by RIG1' and the overcarry making a total of 4 in Accumulator 1M.

Line 28

Subvisor Add Back is made. A S'r Numerical Registration is made (cycle of RIG). The S'r is added in the A Section which returns the A Section and Accumulator 1M to the values prior to the last Trial Subtraction. Accumulator 1M is now 2.

Line 29

Shift one position. All digits are shifted one position. This shift is counted in both the Decimal and M-D Counter.

Line 30

Same as line 7.

Line 31

Same as line 8.

Line 32

Same as line 9 except the M-D counts this shift.

Lines 33-36

Same as lines 25-28.

Lines 37-57 continue with Trial Subtractions, Add Back and shifts.

Line 58

Shift one position. The digits are shifted one position. The M-D Counter reaches a count of 22 indicating the completion of Division. The first Result digit is in 11M.

Line 59

Same as line 7.

Line 60

Same as line 8.

Line 61

B-2 Zeroize. The A Section and M-D Counter are Zeroized leaving a maximum of 11 Result digits.

RESULT TO STORAGE

Plate 15C

Line 62

The Storage Decimal is added in the Decimal Counter.

Line 63

The result is shifted to align with the Storage Decimal. This alignment is indicated by the Decimal Counter reaching 22.

Line 64

Test RIG. A Numerical Registration (cycle of RIG) of Storage is made. This value is zero.

Line 65

Result to Storage. Any digit in Accumulators 1A to 10A will be set in Storage.

Line 66

B-2 Zeroize. Accumulators 1A-11A are Zeroized leaving the Result in Storage.

PROOF MINIDEND REGISTRATION

Plate 16C

Line 67

Proof Minidend Decimal Complement is registered in the Decimal Counter.

Line 68

Proof Minidend Numerical Registration is made (cycle of RIG). The Result value is added in the A Section.

MULTIPLICATION PROCESS CALL

Plate 22C

Lines 69-78--See Multiplication Work Sheet for this operation from line 4-23 for

theory of operation.

MINIDEND SUBTRACTION

Plate 18C

Line 79

Minidend Decimal is added in the Decimal Counter

Line 80

Proof Result is shifted to align with the M'd Decimal. This alignment is indicated by the Decimal Counter reaching 22. These shifts are also counted in the Check Counter.

Line 81

Minidend Numerical Registration is made (cycle of RIG). The value in the Accumulators is now zero in this problem. It is possible, in some problems, for the Accumulators to have a value of nines.

ZERO CHECK

Plate 19C

Line 82

A Shift Operation occurs to bring the count in the Check Counter to 10. In this particular problem 4 shifts are required. The number of shifts will vary from zero to ten depending upon the problem.

Line 83

A Zero Check is now made in Accumulators 1A-10A. In this particular problem the Zero Check is successful. If the Zero Check is not successful because of nines, a one is added to 1A to create a Zero Check condition.

PROCESS	M-SECTION CALC. DEC. REF. POINT											A-SECTION INPUT											COUNTER		
	11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	DEC	M-D	CCT
MINIDEND											12						4	4	4	4					
SUBVISOR											11						2	2							
STORAGE DECIMAL											16														
1. CALC. ZEROIZE																									
2. M'D DEC. COMPL.																							10		
3. M'D NUM. REG.																	4	4	4	4			10		
4. S'R DECIMAL																	4	4	4	4			21		
5. CONSTANT 17																	4	4	4	4			16		
6. SHIFT-DIGIT IN 11M	4	4	4	4																			10	12	CT11
7. 1st S'R TRIAL SUB'T	4	4	4	4							2	9	9	9	9	9	7	8					10	12	CT11
8. S'R ADD BACK	4	4	4	4																			10	12	CT11
9. SHIFT 1 POSITION	4	4	4																			4	11	12	CT11
10. 1st S'R TRIAL SUB'T	4	4	4								2	9	9	9	9	9	7	8				4	11	12	CT11
11. S'R ADD BACK	4	4	4																			4	11	12	CT11
12. SHIFT 1 POSITION	4	4																			4	4	12	12	CT11
13. 1st S'R TRIAL SUB'T	4	4									2	9	9	9	9	9	7	8			4	4	12	12	CT11
14. S'R ADD BACK	4	4																			4	4	12	12	CT11
15. SHIFT 1 POSITION	4																			4	4	4	13	12	CT11
16. 1st S'R TRIAL SUB'T	4										2	9	9	9	9	9	7	8		4	4	4	13	12	CT11
17. S'R ADD BACK	4																			4	4	4	13	12	CT11
18. SHIFT 1 POSITION																			4	4	4	4	14	12	CT11
19. 1st S'R TRIAL SUB'T											2	9	9	9	9	9	7	8	4	4	4	4	14	12	CT11
20. S'R ADD BACK																			4	4	4	4	14	12	CT11
21. SHIFT 1 POSITION																		4	4	4	4		15	12	CT11
22. 1st S'R TRIAL SUB'T											2	9	9	9	9	9	8	2	4	4	4		15	12	CT11
23. S'R ADD BACK																		4	4	4	4		15	12	CT11
24. SHIFT 1 POSITION																	4	4	4	4			16	12	CT11
25. 1st S'R TRIAL SUB'T											1						2	2	4	4			16	12	CT11
26. 2nd S'R TRIAL SUB'T											2						0	0	4	4			16	12	CT11
27. 3rd S'R TRIAL SUB'T											4	9	9	9	9	9	7	8	4	4			16	12	CT11
28. S'R ADD BACK											2						0	0	4	4			16	12	CT11
29. SHIFT 1 POSITION										2								4	4				17	13	CT11
30. 1st S'R TRIAL SUB'T										2	2	9	9	9	9	9	8	2	4				17	13	CT11
31. S'R ADD BACK										2	0							4	4				17	13	CT11
32. SHIFT 1 POSITION									2	0							4	4					18	14	CT11

PROCESS	M-SECTION CALC. DEC. REF. POINT											A-SECTION INPUT											COUNTER		
	11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	DEC	M-D	CCT
MINIDEND											12						4	4	4	4					
SUBVISOR											11						2	2							
STORAGE DECIMAL											16														
33. 1st S'R TRIAL SUB'T									2	0	1						2	2					18	14	CT11
34. 2nd S'R TRIAL SUB'T									2	0	2						0	0					18	14	CT11
35. 3rd S'R TRIAL SUB'T									2	0	4	9	9	9	9	9	7	8					18	14	CT11
36. S'R ADD BACK									2	0	2												18	14	CT11
37. SHIFT 1 POSITION								2	0	2													19	15	CT11
38. 1st S'R TRIAL SUB'T								2	0	2	2	9	9	9	9	9	7	8					19	15	CT11
39. S'R ADD BACK								2	0	2													19	15	CT11
40. SHIFT 1 POSITION							2	0	2														20	16	CT11
41. 1st S'R TRIAL SUB'T							2	0	2		2	9	9	9	9	9	7	8					20	16	CT11
42. S'R ADD BACK							2	0	2														20	16	CT11
43. SHIFT 1 POSITION						2	0	2															21	17	CT11
44. 1st S'R TRIAL SUB'T						2	0	2			2	9	9	9	9	9	7	8					21	17	CT11
45. S'R ADD BACK						2	0	2															21	17	CT11
46. SHIFT 1 POSITION					2	0	2																22	18	CT11
47. 1st S'R TRIAL SUB'T					2	0	2				2	9	9	9	9	9	7	8					22	18	CT11
48. S'R ADD BACK					2	0	2																22	18	CT11
49. SHIFT 1 POSITION				2	0	2																	1	19	CT11
50. 1st S'R TRIAL SUB'T				2	0	2					2	9	9	9	9	9	7	8					1	19	CT11
51. S'R ADD BACK				2	0	2																	1	19	CT11
52. SHIFT 1 POSITION			2	0	2																		2	20	CT11
53. 1st S'R TRIAL SUB'T			2	0	2						2	9	9	9	9	9	7	8					2	20	CT11
54. S'R ADD BACK			2	0	2																		2	20	CT11
55. SHIFT 1 POSITION		2	0	2																			3	21	CT11
56. 1st S'R TRIAL SUB'T		2	0	2							2	9	9	9	9	9	7	8					3	21	CT11
57. S'R ADD BACK		2	0	2																			3	21	CT11
58. SHIFT 1 POSITION	2	0	2																				4	22	CT11
59. 1st S'R TRIAL SUB'T	2	0	2								2	9	9	9	9	9	7	8					4	22	CT11
60. S'R ADD BACK	2	0	2																				4	22	CT11
61. B2 ZEROIZE	2	0	2																				4	0	Ø
62. STOR. DECIMAL	2	0	2																				20		Ø
63. RES. SHIFTED DCR AT 22	2																				2	0	22		
64. TEST RIG	2																				2	0	22		

PROCESS	M-SECTION CALC. DEC. REF. POINT											A-SECTION INPUT											COUNTER		
	11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	DEC	M-D	CCT
MINIDEND											12						4	4	4	4					
SUBVISOR											11						2	2							
STORAGE DECIMAL											16														
65. RESULT TO STORAGE	2																				2	0	22		
66. B2 ZEROIZE	2																				0	0	22		
67. PR. M'D DEC. COMPL.	2																				0	0	6		
68. PR. M'D NUM. REG.	2																				2	0	6		
69. PR. S'R DEC. COMPL.	2																				2	0	17		
70. CONSTANT 17	2																				2	0	12		
71. SHIFT-DIGIT IN 11M	2	0	2																				10	11	
72. 1st PR. S'R ADDITION	1	0	2														2	2					10	11	
73. 2nd PR. S'R ADDITION	0	0	2														4	4					10	11	
74. SHIFT DIGIT IN 11M	2														4	4							12	13	
75. 1st S'R ADDITION	1														4	4	2	2					12	13	
76. 2nd S'R ADDITION	0														4	4	4	4					12	13	
77. SHIFT-DIGIT IN 11M	4	4	4	4																			4	22	
78. B2 ZEROIZE	4	4	4	4																			4	0	
79. M'D DECIMAL	4	4	4	4																			16		
80. RES. SHIFTED DCR AT 22																	4	4	4	4			22		6
81. M'D SUBTRACTION																	0	0	0	0			22		6
82. SHIFT - CCT IS 10																							4		10
83. ZERO CHECK																							4		10

DIVISION PROCESS CALL

Plate 24C

This circuit is the prelude to the actual Division Process. The Division Process Call Circuit prepares Gates, KB and makes the proper Decimal Registrations. This circuit is the preliminary for plate 25.

Operation

Trigger EM is returned left by a Control Ring Pulse. The LP of EM returns low to the RC of ES, triggering ES right. The LP of ES goes high to the LI of ESA. The LP of ESA goes low to the LI of ESK and to diode ENM to check for Minus Factor. The K-ESK goes low to all ESF stages finding one stage which conducts to raise KB as shown on plate 38.

The RP of ES goes low to the LI of EP2 to check on Process. The RP of EP2 is cutoff and connected to the LP of EID which is also cutoff (÷ Process). The RP of EP2 and LP of EID raise the plates of diode EID2. The LK of EID2 raises the LI of DPG1, opening the Gate. The RK of EID2 goes high to the LI of PDP which is shown on plate 25 . The RK of EID2 also goes high to the RC of DEA2. The RP of DEA2 releases a negative pulse to the RP of DEA, kicking DEA right.

After 150 us DEA returns left and the LP of DEA returns low to the RC of DP1 starting a cycle of Decimal Registration. This will be a True Decimal Registration since the DBT line is low.

After 25 us DP1 returns left and the LP of DP1 goes low to the LC of DA1-16. The LP of DA1-16 releases a positive pulse to the LC and RC points of Gate DKG. DKG is open on the right side since Trigger DK is left at this time. The RP of DKG releases a negative pulse to the RP of DP2 to continue the Decimal Registration. The completion of a Decimal Registration is signaled by a negative pulse from the RP of DIC to the RC of DA1-16. The RP of DA1-16 releases a positive pulse to the LC of the open Gate DPG1. The LP of DPG1 releases a negative pulse to the RC and LC points of DK, triggering DK right. The RP of DK goes low to the RI of DKG, closing the right Gate. The LP of DKG goes high to the LI of DKG, opening the left Gate. The LD of DKG taps off high to open DI1 and DB16, as shown on plate 4. This conditions the Decimal Counter Gates for a Constant 17 Registration. The LP of DK goes high to the LC of DEA1 also. The LP of DEA1 releases a negative pulse to the RP of DEA, kicking DEA right.

After 150 us DEA returns left and the LP of DEA returns low to the RC of DP1 starting a cycle of Decimal Registration. This registration will be to register the M-D Constant of 17. The value of 17 is a correction factor needed because of the Calculator Decimal Reference Point Location.

After 25 us DP1 returns left sending the LP of DP1 low to the LC of DA1-16. The LP of DA1-16 releases a negative pulse to the RC and LC points of Gate DKG. The left side of DKG is open (DK is right). The LP of DKG releases a negative pulse to the RP of DP16. The only decimals registered were the 1 and 16 for a total of 17.

The completion of a Decimal Registration is signaled by a negative pulse from the

RP of DIC to the RC of DA1-16. The RP of DA1-16 releases a positive pulse to the LC of the open Gate DPG1. The LP of DPG1 releases a negative pulse to the RC and LC points of DK, returning DK left. DK returning left reconditions DKG open on the right and closed on the left. The RP of DK returns high to the LC of PMM to start shifting the M'd to 11M. This operation is shown on plate 25.

DIVISION PROCESS

Plate 25C

This circuit shows the controls required to perform the Division Operation. The Computer does this operation as follows.

1. Shift the first M'd digit to 11M.
2. Subtract the S'r in the A Section (Trial Subtraction).
3. An 11A to 1M overcarry indicates an Unsuccessful Trial Subtraction.
4. The S'r is Added Back.
5. Shift one position. Count in Decimal Counter only.
6. Steps 2, 3, 4 and 5 continue until no 11A to 1M overcarry occurs on a Trial Subtraction. A one is registered in 1M for each Trial Subtraction. The Trial Subtractions continue until an 11A to 1M overcarry occurs.
7. The S'r is Added Back.
8. Shift one position. This shift is counted in both the M-D and Decimal Counters.
9. Each individual shift from now on is added in the M-D Counter until this Counter reaches 22. At a count of 22 the first Result digit is always in 11M.
10. S'r Trial Subtraction.
11. S'r Add Back.
12. Zeroize the A Section so only a maximum of 11 Result digits remain.

Operation

This circuit is best explained when a specific problem is employed as an example. The Work Sheet problem, line at a time, will be this example. Lines 1 to 3 are not shown in this circuit.

Line 4

Subvisor Decimal Registration. This operation is shown on plate 24. The preparation on plate 24 will raise the LI of PDP. The LP of PDP goes high to the LI of PDMS, opening this Gate. The LP of PDP also goes high to the LI of PSG whose plate goes low through PSGK to lower the cathode on PGMD as shown on plate 21 . These Gates will remain open all during the ES Control Circuit Operation.

Line 5

Constant 17 is registered in the Decimal Counter. This operation is not shown on this circuit (DK right).

Line 6

Shift Operation until the first M'd digit arrives in 11M. Trigger

DK returns left sending the RP of DK high to the LC of PMM. The LP of PMM releases a negative pulse to the RP of PMD2, kicking PMD2 right. PMD2 has a 25 us delay which at this time serves no purpose.

After 25 us PMD2 returns left. The LP of PMD2 returns low to the RC of PM1, triggering PM1 right. The LP of PM1 goes high to the LP of diode SI-1. The cathodes of SI-1 go high to the LD of SMC, starting the Shift Operation.

On line 4 it was stated that the M-D Counter Gate PGMD was opened to receive shifts into this Counter. The entire Counter is shown on plate 21 but in this circuit enough is shown to represent the control it employs.

After 6 shifts PC16 goes right and the RP of PC16 goes low to trigger PDT right. At a count of 10 PC4 goes right and the LP of PC4 goes high to open the left side of PCG. At a count of 11 PC1 again goes right sending the LP of PC1 high to the LC of the open Gate PCG. The LP of PCG releases a negative pulse to the LC of PDT, triggering PDT back left. The LP of PDT going low does the following.

1. Triggers P11S right. The RP of P11S lowers the LI of P11G. The K of P11G goes low to the K of PDMS. PDMS is now fully open.

   NOTE: The cathode control on PDMS is necessary to prevent the Shift Operation from being stopped too soon. This condition could arise in the proof. Shifting is to be stopped when the first digit reaches 11M. In the proof, some digits may already be in the M Section when shifting starts. These digits should not stop shifts. Since the Result is never larger than 11 digits the Gate PDMS doesn't open until 11 shifts are completed.

2. Triggers PDB right. The RP of PDB goes low to the LI of PGMD. This low level closes the M-D Counter to prevent counting any more shifts at this time.

Shifting continues until the first M'd digit arrives in 11M. This digit will, in the work sheet, trigger TØ left in Accumulator 11M. The RP of TØ goes high to the RI of PMS.

The plates of PMS go low to the LI of PMØ. The RP of PMØ goes high to the LC of the open Gate PDMS, The RP of PDMS releases a negative pulse to the RC of PDND and RP of PDN kicking both stages right.

The LP of PDN goes high to the RC of PCG and PGMD. The RP of PCG releases a negative pulse to the LP of PM1, returning PM1 left and stopping shifts. The plates of PGMD release a negative pulse to the M-D Counter to bring the count in this counter to a value of 12.

Line 7

First Subvisor Trial Subtraction. After 25 us PDND returns left. The RP of PDND returns high to the RC of PDM and the RP of PDM releases a negative pulse to the RP of PD1, triggering PD1 right. The RP of PD1 goes low to the RI of PDA. The RP of PDA goes high to raise the Trial Subtraction Bias (1A-11A-, 1M-10+, 11M+). Raising Sign Bias automatically calls for a cycle of RIG as shown on plate 45 . The RD of PDA taps off low to the RD of PD1M. The RP of PD1M goes high to the RP of diode PX as shown on plate 5. The high from PX opens Gate I1-11 to allow the RIG1' Pulse to pass into 1M. The LP of PD1 goes high to raise the LI of PDX, opening this Gate. The LD of PDX taps off high to the RD of PMDR, opening this Gate.

The subtraction of the S'r, A Section is zero, results in a series of overcarries. The 11A overcarry through PS11 goes low to the RC of PDS, triggering PDS right. Accumulator 1M has a value of 2. The completion of this S'r Registration is indicated by a CX Pulse. The CX Pulse to the RC of PM3 kicks PM3 right. The RP of PM3 goes low to the LC of PDS, returning PDS left. The LP of PDS returns low to the LC of PD1 and PD2, returning PD1 left. PD1 returning left sends its LP low to close Gates PDX and PMDR. The RP of PD1 goes high to PDA to lower Sign Bias.

After 25 us PM3 returns left sending its LP low to the RC of PM23. The RP of PM23 releases a positive pulse to the LC of PDX and RC of PMDR. Both Gates are closed so the pulse is rejected.

The LP of PD1 also returns low to the RC of PD2, triggering PD2 right.

Line 8

Subvisor Add Back. PD2 was triggered right by the return of PD1 so the RP of PD2 goes low to the LI of PDA. The LP of PDA goes high to raise Add Back Sign Bias (1A-11A+, 1M-10M-, 11M-). Raising Sign Bias automatically calls for a cycle of RIG as shown on plate 45. The LD of PDA taps off low to the LD of PD1M. The LP of PD1M goes high to the LP of diode PX as shown on plate 5. The high from PX opens Gate I1-11 to allow the RIG1' Pulse to pass into 1M.

The Add Back of the S'r results in a series of overcarries. The 11A overcarry through PS11 goes low to the RC of PDS, triggering PDS right. The count in Accumulator 1M is now zero.

The completion of this S'r Registration is indicated by a CX Pulse. The CX Pulse to the RC of PM3 kicks PM3 right. The RP of PM3 goes low to the LC of PDS, triggering PDS left. The LP of PDS goes low to the LC of PD1 and PD2, triggering PD2 left. The return of PD2 left causes the RP of PD2 to return high to PDA and lower Sign Bias.

After 25 us PM3 returns left but as on line 7 the Gates are closed. The LP of PD2 returns low to the RC of PD2D, kicking PD2D right.

Line 9

Shift one position. After 25 us PD2D returns left. The purpose of the delay of PD2D is to allow Sign Bias to lower before starting shifts. The LP of PD2D returns low to the RC of PDM3. The RA of PDM3 releases a positive pulse to the LC of open Gate PDM (PC16 is right). The LP of PDM releases a negative pulse to the RP of PD3, triggering PD3 right.

The LP of PD3 goes high to the RP of diode SI-1. The K-SI1 goes high to the LD of SMC to call for shifts as shown on plate 4. The signal that a shift occurs comes from the LP of SG. The LP of SG releases a negative pulse to the LC of PD3, triggering PD3 back left.

The LP of PD3 returns low to SI-1 to stop shifts (only one occurred) and low to the RC of PD1, triggering PD1 right.

Line 10

Same as line 7 after PD1 goes right.

Line 11

Same as line 8.

Line 12

Same as line 9.

Lines 13-24

These operations are similar to lines 7, 8 and 9.

Line 25

First S'r Trial Subtraction. PD1 was triggered right when PD3 returned left on line 24. The RP of PD1 goes low to the RI of PDA. The RP of PDA goes high to raise the Trial Subtraction Sign Bias (1A-11A-, 1M-10M+, 11M+). Raising Sign Bias automatically calls for a cycle of RIG as shown on plate 45. The RD of PDA taps off low to the RD of PD1M. The RP of PD1M goes high to the RP of diode PX as shown on plate 5. The high from PX opens Gate I1-11 to allow the RIG1' Pulse to pass into 1M. The LP of PD1 goes high to the LI of PDX, opening this Gate. The LD of PDX taps off high to the RD of PMDR, opening this Gate.

This time when the S'r is subtracted the number present in the A Section is larger than the S'r value so no 11A to 1M overcarry occurs. Accumulator 1M has a value of one as a result of the RIG1' Pulse.

The completion of the S'r Registration is indicated by a CX Pulse. The CX Pulse to the RC of PM3 kicks PM3 right. The RP of PM3 goes

low to the LC of PDS but is rejected since PDS is left.

After 25 us PM3 returns left. The LP of PM3 returns low to the RC of PM23. The RA of PM23 releases a positive pulse to the LC of open Gate PDX and RC of open Gate PMDR.

The LP of PDX releases a negative pulse to the LP of PDB, triggering PDB back left. The RP of PDB returns high to the LI of PGMD to reopen the M-D Counter to accept any forthcoming Shift Pulses. The RP of PMDR releases a negative pulse to the RP of RS starting another cycle of RIG. Sign Bias for Trial Subtraction is still raised since PD1 is on the right.

Line 26

Same as line 25 except PDB remains left.

Line 27

This subtraction of the S'r results in a series of overcarries. The 11A overcarry through PS11 goes low to the RC of PDS, triggering PDS right.

The CX Pulse kicks PM3 right. The RP of PM3 goes low to the LC of PDS, triggering PDS back left.

The LP of PDS goes low to the LC of PD1 and PD2, triggering PD1 back left. PD1 returning left closes PDX and PMDR so that the return of PM3 is nullified. The RP of PD1 goes high to PDA to lower Sign Bias. The LP of PD1 goes low to the RC of PD2, triggering PD2 right. Accumulator 1M has a value of 2.

Line 28

Same as line 8.

Line 29

Same as line 9.

Line 30

Same as line 7.

Line 31

Same as line 8.

Line 32

Same as line 9.

Line 33

Same as line 25.

Line 34

Same as line 26.

Line 35

Same as line 27.

Lines 36-57

These operations are similar to lines 7, 8 and 9.

Line 58

Shift one position. This Shift Pulse brings the count in the M-D Counter to 22. A count of 22 is indicated by PC16 returning left. The RP of PC16 goes high to the LI of PZG, opening the Gate. The LP of PC16 goes low to the LI of PDM, closing this Gate and low to the RC of PMDZ, triggering PMDZ right.

Line 59

Same as line 7.

Line 60

Same as line 8.

Line 61

B-2 Zeroize. PD2 returns left sending its LP low to the RC of PD2D, kicking PD2D, right. After 25 us PD2D returns left. The LP of PD2D goes low to the RC of PDM3. The RA of PDM3 releases a positive pulse to the LC of the closed Gate PDM and LC of the open Gate PZG. The LP of PZG releases a negative pulse to the LP of PMDZ, triggering PMDZ back left.

The RP of PMDZ goes high to the LC of the open Gate EMDC (EZB2 is left). The LP of EMDC releases a negative pulse to the RP of EMDZ, kicking EMDZ right. The LP of EMDZ goes high to the RC of ECS, The RP of ECS releases a negative pulse to the RP of EZB2, kicking EZB2 right. The RP of EZB2 goes low to perform the B-2 Zeroize as shown on plate 36. This operation will Zeroize the A Section of the Accumulators, M-D Counter and the Check Counter. The B-2 Zeroize is completed when EZB2 returns left after a 300 us delay. After 450 us EMDZ returns left. The RP of EMDZ returns high to the RC of EMDC. The RP of EMDC releases a negative pulse onto the Control Ring. This Control Ring Pulse returns ES left and pulls ER right. The ER or Result Operation is shown on plate 15.

ZERO FACTOR

Plate 26C

Zero Factor is the term employed in Multiplication or Division Process when either or both factors are zero. A special circuit is required to handle Zero Factor because the method the Computer uses in Multiplication or Division of digits is not prepared to handle a zero value. For example if the M'd is zero there is no way to stop shifts when the M'd is shifted until the first digit arrives in 11M.

There are three basic Zero Factor operations: M'd is zero, S'r is zero or both are zero. The basic theory of operation is the same in either Multiplication or Division.

The general procedure followed in Zero Factor is as follows. If either or both factors are zero, the result must be zero. Therefore, if the Proof M'd Numerical Registration is zero the step is repeated. This repeat is a form of proof to see if the Proof M'd is again zero. If the repeat of the step shows the Proof M'd to again be zero a Step Advance can be realized to progress to the next step.

All cases of Zero Factor in Multiplication and $Ø \div N$ are numerically a true zero. $Ø \div Ø$ is an indeterminate and $N \div Ø$ is infinity. The Computer cannot give either result so zero is given instead. In case the Programmer does not wish to accept a zero answer for either or both cases ($N \div Ø$, $Ø \div Ø$) the alternative of Stop or Sort and Trip may be employed as shown on plate 27 . It is common practice in programming to use a $Ø \div Ø$ step plugged to Stop to indicate a card out of sequence, etc.

Operation

$N \div Ø$ or $N \times Ø$

The only time this circuit is affected is during the registration of a zero value. This condition first arises during the S'r Numerical Registration. At this time the M'd has been shifted into the M Section leaving the A Section zero. After the S'r Registration the A Section is still zero and that is where this circuit begins to function.

Trigger R1 is returned left following the S'r cycle of RIG. The LP of R1 goes low to the RC of CD, kicking CD right. After 50 us CD returns left sending its LP low to the LC of CDA. The LP of CDA releases a positive pulse to the LC of the open Gate ØF2. (Either x or ÷ Process lowers the plates of PIMD. The LI of PPI is low so the LP of PPI is high to the LI of ØF2, opening the Gate). The LP of ØF2 releases a negative pulse to the RP of OF1, triggering OF1 right. The LP of ØF1 goes high to the LC of Gates ØF3, ØF4 and ØF5. The RC of ØF4 is also pulsed by this high level.

The input to the three Gates, ØF3, ØF4 and ØF5 is controlled by the Zero Check Line. Since the S'r was zero, the A Section, at this time has no value. The LI of Ø9C has a low input so both Ø9C and Ø9C1 are cutoff. The LP of Ø9C and Ø9C1 go high to the LI of ØF4. The LD of ØF4 taps off high to the LD of ØF3 and ØF5. All three Gates now have high grids. Each Gate also has a cathode control, EMK, ESK or ERK. Since the Computer is functioning during ES time, only the ESK line is low. Therefore, only Gate ØF4 has both a high grid and low cathode which is required to enable a

Gate to be open. The RI of ØF4 is low since ØMD is left. The LP of ØF4 releases a negative pulse to the RP of ØSR, triggering ØSR right. The LP of ØSR goes high to the LI of ØEZ1, opening the Gate, and to the RC of ØF2. The RP of ØF2 releases a negative pulse to the RP of ØFS, kicking ØFS right.

The LP of ØFS goes high to the LC of ØESP. The LP of ØESP releases a negative pulse to the Control Ring, returning ES left, and to the RC of ØFD1, kicking ØFD1 right. ES returning left triggers ER right. The RP of ØFS also goes low to the RP of ØFZD, kicking ØFZD right. ØFZD is a 5 MS delay to replace EMZ guard delay. The LP of ØFZD goes high to the RI of Ø9M and RBK. The RP of Ø9M goes low to the LP of DMP to prevent the Proof M'd Numerical Registration until Storage has been cleared. RBK prevents further RIG cycles until EPM time.

After 25 us ØFS returns left. The RP of ØFS returns high to the RC of ØESP. The RP of ØESP releases a second negative pulse to the Control Ring. This second pulse returns ER back left. ER returning left kicks EDPZ right.

ØFD1 returns left sending its LP low to the LC of ØF1, triggering ØF1 back left.

By pulsing ER within 25 us the Computer performed no normal Result functions as shown on plate 15. There was no Storage Set Pulse so once Storage has been cleared its value will remain zero.

The Computer now proceeds through the B-2 Zeroize (EPZ) and then EPM is brought right. At the completion of the Proof M'd Numerical Registration Trigger R1 returns left. The LP of R1 goes low to the RC of CD, kicking CD right. After 50 us CD returns left sending its LP low to the LC of CDA. The LP of CDA releases a positive pulse to the LC of tne open Gate ØF2. The LP of ØF2 releases a negative pulse to the RP of ØF1, triggering ØF1 right. The LP of ØF1 goes high to the LC of Gates ØF3, ØF4 and ØF5.

The value in the A Section is zero so the grids of the three Gates are high. The Computer is in EPM time so the ERK line is low. Only Gate ØF5 now has a high grid and low cathode. The LP of ØF5 releases a negative pulse to the RC and LC of ØRS, triggering ØRS right. The LP of ØRS goes high to the LC of the closed Gate ØEZ (ØMD is left) and the LC of the open Gate ØEZ1 (ØSR is right). The LP of ØEZ1 releases a negative pulse to the RP of EZ to restart the step over again.

EZ going right initiates a B-2, B-5 Zeroize. This Zeroize will return all Triggers left except ØRS which remains on the right.

The repeat of this step follows the same procedure as previously explained. The only exception occurs during EPM when ØF5 again releases a negative pulse to the RC and LC of ØRS.

ØRS was still on the right so the negative pulse from ØF5 to the RC and LC of ØRS, triggers ØRS back left. The RP of ØRS goes high to the RC of the closed Gate ØEZ and the RC of the open Gate ØEZ1. The RP of ØEZ1 releases a negative pulse to the RP of EGD, kicking EGD right. EGD going right will advance the Computer into the next step as shown on plate 11.

In the Division Process the Programmer may want to prevent any continued calculation from a N ÷ Ø step. This can be accomplished by plugging the N ÷ Ø hub on the Program Plugboard to Stop or Sort. The control on this Plugboard hub is as follows.

The Process being Division lowers the grids of ØFD3. In N ÷ Ø, Trigger ØSR is right

and ØMD is left. The LP of ØMD is low to the LI of ØFR1. The RP of ØSR is low to the RI of ØFR1. The plates of ØFR1 are tied to the LP of ØFD3. All three plates are cutoff so they are free to go high to the RP of the diode ØFM. The RK of ØFM goes high to the N ÷ Ø hub on the plugboard. Further explanation of this control is shown on plate 27 .

Ø ÷ N or Ø x N

The first time a zero value is registered is during the M'd Numerical Registration. The problem encountered with a zero value for the M'd is stopping shifts. To prevent continuous shifting an Artificial One will be inserted for this purpose. The problem cannot be allowed to continue because a false answer would result.

The completion of the M'd cycle of RIG is indicated by the return of Trigger R1. The LP of R1 returns low to the RC of CD, kicking CD right. After 50 us CD returns left sending its LP low to the LC of CDA. The LP of CDA releases a positive pulse to the RC of the open Gate ØF2. (This Gate is opened by the low process through PIMD and out high through PPI). The LP of ØF2 releases a negative pulse to the RP of ØF1, triggering ØF1 right.

The LP of ØF1 goes high to the LC of Gates ØF3, ØF4 and ØF5. Since the value in the A Section is zero at this time the LI of Ø9C is low. The LP of Ø9C and Ø9C1 will be high to the LI of ØF4. The LD of ØF4 taps off high to the LD of ØF3 and ØF5. All three Gates have high grids. The Computer is in EM time so the EMK line is low. This means that only Gate ØF3 has both a high grid and low cathode.

The LP of Gate ØF3 releases a negative pulse to the RP of ØMD, triggering ØMD right. The LP of ØMD goes high to the LI of ØF4, conditioning this Gate. The LD of ØF4 taps off high to ØEZ, opening this Gate. The LP of ØMD also goes high to the RC of ØF3. The RP of ØF3 releases a negative pulse to the 11A Accumulator Odd Line. This gives Accumulator 11A a value of one. This value of one will be used to stop shifting, during ES, when this digit reaches 11M.

EM is returned left by a Control Ring Pulse which also kicks ØFD1 right. After 25 us ØFD1 returns left sending its LP low to the LC of ØF1, triggering ØF1 back left. EM returning left triggers ES to the right. The S'r is a numerical value so the Zero Factor circuit supposedly should not be affected. Since an artificial one value was inserted during EM the problem cannot be allowed to continue in a normal pattern.

The completion of the S'r RIG pulses CD, which through CDA and open Gate ØF2, triggers ØF1 right. The LP of ØF1 goes high to the LC of ØF3, ØF4 and ØF5 and also to the RC of ØF4. The A Section is no longer zero (S'r RIG) so the LI of Ø9C is high. The LP of Ø9C and Ø9C1 is low to the LI of ØF4. The LD of ØF4 taps off low to the LD of ØF3 and ØF5. The grids of all three Gates are low so the Gates are closed. The RI of ØF4 is high (ØMD is right) and, since the ESK line is low during ES, the right side of ØF4 is open. The RP of ØF4 releases a negative pulse to the RP of ØFS, kicking ØFS right.

The operation of ØFS through ØESP results in two Control Ring Pulses being released. These Control Ring Pulses return ES to bring ER right and 25 us later ER is returned left to bring up EDPZ.

The release of the low level from the RP of ØFS kicks ØFZD. ØFZD is a guard delay

to prevent reading out from Storage during EPM before the Zeroize of Storage is completed.

After the B-2 Zeroize EPM goes right. This operation is fully explained under the N ÷ Ø write up. The only exception is that the left side of Gate ØEZ is used instead of the left side of Gate ØEZ1.

The step is then repeated following the same procedure as previously stated. When ØRS is pulsed the second time the RP of ØRS pulses the RC of ØEZ. ØEZ releases a negative pulse to the RP of EGD to advance to the next step.

No provision is made in Ø ÷ N to prevent the Step Advance Operation since Ø ÷ N is mathematically zero.

Ø ÷ Ø or Ø x Ø

This operation is a combination of N ÷ Ø and Ø ÷ N. Combining these two writeups will explain this operation.

In the Division Process the Programmer may want to prevent any continued calculation from Ø ÷ Ø step. This can be accomplished by plugging the Ø ÷ Ø hub on the Plugboard to Stop or Sort. The control on this Plugboard hub is as follows:

The Process being Division lowers the grids of ØFD3. In Ø ÷ Ø, Triggers ØMD and ØSR are right. The RP of ØMD is low to the LI of ØFR2. The RP of ØSR is low to the RI of ØFR1. The RD of ØFR1 taps off low to the RD of ØFR2. The plates of ØFR2 and the RP of ØFD3 are tied together. All three plates are cutoff so they are free to go high to the LP of diode ØFM. The LK of ØFM goes high to the Ø ÷ Ø hub on the Plugboard. Further explanation of this control is shown on plate 27.

In the event the Computer does not show Zero Factor on the repeat of the step the Trigger ØRS would still be right. ØRS would be returned left by the ESI pulse through the diode ØRSZ. Any time the step is repeated by the Timer, stage MC3 would also return ØRS left as shown on plate 20.

PROCESS	M-SECTION CALC. DEC. REF. POINT											A-SECTION N ÷ Ø N X Ø INPUT											COUNTER		
	11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	DEC	M-D	CCT
MINIDEND											11						2.	2							
SUBVISOR											16														
STORAGE DECIMAL											16														
1. CALC. ZEROIZED																									
2. M'D DEC COMPL.																							11		
3. M'D NUM REG.																	2	2					11		
4. S'R DECIMAL																	2	2					5		
5. CONSTANT 17																	2	2					Ø		
6. SHIFT M'D TO 11M	2	2																					16	12	CT11
7. S'R TRIAL SUB'T	2	2									1												16	12	CT11
8. CONTROL RING																									CT11
9. B-2 ZEROIZE	2	2									1												16	Ø	CT11
10. PR. M'D DEC COMPL.	2	2									1												Ø		CT11
11. PR M'D NUM REG	2	2									1												Ø		CT11
12. EZ	0	0									0												Ø		Ø
13. M'D DEC COMPL																							11		
14. M'D NUM. REG.																	2	2					11		
15. S'R DECIMAL																	2	2					5		
16. CONSTANT 17																	2	2					Ø		
17. SHIFT M'D TO 11M	2	2																					16	12	CT11
18. S'R TRIAL SUB'T.	2	2									1												16	12	CT11
19. CONTROL RING																									CT11
20. B-2 ZEROIZE	2	2									1												16	Ø	CT11
21. PR M'D DEC COMPL.	2	2									1												Ø		CT11
22. PR M'D NUM. REG.	2	2									1												Ø		CT11
23. EGD																									Ø

PROCESS	M-SECTION CALC. DEC. REF. POINT											A-SECTION Ø ÷ N / Ø X N INPUT											COUNTER		
	11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	DEC	M-D	CCT
MINIDEND											16											0			
SUBVISOR											11						2	2							
STORAGE DECIMAL											16														
1. CALC. ZEROIZED																									
2. M'D DEC. COMPL.																							6		
3. M'D NUM. REG												1											6		
4. S'R DECIMAL												1											17		
5. CONSTANT 17												1											12		
6. SHIFT M'D TO 11M	1																						1	12	CT11
7. 1st S'R TRIAL SUB'T	1										2	9	9	9	9	9	7	8					1	12	CT11
8. CONTROL RING																									CT11
9. B-2 ZEROIZE	1										2												1	0	CT11
10. PR. M'D DEC. COMPL	1										2												7		CT11
11. PR M'D NUM. REG	1										2												7		CT11
12. EZ	0										0												0	0	Ø
13. M'D DEC COMPL																							6		
14. M'D NUM. REG												1											6		
15. S'R DECIMAL												1											17		
16. CONSTANT 17												1											12		
17. SHIFT M'D TO 11M	1																						1	12	CT11
18. 1st S'R TRIAL SUB'T	1										2	9	9	9	9	9	7	8					1	12	CT11
19. CONTROL RING																									CT11
20. B-2 ZEROIZE	1										2												1	0	CT11
21. PR M'D DEC COMPL	1										2												7		CT11
22. PR M'D NUM. REG.	1										2												7		CT11
23. EGD																									Ø

PROCESS	M-SECTION CALC. DEC. REF. POINT											A-SECTION Ø ÷ Ø / Ø x Ø INPUT											COUNTER		
	11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	DEC	M-D	CCT
MINIDEND											16														
SUBVISOR											16														
STORAGE DECIMAL											16														
1. CALC. ZEROIZED																									
2. M'D DEC. COMPL.																							6		
3. M'D NUM. REG.												1											6		
4. S'R DECIMAL												1											Ø		
5. CONSTANT 17												1											17		
6. SHIFT M'D TO 11M	1																						6	12	CT11
7. S'R TRIAL SUB'T	1										1												6	12	CT11
8. CONTROL RING																									CT11
9. B-2 ZEROIZE	1										1												6	Ø	CT11
10. PR. M'D DEC. COMPL.	1										1												12	Ø	CT11
11. PR. M'D NUM. REG.	1										1												12	0	CT11
12. EZ	0										0													Ø	
13. M'D DEC. COMPL.																									
14. M'D NUM. REG.												1											6		
15. S'R DECIMAL												1											Ø		
16. CONSTANT 17												1											17		
17. SHIFT M'D TO 11M	1																						6	12	CT11
18. S'R TRIAL SUB'T	1										1												6	12	CT11
19. CONTROL RING																									CT11
20. B-2 ZEROIZE	1										1												6	Ø	CT11
21. PR. M'D DEC. COMPL.	1										1												12		CT11
22. PR. M'D NUM. REG.	1										1												12		CT11
23. EGD																									Ø

SORT OR STOP: - (N ÷ Ø or Ø ÷ Ø)

Plate 27C

Sort (N ÷ Ø or Ø ÷ Ø)

A problem of N ÷ Ø or Ø ÷ Ø in Zero Factor as shown on plate 26 may be plugged to Sort on the Constant and Program Plugboard. The control on diode ØFM is shown on plate 26. The high level from either cathode of ØFM raises the LI of ARG and ARZ. The high input to ARG opens this Gate. The LP of ARZ goes low to the RI of ARG to close this Gate. The RD of ARG taps off low to the RB of ARM to block any pulses at the RC of ARM.

The completion of the Zero Factor step is signalled by pulsing EGD. The RP of EGD goes low to the RC of the Negative Pulse Amplifier ARG1. The RP of ARG1 releases a positive pulse to pin 6 and out pin 9 of ARA1 to the RC of ARM and the RC and LC of ARG. The positive pulse is rejected at the RC of ARM and ARG but accepted at the LC of ARG. The LP of ARG releases a negative pulse to the RP of ART, triggering ART right. ARG and ARM rejecting the positive pulse prevents branching to a new step, ESI, or zeroizing the present Step Trigger, ESZ.

The LP of ART goes high to the LC of ARM. The LP of ARM releases a negative pulse to the RC of AGT on plate 28 to initiate the 20 MS Guard Delay used in Function steps.

The LP of ART also goes high to the LI of ARA1. The LD of ARA1 taps off high to the LD of ARA2, LD of ARA3 and RI of AGTZ. The stages with the high grids will do the following:

1. ARA1 - The thyratron in ARA1 will fire when the Ready Line is grounded and energize the Sort Pulse Relay which is shown on plate 55.

2. ARA2 - The thyratron in ARA2 will fire when the Ready Line is grounded and energize the Trip Pulse Relay which is shown on plate 54.

3. ARA3 - The plates of ARA3 go low to the LI of AP3 shown on plate 30 resulting in cutting off the Timer.

4. AGTZ - The RP of AGTZ goes low to the RI of ARG which taps off low to the RB of ARM. This low level on ARG and ARM is necessary in case the Trip Signal originated clears Selectors which might remove the high level from the LI of ARZ. For example, opening the Division Process Call would do this or breaking the Zero Factor Sort Line itself.

The Computer will not continue to calculate but instead the card will be ejected and sorted.

Stop (N ÷ Ø or Ø ÷ Ø)

A problem of N ÷ Ø or Ø ÷ Ø in Zero Factor as shown on plate 26 may be plugged to

Stop on the Constant and Program Plugboard. The control on diode ØFM is shown on plate 26. The high level from the LK of ØFM raises the LI of ARY. The high level from the RK of ØFM raises the RI of ARZ. The RP of ARZ and LP of ARY are tied together so either N ÷ Ø or Ø ÷ Ø results in lowering the RI of ARG. The RD of ARG taps off low to the RB of ARM.

The completion of the Zero Factor step is signalled by pulsing EGD. The RP of EGD goes low to the RC of the Negative Pulse Amplifier ARG1. The RP of ARG1 releases a positive pulse to pin 6 and out pin 9 of ARA1 to the RC of ARM and RC and LC of ARG. The positive pulse is rejected at all points due to low grid levels. The rejected pulse prevents branching to a new step, ESI, or zeroizing the present Step Trigger, ESZ. The Computer cannot continue calculating so the operator must manually remove the card.

The Step Switch on the PTP, when operative, will put a high level to the RI of ARY. The RP of ARY goes low to the RI of ARG which prevents branching and zeroize as explained above.

OUTPUT CONTROL: - Chassis #1 & #2

Plates 28C, 29C & 30C

The various special Function Program and Step Triggers are located in Output Control Chassis - they are in OCL1 -

(a) APT1 through APT4 controlling Select I through Select IV.

(b) AAT1 and AAT2 controlling Punch Actuator Set I and II.

(c) AST1 and AST2 controlling Punch Sort I and II.

(d) ACT controlling Program Storage Clear.

(e) ATT controlling Punch Trip.

and in OCL2 -

(f) ART which controls the Zero Factor Reject Operation for Sort and Trip.

(g) AGT initiates the guard time for the foregoing stages "b" through "f" except "d" when the Punch Ready Signal is present.

The branching into and out of "a" through "e" is exactly like the branching for the Numerical Steps. One function only of each type is described for the Triggers themselves.

Sort I, Set I and Clear Operation (Plate 28)

This plate shows the circuitry of three of the Function Steps. Each Function Step can be branched In from either a Numerical Step or a different Function Step. The Out branch from these Function Steps can go to either a Numerical Step or a different Function Step. Each Function Step is 20 MS in duration. In each step the Function is separate from the delay and Out Branch of the Step. This leaves the possibility of branching out of a Function Step without performing the Function.

Sort I

Branching In the Sort I Step lowers the LI of the Diode Gate ASG. The ESI pulse to ASG causes a negative pulse to be released from the LP of ASG to trigger AST1 right.

The LP of AST1 goes high to the LI of ASD. The LP of ASD goes low to pull down the Sort I Out Line to condition the branching to the next step. The LD of ASD taps off high to the LD of thyratron ASA1. This fires the thyratron ASA1 resulting in energizing the Sort Pulse Relay in the Punch. The thyratron ASA1 cannot fire until the Ready Line, Cam C, is closed.

The LP of AST1 also goes high to the LC of ASM. The LP of ASM releases a negative pulse to the RC of AGT, triggering AGT right. This starts the Guard Delay of the step which is explained under a separate heading.

Set I

Branching In the Set I Step lowers the LI of the Diode Gate AAG. The ESI pulse to AAG causes a negative pulse to be released from the LP of AAG to trigger AAT1 right.

The LP of AAT1 goes high to the LI of AAD. The LP of AAD goes low to pull down the Set I Out Line to condition the branching to the next step. The LD of AAD taps off high to the LD of AAR. The high grid of AAR and the Ready Line, Cam C, being closed, allows the LP of AAR to go low to the RC of AAF1, kicking AAF1 right. AAF1 has a 10MS delay. While AAF1 is right its LP goes high to the LI of AAK1. The K-AAK1 goes high to the Set I Common on the Plugboard. The operation of this circuit on the Storage Bits is shown on plate 10 . After 10MS AAF1 returns left and the Set Pulse is completed.

The LP of AAT1 also goes high to the LC of AAM. The LP of AAM releases a negative pulse to the RC of AGT, triggering AGT right. This starts the Guard Delay of the step which is explained under a separate heading.

Clear

Branching In the Clear Step lowers the LI of the Diode Gate ACG. The low In line also lowers the LI of ASC. The K-ASC goes low to the Clear Common on the Plugboard. The additional conditioning of the Storage Circuit is shown on plate 10.

The ESI pulse to ACG causes a negative pulse to be released from the LP of ACG to trigger ACT right. The RP of ACT goes low to the LC of ACI. The LP of ACI releases a positive pulse to the RC of ACI. (ACI' operates in parallel with the right side of

ACI). The RP of ACI releases a negative pulse to the LC and RC of all MC Diode Gates. These Gates were conditioned by the K-ASC.

The LP of ACT goes high to the LI of ACM. The LP of ACM goes low to pull down the Clear Out Line to condition the branching to the next step. The LP of ACT also goes high to the RC of ACM. The RP of ACM releases a negative pulse to the RP of AGF1 to start the Guard Delay of the step which is explained under a separate heading.

Guard Delay of Function Steps

All Function Steps, Set, Sort, Select, Clear and Trip, use the same Guard Delay. Those Functions, which directly operate in the Punch, start with AGT for Ready Line protection.

Assuming AGT is right the LP of AGT goes high to the LI of AGD. AGD has a Ready Line control on its cathode but when the Ready Line is closed AGD conducts. The LP of AGD goes low to the RC of AGF1, kicking AGF1 right. AGF1 has a 10MS delay and, on its return left, the LP of AGF1 returns low to the RC of AGF2 kicking AGF2 right. The LP of AGF2 goes high to the LC of AGTZ. The LP of AGTZ releases a negative pulse to the LP of AGT, returning AGT left. AGT is normally returned left by this method instead of ESZ in order to set up this Trigger for a possible immediate Function Step following this one.

After 10MS, AGF2 returns left, and the RP of AGF2 goes high to the RC of AGA. The RP of AGA releases a negative pulse to the RC of ARG1. The plates of ARG1 release a positive pulse to the RC of ARM and LC and RC of ARG. The RI of ARG and RB of ARM are high except when the PTP Switch is in Step or ØF (N ÷ Ø or Ø ÷ Ø Stop) is present. The RP of ARG releases a negative pulse to the RC of ESIA and LC of ESZA creating an ESZ and ESI Pulse. The RP of ARM releases a negative pulse to the RP of EZ to start the next step. A more detailed explanation of the controls on ARG are shown on plate 27.

Select Step (Plate 29C)

The purpose of the Select Step is to energize Selector Relays by means of a Select Thyratron. No control holes are necessary as the Program Branching Control governs when the Select step is to be used. There are four separate Select Steps, I, II, III and IV, each performing separate but similar functions, energizing Selector Relays. The thyratrons are fired in their Select Step but are generally extinguished by Punch Control. The cathode of each Select Thyratron is returned to ground through the Select Cam and the energized Manual Clear Relay Contacts or the energized Select Control Relay Contacts in series with the de-energized Trip Pulse Relay Contacts and the energized Manual Clear Relay Contacts.

The Manual Clear Relay is normally energized and only drops out if B+ is removed or in a Trip Step with the Punch Motor turned off. A Manual Clear will also de-energize the Manual Clear Relay. At 324°Punch time the Select Cam closes, then at 75° the Trip Pulse Relay de-energizes and at 135° the Select Control Relay energizes. At 200° the Select Cam opened so a Trip Pulse will break the cathode circuit when the Trip Pulse Relay energizes. The Select Thyratron can also be extinguished if the plate is grounded by Control Common or Selector Hold. At this time the Selector Relays do not drop out and the PTP neon indicator stays fired even though the

thyratron is technically extinguished. The Thyratron can also be extinguished if its load (relay) is removed.

It is not necessary to fire the thyratron in order to branch out of a Select Step. The function of the thyratron is independent from the branching. One Select Thyratron can pull in all the Selector Relays if the program requires such an application. Each Select Thyratron plate has a six hole bus on the plugboard from which the Selector Relay Pull Up is plugged. An additional bus may be used if more than six Selector Relays are to be energized.

Each Selector Relay has its own half wave 115 volt DC Power Supply. The half wave gives high voltage for pull in and lower voltage for holding. The Power Supply for these relays are in the Selector Power Chassis (SEP). The Select Thyratrons are located under the meter panel in the Power Control end of the Computer.

Operation

A branch, + or -, into a Select I Step is indicated by lowering the LI of diode APGA. The ESI pulse to APGA releases a negative pulse at the LP of APGA to trigger APT1 right. The LP of APT1 goes high to the LI of APD1 and LC of APMA. The LP of APD1 lowers the Select I branch Out Line. The LP of APMA releases a negative pulse to AGF1 to give the 20 millisecond Guard Delay of the step as shown on plate 28.

The RP of APT1 goes low to the RI of APD1. The RP of APD1 goes high to the grid of the Select I Thyratron causing this thyratron to fire. Any Selector Relays whose Pull Up is plugged will be energized. The indicator neon on the PTP will fire and remain fired until the thyratron is extinguished.

The Manual Clear will Zeroize the Select Step Triggers. This is necessary to prevent leaving a Select Thyratron fired if the Computer hangs up in a Select Step and it is desired to Clear and Restart the problem.

Trip (Plate 30C)

Trigger ATT is pulled right through ACG when branching into Trip. ATT raises the left grid of ATM1 to fire the Thyratron and operate the Trip Pulse Relay in the Punch when the Ready Line and cathode go to ground. The left divider of ATM1 also raises the grids of ATA which operates the Reproduce Power Relay in a Reproduce Operation. The high from the LP of ATT to the RC of ATM2 causes the RP of ATM2 to release a negative pulse to AGT to start the Guard Delay for this step as shown on Plate 28 . The plates of ATA also operate AP3 to pulse the master control on the Timer left since the Trip Signal indicates the end of the problem. The input from the plates of ATA into APC1 is for certain test conditions. Whenever a Trip Signal is received, the left grid of APC1 is cut off. The right grid of APC1 is controlled by the Punch Motor Switch. When the Motor Switch is On, a +70R Supply is available to the right grid so APC1 remains conducting during a Trip. When the Motor Switch is Off, the right side of APC1 does not conduct; therefore, when a Trip Pulse occurs, APC1 is cut off on both sides causing the Manual Clear Relay to de-energize. This relay dropping out will Zeroize all 12 Storages, break Selector Hold and the Control Common. The same result, APC1 cut off, can be accomplished manually. When the Clear Switch on the PTP or Unit and Clear Switch on the Punch is operated, the Cathode Circuit of APC1 is broken and the tube stops conducting.

When the Trip Pulse is received with the Motor Switch Off and the Timer Cut-off blocked, a Test Problem can be run in the Calculator which will be completely cleared every time a Trip Pulse occurs. All Selector Relays will drop out and all Storages will be cleared. Since the Timer Cut-off is blocked, problem repeat being plugged will cause calculation to start from the beginning. ATT may be operated directly from the Punch Non-Calculate Cam Switch through the filter of ATR for the purpose of tripping the first card fed through the sensing cycle for that card.

SELECTOR RELAY CONTROL

Plate 31C

This circuit shows the various controls available to pull in or hold in Selector Relays and the Select Thyratrons. The Common Busses are located on the Field Plugboard and the Selector Hold Bus is located on the Program Plugboard. The Manual Clear Relay is located in the Power Control end of the Computer. The Select Cam, Select Control and Trip Pulse Relays are located in the Punch.

Control Common

The Control Common and Select Thyratron cathodes are returned to ground through the energized Manual Clear Relay contacts and either the Select Cam or the energized Select Control Relay contacts in series with the de-energized Trip Pulse Relay contacts.

The Control Common is normally broken when the Trip Pulse Relay is energized. This gives the Selector Relays the maximum drop out time before the sensing switches break.

When a card is manually released, Card Release Operation, the Trip Pulse Relay is not energized. The Select Control Relay, being cam controlled, will therefore break the Control Common before the sensing switches break.

Selector Hold

The Selector Hold Bus is returned to ground through the energized Manual Clear Relay contacts. The Manual Clear Relay remains energized from card to card so therefore the Selector Hold is a constant ground. Use of the Selector Hold Bus enables a Selector Relay to be held in from card to card.

Delayed Control Common

The Delayed Control Common is returned to ground during the short interval after the Trip Pulse Relay energizes until the Select Control Relay de-energizes. The purpose of this line is to delay using the Control Hole in a card until that card has been completely calculated (Trip Pulse). A Selector Relay which is energized by the Delayed Control Common will not remain energized until the following card is sensed unless Selector Hold is used.

TEST COUNTER

Plate 32C

The Test Counter is controlled in its operation from the Test Counter Panel which is located in the center rear of the Computer. The purpose of the Counter and Panel is to assist in servicing the Computer. By use of the Counter and Panel it is possible to stop the Computer calculation after a predetermined quantity of shifts, carries or RIGS. The operation of the Off-On switch enables the Counter to be effective. The Panel can be set to stop the Computer in any calculating step by use of the Step switches.

Input

The source of input to the Test Counter is controlled by the setting on the Panel Stop Switch.

Post or Pre RIG - RIG1' in the RIG (plate 5).
Pre SIG - SK2 in the Decimal Counter (plate 4).
Pre CIG - CSK in the Carry Input Generator (plate 3).

Output

The destination of output from the Test Counter is controlled by the setting on the Panel Stop Switch.

Post RIG - CX in Carry Input Generator (plate 3).
ØF2 in Zero Factor (plate 26).
Pre RIG - RB in Sign Bias (plate 43).
PMDR in Multiplication and Division (plate 23 and 25).
Pre SIG - SMG in the Decimal Counter (plate 4).
Pre CIG - SCK1' in Carry Input Generator (plate 3).

The Test Counter has a capacity of 400. At a count of 400 all Count Triggers are left. Trigger TB is right raising the cathode of TK through the Off-On switch. The Counter, therefore, becomes effective when its count becomes 400.

There are three Count Set switches on the Test Counter Panel, Units, Tens and Hundreds. The Count Set switches are set to a value which represents the number of pulses permitted before the Test Counter becomes effective. For Example: The Computer is to be stopped before the 21st shift pulse is released. The Stop switch is set to Pre SIG. The Count Set switch has a zero Unit setting and a two tens setting. The TCR is set at Pre SIG 20. This setting indicates that 20 shift pulses may occur prior to the TCR reaching 400.

The value set in the Count Set switches is placed into the Counter as the complement of 399. If the value in the switches is 20, the Counter value would be 399-20 or 379. This complement value is placed into the Counter by the B-5 Zeroize. The letters under the Counter Triggers refer to connections made to the Panel for use with the B-5 Zeroize. This Zeroize is effective on the Counter whether the Off-On switch is effective or not. Even though the Counter has a capacity of 400 the Complement of 399 is placed in the counter. The operation of DEA, Decimal Registration, adds one

more to the Counter bringing its value to the complement of 400. This is necessary in case the Count Set is set at zero. If the complement of 400 were used the complement of zero is 400 which to the Counter would be zero. Using 399 instead, enables the Counter to go to 400 by DEA which then makes the Counter 400 before any Stop switch pulses can occur.

The Test Counter Triggers have the following values.

Digit	4	2	$\overline{2}$	1
1				1
2			$\overline{2}$	
3			$\overline{2}$	1
4		2	$\overline{2}$	
5		2	$\overline{2}$	1
6	4		$\overline{2}$	
7	4		$\overline{2}$	1
8	4	2	$\overline{2}$	
9	4	2	$\overline{2}$	1
0				

Overcarry occurs from Units to Tens and from Tens to Hundreds.

The Test Counter is only effective in the step set on the Step switches. When the selected step is reached the LP of this selected Step Trigger goes high to the LB of TSA. The LP of TSA goes low to the RI of TG, a Cathode Follower on the right side. This lowers the cathode of Gate TG. When DEA returns left its LP goes low to the RC of TS, triggering TS right. The LP of TS goes high to the LI of TG, opening the Gate. The LP of TS also goes high to the RC of TSA. The RP of TSA releases a negative pulse to the RC and LC of T1 to increase the count in the Test Counter by one. This brings the count in the Counter to the complement of 400.

Gate TG being open allows the selected pulses from the Stop switch to be accumulated in the Counter.

The SD position on the TCR Panel is connected to the LP of TSP. When the Computer is in the step selected by the Step switch the LP of TSP goes low to the SD jack. This SD jack can be plugged into the oscilloscope using the (-) input. This is the same as triggering from a Step Trigger. The TCR input on the Sweep Delay is not required.

VOLTAGE ABNORMALITY DETECTOR

Plate 33C

The purpose of the VAD Chassis is to provide:

(1) a visual indication on the Operator's Panel which will persist until manually reset

(2) and stop the operation of the Punch

whenever the power line voltage variations cause the D.C. Supply voltages to exceed a predetermined safe operating range. The circuit has been made failsafe by arranging it so that an indication is provided not only when the supply voltages exceed a safe operating range, but also in the case of a D. C. supply voltage failure or an open interlock switch.

The circuit contains a Detector, Mixer, Inverter and an Output stage. The Detector consists of two self-extinguishing Thyratron Circuits, THY1 and THY2. The Control Grid Resistor of each Thyratron is returned to individually adjustable reference voltages. By adjusting these reference voltages, an output indication can be provided at any desirable plus or minus supply voltage variation. The power supply voltage -150, which is monitored, is applied to the cathode of Thyratron, THY1, and to the control grid of Thyratron, THY2, so that any variation in the power supply voltage appears directly in both of the Thyratron grid-to-cathode circuits but of opposite polarity. If the magnitude of the supply voltage should increase, the grid-to-cathode voltage of Thyratron, THY1, will become more positive while the grid-to-cathode voltage of Thyratron, THY2, will become more negative. Should the magnitude of the supply voltage increase beyond the safe operating limit (150 + 8%) Thyratron, THY1, will fire. If the magnitude of the supply voltage should decrease, the grid-to-cathode voltage of Thyratron, THY2, will become more positive while the grid-to-cathode voltage of Thyratron, THY1, will become more negative. Should the magnitude of the supply voltage decrease beyond the safe operating limit (150 - 8%), Thyratron, THY2, will fire.

Operation

The plates of the Thyratrons are direct coupled to the grids of a Mixer stage, MXR. Both triodes of the Mixer stage are normally conducting. When a Thyratron fires, one of the triodes of the MXR stage will become cut-off. This will cause the Inverter stage, INV, which is normally non-conducting to go into conduction. The Inverter plates now being low, cut-off the normally conducting Output stage, OTP, and the relay in the plate circuit of OTP becomes de-energized and its contacts provide the necessary output. The relay is then locked-out by one of its own contacts so that it cannot be energized again until the Clear Punch Switch, located on the Operator's Panel in the Punch Unit, or Service Switch under the TCR Panel, is closed.

When the Power supply voltages exceed the safe operating limits, one of the Thyratrons will fire and then extinguish itself, the red Voltage Indicator Light on the Operator's Panel will go On and the Punch Operation will stop. The machine will remain in this condition until the operator manually resets the VAD with the Clear

Punch Switch. If the operator tries to reset the VAD while the line voltage is still beyond the safe operating limit, the red Voltage Indicator Light will go out while the Clear Punch Switch is closed, but it will immediately come back on when the switch is released indicating an abnormal voltage condition. If the line voltage had come back within the safe operating range and then the operator tries to reset the VAD, the red Voltage Indicator Light will go out when the Clear Punch Switch is closed and it will stay out when it is released indicating that the machine is now ready for normal use.

The relays affected by the +150 volt supply to the punch are:

K2	B+ Failure
K17	Select Control
K18	Calc. In Progress
K8	Secondary Reproduce
K16	Trip Pulse
K7	Sort Pulse
K211	Reproduce Power

AUTOMATIC CIRCUIT TIMER

Plate 34C

The Automatic Circuit Timer is a device to start the Computer over again in case an incorrect result or a transient pulse prevents the Computer from reaching the Trip or end of computation step. The Restart Signal is pre-controlled by the Programmer from the Plugboard. When plugged to Restart Step only the step in which the stoppage occurred is restarted. If plugged to Restart Problem the Automatic Timer has the same effect as the initial calculator Start Signal.

Circuit

The Restart Circuit is contained in the SCL Chassis, and operates as follows: Trigger EP3 is the master control which is kicked right by EP thru ESB1 to unlock the Timer on a calculator Start Signal. EP3 going right cuts off the right side of EPX. The left side of EPX is normally cut off, therefore the plate starts to rise, delayed by a large capacitor and high resistance plate load. If allowed to continue the plate voltage would rise far enough to fire two neons and apply a positive pulse to the two "C" inputs of EP5, however, EP4 is operated by EZ at the start of every step to recharge the capacitor in the plate circuit of EPX and prevent the neons from firing. The time for the plates of EPX to rise to the neon firing potential is approximately 300 milliseconds or roughly three times the duration of the longest problem. If a step is not completed within this time the pulse at the inputs of EP5 is passed thru the side which is held open by Plugboard Program which connects the bias input to ground. The left side of EP5 kicks EP to restart the problem and the right side of EP5 kicks EZ to restart the step. The Trip Signal through ATM1 or ATM2 in OCL returns EP3 to lock the Timer during the intervals between problem calculations.

In restarting a step, the left grid of EP4' is in parallel to the right grid of EP5 and therefore passes the same pulses as EP5 in order to return MC2 and ØRS in ØF should either be on the right. EP3 is also returned by the right side of EP4' when the Program Test Panel switches are in use. EP3C is a diode and RC circuit to insure that the Master Timer Trigger EP3 is on the left when the Computer D. C. voltages come on during the turn on period. The Minus Voltages coming on first apply a clamping voltage to the right grid of EP3 and then when the Plus Voltages follow, the cathodes of the diodes EP3C rise slowly above the plates and the diodes cease to conduct.

PROGRAM TEST PANEL

Plate 35C

In addition to serving to indicate the various digits in the Accumulator, elements called (Keyboard Biases), etc., the Program Test Panel provides the means to advance to any step of the program and to call V1, V2 or the Result as desired with its identity (N1---N36 or S1---S12,) decimal and such indicated. Briefly the sequence of operation of the switch is:

> Step, Clear, Start, then to Dial, if other than the first step is desired, or to Read. Then V1, V2 or R may be depressed in any order and more than once if desired.

The functions of the switches and associated circuitry are described.

Program Test Panel Operation

Step

The Automatic Circuit Timer is made inoperative by returning its Master Control Trigger EP3 whenever Switch #1 is placed in either the Step or Read positions. The opening of C2 or C3 Contacts allows the right grid of EP4^{1} to go from -90 Volts to ground and the right plate of EP4^{1}, in turn, clamps EP3 left.

The Step Zeroize and Advance Pulses ESZ and ESI are blocked by the right grid of ARY being raised to ground through C1 which, in turn, closes the right gate of ARG. Therefore, if a step is started, it can go to completion but no branching will take place. The Step Trigger for the step just completed will remain on the right.

Clear

C2 clears all the Storages and Select Circuits including the Program Board Hold Common by de-energizing the Manual Clear Relay. This Clear Operation may be performed regardless of the position of Switch #1.

Start

C1 calls for a normal Start Signal by grounding the Start Line. Contacts C2 allow EGD to operate the Program Test Check Trigger PT1. An incorrect result will fail to operate PT1 and prevent advancing from the step in which the error occured.

When Switch #1 is in the normal position, the Check Trigger has no function although the Check Indicator will light if switch #3 is held up. The Start Function is independent of Switch #1 and may be operated for trouble shooting with the Test Counter Panel.

Dial

When Switch #1 is in the Step position, the Dial is operated to give the desired number of steps to be advanced. The A Contacts on the Dial are closed while the Dial is operating to open the right Gate of PT2 which allows the Program Test Check Trigger PT1 to be operated. Dialing a 1 opens the Interrupter Contacts once allowing PT4 to go to the left. The .022 mfd. Capacitor, in ES13, prevents contact bounce in the Dial Interrupter Contacts from operating PT4 more than once per interruption.

The LA point of PT4 pulses the right grid of ARY below cut-off which, in turn, opens the right Gate of ARG. The left plate on the same negative pulse, operates PT3 which allows the Gate of ARG time to open. The return of PT3 to the left operates EGD through the left side of Gate PT2, which is held open on a correct result by PT1. EGD, in turn, initiates an ESI and ESZ pulse which returns the present Step Trigger and operates the next step in the branch.

The interval between pulses from the Dial is 200 milli-seconds which is longer than any step; therefore, the Computer can finish one step before an Advance Pulse is received to go to the next step.

Read

Contacts C3 (a & b) open to hold the Automatic Restart Control Trigger EP3 off the same as the Step position does.

The call for Storage is blocked to prevent clearing of the Result during the reading operation because Contacts C3 (c & d) allow the cathode of ERK to go to ground during Zeroize Guard Time, EZ, without calling the Result through the ERK bus.

C4 raises the cathode of CX through a 5K Resistor to block the Computer immediately after the RIG cycle called for to read V1, V2 or R. No carries are allowed if a Negative Factor is read on an Addition or Subtraction step; therefore, each negative digit will be the complement of 10 instead of 9.

V1

C3 closes to start the step by kicking EZ. MC2 is also returned to the left, if it should be on the right, in order that V1, V2 or the Result can be read with its proper sign on Addition or Subtraction.

V1 is registered into the Accumulator in the normal manner and left there since further operation of the step is blocked by Switch #1.

V2

C4 (d & e) open to prevent calling V1 through the EMK Bus. The ESK Bus is transferred by C4 (a, b, & c) to the cathode of EMK, therefore, V2 is substituted in place of V1 and is registered into the Accumulator

when EZ is operated by C3 (a & b) which close after C4 contacts have completed their transfer operation.

R

The Result Bus ERK which is disconnected from the cathode of ERK by the Read Switch is connected to the cathode of EMK by C4 (a & b) and then contacts C3 (a & b) close to register the Result into the Accumulator.

NOTE: When V1, V2 or R is depressed in an Addition or Subtraction Process, a minus value will be subtracted, resulting in its 10's complement being read on the PTP.

B2-B5 ZEROIZE

Plate 36C

Maintaining B5 at -90

The plate level of VTB5 governs the grid level on the right side of ZR5. This grid will control the cathode level. A rise or fall of this grid level will therefore affect the cathode level similarly. Since the left grid is maintained at -90 any change on the cathode will affect the left plate. The voltage level change on the left plate will be fed back to the control grid of VTB5 to adjust its conduction to bring its plate level back to -90.

B-5 Zeroize

When EZB5 goes right its LP, through the 220 uuf capacitor, will hold the grid of ZD52 high for approximately 60 us. The RP of EZB5, going low, will then cutoff ZD52 causing its plate to go high. Through the 1000 uuf capacitor, the grid of ZB52 is raised and the tube conducts. ZB52 conducting will disable ZR5 and also lower the control grid of VTB5 enough to cutoff this tube. This allows the plate of VTB5 to go to approximately ground potential and give the Zeroize effect.

Trigger Zeroize

B2 - Acc. (1A-11A incl.), M-D chassis, CCT except CT11
B5 - All other Triggers except those listed below
ESZ - Step Triggers, Function Triggers & AGT.
ESI - MC2, ØRS (also by step repeat)
EBS is Zeroized when ER goes right
EP3 - Trip Pulse, Clear Switch (Punch and PTP), Step & Read Switch (PTP)

KB RECOVERY AND DECIMAL CONTROL

Plate 37C

In the Computer, a means is provided in order to read the Numerical Value, Decimal Value and sign of the Numerical Value. A reading voltage is employed for this purpose and is called KB, Keyboard Bias.

There are 36 Elements in a full capacity Univac 120. Each Element may represent a Constant or a Card Field. Each Element has its own Decimal Location. It is not possible to use all the Elements at once so each must have its own reading voltage which can be called upon when required. This reading voltage is called KB.

There are 12 Storages in a Univac 120. Each Storage has its own associated circuitry which is referred to as KB but the voltage levels and the circuitry are not the same as that employed by Elements. When a specific Storage is called for the reference is made that the Storage KB is raised.

This plate gives an example of how KB is raised and shows the KB Recovery Operation. KB Recovery Operation is, as the name implies, used to lower a KB more rapidly than if it recovered from its own circuitry.

Operation

In the center of the plate are three circles labeled V1, V2 and R. V1 represents the first factor, Minidend (EM), V2 the second factor, Subvisor (ES), and R the Result, Storage (ER). As the various control circuits are encountered at various times V1, V2 or R will be pulled low. On this plate when V1 is pulled low the LI of KBA is lowered causing the LP of KBA to go high. Since V1 was plugged on the Program Board to N1 the KBA stage that is cutoff represents Element N1. The high level from the LP of KBA raises the grids and cathode of KB (1). This high level from the K-KB (1) is called Keyboard Bias. The high level from K-KB (1) goes to the following.

1. Plate of a diode located above the Plugboard Mechanism. The cathode of the diode is raised and is connected to the N1 Decimal Locator on the Plugboard. Here the N1 position is plugged to any of the 11 decimal positions. This plate uses a 2/1 decimal for N1. This 2/1 decimal is permanently connected to a group of neons, as shown, which are located on a panel located behind the DCL chassis. The KB level fires the neons which in turn condition the Decimal Counter Gates as shown on plate 4. There is one group of neons for each decimal position 11/10 to 1/0. Each Element uses one half of a diode. This diode prevents backfeed in the event two Elements use the same decimal.

2. The Plugboard position, marked Element Designators, at the N1 position. This high level at this point on the Plugboard is available to be wired to a Card Field or a Constant selection. If a Card Field is chosen the KB level is carried to the Punch Plugboard by means of a Transfer Line. If a Constant is chosen the KB level is plugged to one of the constant, C, hubs. If the value of the Element is to be negative then the N1

position must also be plugged to the Minus position which is located next to the N_1 hub.

At the top right of the plate is stage ØFD1. This stage functions whenever a Control Ring Pulse occurs and when EZ goes left. In a normal step these times would be when the following stages return left: EZ, EM, ES, ER, EPM, EPS and EPP. ØFD1 remains right for 25 us and during this interval the KB Recovery Circuit is in operation. The LP of ØFD1 goes high to ØLD1 & ØLD2. The high level from the K of ØLD1 and K-ØLD2 raises the plates of all KBR and FD diodes. These diodes, in turn, raise their cathodes and any cathode that had been low, KB call, will be returned high. Any cathode going low will be held up until ØFD1 returns left. This insures a rapid return of the KB level so that the next rising KB level will not be able to temporarily keep two KB levels high at the same time. This will reduce the possibility of wrong Decimal Registration and false Double Input Operation.

Each of the 40 Program Steps has its own associated V_1 and V_2 and R as shown on plate 38 . V_1 and V_2 can be plugged to any Element or Storage. The same Element or Storage can be used twice in one step or in any other step. The R position can only be plugged to a Storage. That storage cannot be used as a V_1 or V_2 in that same step.

The KB level is normally a low level and is raised only when that KB is called for. The call is controlled by one of the various Control Triggers.

PLUGBOARD CONTROL

Plate 38C

The Plugboard Control Plate shows the various connections required in order to perform the functions necessary in a calculating step.

The basic control is the Step Trigger, such as 2ES. This Trigger conditions an associated group of Amplifiers.

1. ESF Subvisor Control (V_2)
2. EMF Minidend Control (V_1)
3. ERF Result Control (R)
4. EPF Process Control (PROC)
5. EBP Plus Branch Control
6. EBM Minus Branch Control

The Amplifiers enable the Computer to perform any of the four mathematical processes, handling each factor, V, V_2 and R, independently.

Step Control

There are 40 calculating steps in the Computer, each step being controlled by a Step Trigger. Each Step Trigger, through its associated Amplifier controls the Process, V_1, V_2, and R and Out branch hubs of that particular step. The V_1 (Minidend), V_2 (Subvisor), and R (Result) cannot all be used simultaneously so each Amplifier controlling these hubs has a cathode control so that their values can be called upon at specific times during a calculating step. This means that only one of the three values, V_1, V_2 or R, can be read at a time. This is the source of control as to which KB is to be raised. The plugging of the plugboard hubs are on plate 37.

Branching Control

Each Step Trigger is kicked from one side of a Diode Gate. There is one side of a Diode Gate for each Step Trigger. The Diode Gate is conditioned from the In hub of the Plugboard. There is an In hub for each Diode Gate. The Diode Gates are pulsed by the ESI, Step Advance Pulse, at the beginning of each step. At the same time the ESZ, Step Zeroize Pulse, is released to return the previous Step Trigger left.

The In hub is plugged from the (+) or (-) Out hub of another step. The Out hubs are controlled by the EBP and EBM Amplifiers. The sign of the Result of a step is indicated by the position of Trigger EBS. If the Result is positive or zero, EBS is conducting on the left, and, through the Cathode Follower EBP, lowers all EBP Amplifier cathodes. The Amplifier with a high grid conducts and lowers its

respective (+) Out hub. If the Result of the step is negative the low into the LI of MC7 and high from the LP of MC7 opens LI of Gate EBG. Trigger ER going right Zeroized EBS, if EBS was right. During ER time MS goes right and the LP of MS reads Gate EBG. A Minus Result finds the Gate open so the LP of EBG releasing a negative pulse pulls EBS right. The EBP cathode is raised and the EBM cathode is lowered. This causes the (-) Out hub to be pulled low for Minus Branching.

CONTROL RING

Plate 39C

This circuit shows the various means the Control Triggers in a calculation step are operated. Only one Control Trigger can be right at any specific time. Each time a Control Trigger is returned left the KB Recovery Circuit functions as shown on plate 37 . The following is a general sequence of operation.

1. EZ 450 us delay to allow B2, B5 and Storage Zeroize. Timer is reset.

2. EM Minidend Operation

   A. M'd Decimal Complement Registration
   B. M'd Numerical Registration

3. ES Subvisor Operation

   A. S'r Decimal Registration
   B. Shifts
   C. S'r Decimal Complement Registration
   D. S'r Numerical Registration

4. ER Result Operation

   A. Result Decimal Registration
   B. Shifts
   C. Test RIG
   D. Result set in Storage

5. EDPZ 14 us delay for Storage Set Recovery

6. EPZ 450 us delay to obtain a B2 Zeroize

7. EPM Proof Minidend (Storage) Operation

   A. Storage Decimal Complement Registration
   B. Storage Numerical Registration

8. EPS Proof Subvisor (Subvisor) Operation

   A. S'r Decimal Registration
   B. Shifts
   C. S'r Decimal Complement Registration
   D. S'r Numerical Registration

9. EPP Minidend Subtraction Operation

   A. M'd Decimal Registration
   B. Shifts
   C. M'd Numerical Registration

10. CØD 100 us delay to allow Ø Check lines to normalize

Each of the above Control Triggers operations are shown on other plates in detail.

This circuit is employed by all four of the Processes, +, -, x and ÷. The circuit is only employed during ES and EPS Control Circuit Time. The circuit has two basic functions:

1. During ES time pre-condition SB and gating control for the Process plugged.

2. During EPS time pre-condition SB and gating for the reverse of the Process plugged.

Operation

Addition Process

The + Process line controlled from EPF through the Plugboard wire lowers the LI of EIA. This cuts off the LP of EIA during the entire step but the plate level cannot rise until the LP of EP1 also is cutoff. The LP of EP1 is cutoff when ES is right, plate 14 . The RP of ES goes low to the LI of EP2. The grids of EP1 and EP2 are all tied together so both stages are cutoff. All plates of EP1 and EP2, except the LP of EP1, are connected to plates of tubes which are conducting so no appreciable change can occur on their plates. The LP of EP1 can go high in conjunction with the LP of EIA to raise the plates of diode EIA2. The left cathode of EIA2 raises the LI of Gate DPG2 to hold this Gate open during all of ES time. The right cathode of EIA2 raises the LI of PSA so that when DRB goes right during ES time the Add Bias will be raised. SB is not raised when ES goes right but merely prepared for future use in ES time.

During EPS time the RP of EPS goes low to the LI of EPP2. The grids of EPP2 and EPP1 are tied together so that both stages are cutoff. Only the RP of EPP1, which is connected to the RP of EIA, is free to go high. The high from the RP of EIA and EPP1 raises the plates of diode EIS1. The left cathode of EIS1 raises the LI of Gate DPG2 to hold this Gate open during all of EPS time. The right cathode of EIS1 raises the RI of PSA so that when DRB goes right during EPS time the Subtract Bias (proof process) will be raised. SB is not raised when EPS goes right but merely prepared for future use in EPS time.

Subtraction Process

The - Process line controlled from EPF through the Plugboard wire lowers the LI of EIS. This cuts off the LP of EIS during the entire step but the plate level cannot rise until the RP of EP1 also is cutoff. The RP of EP1 is cutoff when ES is right, plate 14 . The RP of ES goes low to the LI of EP2. The grids of EP1 and EP2 are all tied together so both stages are cutoff. All plates of EP1 and EP2, except the RP of EP1, are connected to plates of tubes which are conducting so no appreciable change can occur on their plates. The RP of EP1 can go high in conjunction with the LP of EIS to raise the plates of diode EIS2. The left cathode of EIS2 raises the LI of Gate DPG2 to hold this Gate open during all of ES time. The right cathode of

EIS2 raises the RI of PSA so that when DRB goes right during ES time the Subtract Bias will be raised. SB is not raised when ES goes right but merely prepared for future use in ES time.

During EPS time the RP of EPS goes low to the LI of EPP2. The grids of EPP1 and EPP2 are tied together so that both stages are cutoff. Only the LP of EPP1, which is connected to the RP of EIS, is free to go high. The high from the RP of EIS and LP of EPP1 raises the plates of diode EIA1. The left cathode of EIA1 raises the LI of DPG2 to hold this Gate open during all of EPS time. The right cathode of EIA1 raises the LI of PSA so that when DRB goes right during EPS time the Add Bias (proof process) will be raised. SB is not raised when EPS goes right but merely prepared for future use in EPS time.

Multiplication Process

The x Process line controlled from EPF through the Plugboard wire lowers the LI of EIM. This cuts off the LP of EIM during the entire step but the plate level cannot rise until the LP of EP2 also is cutoff. The LP of EP2 is cutoff when ES is right, plate 22 . The RP of ES goes low to the LI of EP2. The grids of EP1 and EP2 are tied together so both stages are cutoff. All plates of EP1 and EP2, except the LP of EP2, are connected to plates of tubes which are conducting so no appreciable change can occur on their plates. The LP of EP2 can go high in conjunction with the LP of EIM to raise the RP of diode EIM1. The right cathode of EIM1 raises the RI of DMD and from the RD of DMD raises the LD of PMP to prepare for Multiplication Process as shown on plate 23.

During EPS time the RP of EPS goes low to the LI of EPP2. The grids of EPP2 and EPP1 are tied together so that both stages are cutoff. Only the RP of EPP2, which is connected to the RP of EIM, is free to go high. The high from the RP of EIM and EPP2 raises the RP of diode EID1. The right cathode of EID1 raises the LI of PDP to prepare for Division Process as shown on plate 25.

Division Process

The ÷ Process line controlled from EPF through the Plugboard wire lowers the LI of EID. This cuts off the LP of EID during the entire step but the plate level cannot rise until the RP of EP2 also is cutoff. The RP of EP2 is cutoff when ES is right, plate 24. The RP of ES goes low to the LI of EP2. The grids of EP1 and EP2 are tied together so both stages are cutoff. All plates of EP1 and EP2, except the RP of EP2, are connected to plates of tubes which are conducting so no appreciable change can occur on their plates. The RP of EP2 can go high in conjunction with the LP of EID to raise the RP of diode EID2. The right cathode of EID2 raises the LI of PDP to prepare for Division Process as shown on plate 25.

During EPS time the RP of EPS goes low to the LI of EPP2. The grids of EPP2 and EPP1 are tied together so that both stages are cutoff. Only the LP of EPP2, which is connected to the RP of EID, is free to go high. The high from the RP of EID and LP of EPP2 raises RP of diode EIM2. The right cathode of EIM2 raises the RI of DMD and from the RD of DMD raises the LD of PMP to prepare for Multiplication Process as shown on plate 23.

CONDITIONING CCT FOR SHIFTS

Plate 41C

The Check Counter (CCT) receives its count from Shift Pulses but only under limited conditions. The Counter is opened to count Shift Pulses under the following conditions:

1. ES time for Complementize indication.
2. EPP time in Multiplication or Division only.
3. Zero Check time to bring the CCT Count to 10.

The Counter counts shifts during ES when the M'd and S'r are being aligned, and it indicates whether or not the M'd is shifted 11 times or more.

The reason for the count of 11 can be explained by inspection of possible cases that can occur. The farthest place to the left in the Accumulator that a number may be entered is 10A. For the first 11 shifts it is impossible for any number to arrive in 11M. Therefore, carry indications would be true indications coming from 11M up till this time. However, if the M'd is shifted 11 times or more to align, then there can not possibly be a number in 11A, and there is a possibility of a number in 11M that would not give an overcarry indication should there be one due to a negative number. Therefore, the indication is taken from 11A. The most shifts that can occur to align is 22, making it impossible for the first digit of the M'd to get into 11A again. Thus the indication can be taken from 11A after 11 shifts. Actually because of the decimal input positions the count is never 11, but may be more or less than 11.

CT11 is Zeroized by B5 so that the rest of the counter may be Zeroized by B2 to be used in the Zero Check Operations and still retain the 'over 11 shifts' indication for use in the rest of the problem.

The CCT counts shifts during EPP in Multiplication or Division to record the number of shifts required to align the proof result with the M'd. During Zero Check additional shifts can be generated to bring the times the Proof Result was shifted to a total of 10. This will insure checking 10 Proof Result digits for zero.

The CCT counts shifts during Zero Check in any Process when the count in the CCT at this time is less than 10. In Addition or Subtraction the CCT count will always be zero so a total of 10 shifts are required to reach a count of 10 in the CCT. This extra 10 shifts allows a total of 20 digits to be Zero Checked. In Multiplication or Division there generally is some count, from EPP time, in the CCT. If this count is less than 10, shifts will occur to reach a count of 10.

Operation

ES Time. ES is on the right so the LP of ES is high to the LI of ESA. The LD of ESA taps off high to the RD of EMZ. The RP of EMZ goes low to the LI of CGA. The LP of CGA is tied to the RP of CCM and the RP of CCM is also cutoff. (CT11 is left so its RP is high to the RD of DCK2. The RP of DCK2 is low to the RI of CCM holding CCM cutoff).

The high from the RP of CCM and LP of CGA raises the LI of CTSG to open this Gate to shifts during ES. The Count Triggers in the CCT indicate count as their stage names state. At a count of 10, CT10, CT8 and CT2 are right. At a count of 11, CT11, CT10, CT8, CT2 and CT1 are right. If the number of shifts exceeds 16 the CCT is closed to any shifts after 16. At a count of 16 only CT11 is right. The RP of CT11 is low to the RD of DCK2. DCK2 is cutoff so its plates are high to the RI of CCM causing the RP of CCM to go low and close CTSG to any further shifts. The purpose of counting shifts during ES is strictly to see if the shifts required are more or less than 11.

EPP Time in Multiplication or Division Process. EPP is on the right so the RP of EPP is low to the RI of ECB1. The RD of ECB1 taps off low to the LD of EMZ', cutting off the LP of EMZ'. The LP of EMZ' is tied to the RP of CPMD which is also cutoff. (The Process of Multiplication or Division lowers the plates of the diode PIMD). The low from PIMD lowers the LI of PPI and taps off the LD of PPI to the RD of CPMD. The RP of CPMD is cutoff. The high from the RP of CPMD and LP of EMZ' raises the LI of CPMD. The LP of CPMD goes low to the LI of CGA, cutting off the LP of CGA. At this time, CT10 and CT11 are both left so DCK2 has a low plate to the RI of CCM, cutting off the RP of CCM. The RP of CCM and LP of CGA go high to the LI of CTSG opening this Gate to shifts during EPP.

Zero Check. If the count in the CCT is less than 10, CT10 left, Trigger CØCS (Plate 19) will go right and lower the RI of CØDD. The RP of CØDD goes high to the RI of CTSG to open the CCT to count shifts. When CT10 goes right, Trigger CØCS will be returned left to again close the CCT to shifts.

SIGN BIAS

Plate 42C

This plate is a schematic representation of the circuit shown on plate 43. The explanation of this circuit is written up under Sign Bias - Addition and Subtraction.

SIGN BIAS - ADDITION AND SUBTRACTION

Plate 43C

This plate illustrates the method employed in controlling the Accumulator Amplifier Biases. These Biases are shown on plate 1 and referred to as Add and Subtract Bias.

The raising of Sign Bias requires two steps. The control circuit first prepares which Sign Bias, Add or Subtract, is to be raised. At the proper time the clamp is released and Sign Bias rises. One control tells which Bias and the second control tells the proper time.

Raising SB automatically starts a cycle of RIG.

Operation

This circuit shows the controls required to raise either the Add or Subtract Bias. Each control will be explained separately.

Add Bias

The control circuits will condition the LI of PSA high from either EIA1, EIA2, or EIA3. At this time DRB is left so the RP of DRB is high to the RI of PSAC. The plates of PSAC are conducting and therefore take precedence to maintain the left grid of PSA low. This condition will remain until DRB is triggered right. DRB going right cuts off PSAC, removing the clamp on PSA. The left grid of PSA is raised and the LP of PSA conducts. The low from the LP of PSA lowers the LI of PABA. The RD of PABA is low since Trigger PAM is on the left (no negative number). Both sides of PABA are cutoff so the plates are free to go high. The high from the plates of PABA go to BA+1, BM+1 and B11+1. In the three latter stages two neons in series, as shown on plate are fired which raises the grids of BA+ and BA+1, BM+ and BM+1 and B11+ and B11+1. These stages are Cathode Followers and control the Amplifier Add Biases of Accumulators 1A-11A, 1M-10M and 11M respectively.

The grid of BA+ is connected, through a resistor, to the LC of RB. The high from BA+ causes RB to conduct, releasing a negative pulse from the LP of RB. This negative pulse from RB starts a cycle of RIG as shown on plate 5.

SB will remain high until the cycle of RIG is completed (CX Pulse). DRB returns left and reclamps PSA resulting in lowering SB.

The Test RIG, during ER Control Circuit Time, does not require any SB preparation. When the LP of MZR goes low the Add Bias is raised.

Subtract Bias

The control circuits will condition the RI of PSA high from either EIS1, EIS2 or EPPM. At this time DRB is left so the RP of DRB is high to the RI of PSAC. The plates of PSAC are conducting therefore they take precedence to maintain the right grid of PSA low. This condition will remain until DRB is triggered right. DRB, going right, cuts off PSAC removing the clamp on PSA. The right grid of PSA is raised and the RP of PSA conducts. The low from the RP of PSA lowers the LI of PABA1. The LD of PABA1 taps off low to the RD of PABS1. The LI of PABS1 is low since Trigger PAM is on the left (no negative number). Both sides of PABS1 are cutoff so the plates are free to go high. The high from the plates of PABS1 go to BA-1, BM-1 and B11-1. In the three latter stages two neons in series, as shown on plate 42 , are fired which raises the grids of BA- and BA-1, BM- and BM-1, and B11- and B11-1. These stages are Cathode Followers and control the Amplifier Subtract Biases of Accumulators 1A-11A, 1M-10M and 11M respectively.

The grid of BA- is connected, through a resistor, to the RC of RB. The high from BA- causes RB to conduct, releasing a negative pulse from the RP of RB. This negative pulse from RB starts a cycle of RIG as shown on plate 5.

SB will remain high until the cycle of RIG is completed (CX Pulse). DRB returns left and reclamps PSA resulting in lowering SB.

MINUS FACTOR - ADDITION AND SUBTRACTION

Plate 44C

This plate shows the method employed for controlling the Accumulator Amplifier Biases. These Biases are shown on plate 1 and are referred to as Add and Subtract Bias. This circuit is employed in the event the number has a negative value.

The raising of Sign Bias in dealing with Minus Factor requires 3 steps. The control circuit first prepares which Sign Bias, Add or Subtract, is to be raised. Secondly, the control circuit, by means of Keyboard Bias, reads to check for Minus Factor. This operation is shown on plate 20 . If a number proves to be negative Trigger PAM is kicked right.

NOTE: An exception to this occurs in Complementize where the reverse is true. A positive number kicks PAM.

Last, the Trigger DRB goes right to release the clamp and raise Sign Bias. In this case, because PAM is right, the opposite Sign Bias to the one originally prepared will be raised.

Raising SB automatically starts a cycle of RIG.

Operation

Add Bias - Subtraction with Minus Factor

This operation would occur during ES, EPS or EPP Control Circuit Time. The control circuits will condition the RI of PSA high from either EIS1, EIS2 or EPPM. At this

time DRB is left so the RP of DRB is high to the RI of PSAC. The plates of PSAC are conducting so therefore take precedence to maintain the right grid of PSA low. This condition will remain until DRB is triggered right. DRB, going right, cuts off PSAC, removing the clamp on PSA. The right grid of PSA is raised and the RP of PSA conducts. The low from the RP of PSA lowers the LI of PABA1. The RD of PABA1 is low since Trigger PAM is on the right (negative number). Both sides of PABA1 are cutoff so the plates are free to go high. The high from the plates of PABA1 go to BA+1, BM+1, and B11+1. In the three latter stages two neons in series, as shown on plate 42 , are fired which raises the grids of BA+ and BA+1, BM+ and BM+1 and B11+ and B11+1. These stages are Cathode Followers and control the Amplifier Add Biases of Accumulators, 1A-11A, 1M-10M and 11M respectively.

The grid of BA+ is connected, through a resistor, to the LC of RB. The high from BA+ causes RB to conduct, releasing a negative pulse from the LP of RB. This negative pulse from RB starts a cycle of RIG as shown on plate 5.

SB will remain high until the cycle of RIG is completed (CX Pulse). DRB returns left and reclamps PSA resulting in lowering SB.

Subtract Bias - Addition with Minus Factor

This operation could occur during any control circuit time except ER or EPM. The control circuits will condition the LI of PSA high from either EIA1, EIA2 or EIA3. At this time DRB is left so the RP of DRB is high to the RI of PSAC. The plates of PSAC are conducting, therefore they take precedence in maintaining the left grid of PSA low. This condition will remain until DRB is triggered right. DRB, going right, cuts off PSAC, removing the clamp on PSA. The left grid of PSA is raised and the LP of PSA conducts. The low from the LP of PSA lowers the LI of PABA and taps off the LD of PABA low to lower the RD of PABS. The LI of PABS is low since PAM is right (negative number). Both sides of PABS are cutoff so the plates are free to go high. The high from the plates of PABS go to BA-1, BM-1 and B11-1. In the three latter stages, two neons in series, as shown on plate 42 are fired which raises the grids of BA- and BA-1, BM- and BM-1 and B11- and B11-1. These stages are Cathode Followers and control the Amplifier Subtract Biases of Accumulators 1A-11A, 1M-10M and 11M respectively.

The grid of BA- is connected, through a resistor to the RC of RB. The high from BA- causes RB to conduct, releasing a negative pulse from the RP of RB. This negative pulse from RB starts a cycle of RIG as shown on plate 5.

SB will remain high until the cycle of RIG is completed (CX Pulse). DRB returns left and reclamps PSA resulting in lowering SB.

SIGN BIAS - DIVISION AND MULTIPLICATION

Plate 45C

This plate shows the method employed for controlling the Accumulator Amplifier Biases in Multiplication or Division. These Biases are shown on plate 1 and referred to as Add and Subtract Bias.

This circuit is employed only during ES or EPS Control Circuit Time. No preparation is necessary, as in Addition or Subtraction, since negative numbers do not affect this circuit.

Raising SB automatically starts a cycle of RIG.

Operation

This circuit is composed of three parts, Multiplication, Trial Subtraction, and Add Back. Each operation is covered separately.

Multiplication

Trigger PM2 goes right in Multiplication whenever a number is to be registered (cycle of RIG). The RP of PM2 going low cuts off the LP of PM23. The LP of PM23 goes high to BA+1, BM+1 and B11-1. In the three latter stages two neons in series, as shown on plate 42 , are fired which raises the grids of BA+ and BA+1, BM+ and BM+1 and B11- and B11-1. These stages are Cathode Followers and control the Amplifier Add or Subtract Biases of Accumulators 1A-11A, 1M-10M and 11M respectively.

The grid of BA+ is connected, through a resistor, to the LC of RB. The high from BA+ causes RB to conduct, releasing a negative pulse from the LP of RB. This negative pulse from RB starts a cycle of RIG as shown on plate 5.

This combination of Sign Biases allows a number to be added in Accumulators 1A-11A and 1M-10M. Accumulator 11M has the Subtract Bias raised so any pulses in this Accumulator will cause subtraction.

This SB is not necessarily lowered at the completion of one cycle of RIG (CX Pulse). The length of time this SB combination is raised is controlled by PM2 which is in turn controlled by the presence of a digit in 11M. This operation is shown on plate 23.

Division - Trial Subtraction

Trigger PD1 goes right in Division whenever a Trial Subtraction is required (cycle of RIG). The RP of PD1 going low cuts off the RP of PDA. The RP of PDA goes high to BA-1, BM+1 and B11+1. In the latter three stages, two neons in series, as shown on plate 42 are fired which raises the grids of BA- and BA-1, BM+ and BM+1, and B11+ and B11+1. These stages are Cathode Followers and control the Amplifier Add or Subtract Bias of Accumulators 1A-11A, 1M-10M and 11M respectively.

The grid of BA- is connected, through a resistor, to the RC of RB. The high from BA- causes RB to conduct, releasing a negative pulse from the RP of RB. This negative pulse from RB starts a cycle of RIG as shown on plate 5.

This combination of Sign Biases permits a number to be subtracted in 1A-11A and added in 1M-10M and 11M.

This SB is not necessarily lowered at the completion of one cycle of RIG (CX Pulse). The length of time this SB combination is raised is controlled by PD1 which in turn is controlled by the 11A to 1M overcarry. This operation is shown on plate 25.

Division - Add Back

Trigger PD2 goes right in Division whenever an Add Back is required (cycle of RIG). The RP of PD2 going low cuts off the LP of PDA. The LP of PDA goes high to BA+1, BM-1 and B11-1. In the latter three stages two neons in series, as shown on plate 42 , are fired which raises the grids of BA+1 and BA+, BM-1 and BM- and B11-1 and B11-. These stages are Cathode Followers and control the Amplifier Add or Subtract Bias of Accumulators 1A-11A, 1M-10M and 11M respectively.

The grid of BA+ is connected, through a resistor, to the LC of RB. The high from BA+ causes RB to conduct, releasing a negative pulse from the LP of RB. This negative pulse from RB starts a cycle of RIG as shown on plate 5.

This combination of Sign Biases allows a number to be added in Accumulators 1A-11A and subtracted in 1M-10M and 11M.

This SB is lowered after one cycle of RIG is completed (CX Pulse). Trigger PD3 controls this SB and is in turn controlled by the 11A to 1M overcarry which occurs on every Add Back Operation. This operation is shown on plate 25.

(-) STORAGE BIT OPERATION

Plate 46C

Any minus Result in x or ÷ and a numerical minus Result in + or - will result in lowering the plates of MC8. This, in turn, raises the LP-MC7 to condition Gate EBG for Minus Branching. The same low from MC8 cuts off the LP-SSRO to raise the cathodes of SSK conditioning the starter electrode of the Minus Bits so that the Storage Set Pulse can fire the proper tube. When the Minus Bit is fired its indication is read, by the Read Out Driver, thru the right side of SSRO resulting in raising the RP-SSRO and firing the minus neon for Storages. Whenever the A Section is zero during MS time and MC2 is right, Minus Branching & Minus Result to Storage are defeated. Stage Ø9C would be cut off and the high from its LP keeps the LI-MC8 low preventing conduction in this tube as shown on plate 20.

-40V REGULATED SUPPLY

Plate 47C

The -40V supply is employed in the Storage Circuit. It is used as a high voltage limit on the cathode of the FK stages. The tubes and circuit components used to make up this supply are located in the Power Control Section behind the Meter Panel. The supply is self regulating.

Operation

Tube OB2, a Voltage Regulator, is placed in parallel with three resistors. This means that the voltage drop across these three resistors is constant and regulated. One of these resistors is a potentiometer, R212. R212 adjusts the control grid of the pentode 6AU6. It is this potentiometer which is adjusted to obtain a -40 reading. The amount of conduction thru the 6AU6 and therefore the plate voltage of the 6AU6 will control the grid level of the 6AS7 tube. The plate of the 6AU6 uses a 120K resistor to +150 as a load resistor. The voltage drop across this resistor, through the 114V neon, controls the grid voltage of the 6AS7. The plate of the 6AS7 controls the output voltage level which is adjusted at R212 to be -40 volts.

The regulation of this -40 volt supply is obtained by the 6AU6 tube. Any variation of the -40 volt level will affect conduction in the 6AU6 since the cathode of the 6AU6 is connected to this -40 volt line. Suppose the -40 volt supply attempts to go to -38 volts. This rise in voltage raises the cathode of the 6AU6 lessening conduction in this tube. The plate of the 6AU6 will rise and because of amplification some of the change on the plate is fed back to the control grid through the 47 uuf. capacitor. The amount of plate rise is then fed to the grid of the 6AS7 which causes this tube to conduct more and bring the -40 volt line back to normal. The inverse would be true if the -40 volt supply was momentarily lowered.

CATHODE CONTROLS ON CX

Plate 48C

The CX Gate cathode control is used to stop the Computer operation under the following conditions:

1. The Test Counter reaching 400 when used on Post RIG. This enables the Service Technician to read the Accumulator values at various times.

2. Alpha or Double Input Check in the Input Decoder. The decoding system combined with a cycle of RIG would enable the Computer to register a number value when a Double Input is present. This cathode control prevents the Computer from continuing calculation whenever this occurs.

3. PTP when Read switch is operative. The Read switch is used whenever the V_1, V_2, or R values are to be read. This prevents the Computer from calculating beyond EM time.

4. KB Detector Circuit. Whenever a KB is raised some detection is necessary since a zero numerical value is permissible. Every value, zero included, must have a decimal. The lack of any Decimal Input Line being raised will block CX to indicate that KB is missing.

5. C9T time must nullify the KB Detector Circuit since C9T has no decimal but does register a 1 in Accumulator 1A.

STEP TRIGGER AND GATE

Plate 49C

This circuit is a schematic representation of the method used to bring a Step Trigger right.

Branching into a new step is controlled from stage EBP for a Positive Result or from stage EBM for a Minus Result. The plate of one stage will conduct sending its plate low, through the Plugboard, to the resistive input of a Diode Gate, opening the Gate. When the previous step is completed an ESI Pulse is released. This ESI Pulse pulses the open Diode Gate. The plate of the Diode Gate releases a negative pulse to the RD of a Step Trigger, triggering this stage right.

This method is employed in branching into Function Steps as well as Calculating Steps.

FLIP - FLOP DELAYS

NAME	TYPE	TIME	DELAY
RS	F-1	25 us	T.D. between RIG1' & RIG8
ØFD1	F-1	25 us	T.D. for return of ØF1. KB Recovery
ØFS	F-1	25 us	T.D. between Ctl. Ring Pulses
PMD2	F-1	25 us	T.D. lower SB before shifts (M-D)
PM3	F-1	25 us	T.D. to condition circuit for a Ø or digit in 11M
PDND	F-1	25 us	T.D. to stop shifts before 1st Trial Subtraction
PD2D	F-1	25 us	T.D. to lower SB before Shifts
PMØD	F-1	25 us	T.D. for M-D CTR. to be conditioned
PDAM	F-1	25 us	T.D. to return PAM
DCCD	F-1	25 us	Delays the (-2) Corr. Pulse in DCR
DP1-DP16	F-1	25 us	Decimal Registration delay
PT3	F-1	25 us	Allow ARG to open before pulsing EGD
RD	F-2	100 us	T.D. for SB to rise
CØD	F-2	100 us	T.D. for Ø Check Lines to normalize
CØDA	F-2	100 us	" " " " " " "
C9D	F-2	100 us	" " " " " " "
ICL	F-2	100 us	Operates Input Recovery
EZB5	F-2	300 us	B5 Zeroize
EZB2	F-2	300 us	B2 Zeroize
EPZ	F-3	450 us	T.D. for B2 Zeroize
EMDZ	F-3	450 us	" " " "
ØFZD	F-3	5 ms	T.D. for Storage Zeroize
EMZ	F-3	5 ms	" " " "
AGF1	F-3	10 ms	Function Step delay
AGF2	F-3	10 ms	" " "
AAF1	F-3	10 ms	Set I Pulse
AAF2	F-3	10 ms	Set II Pulse
EP4	F-3	1200 us	Timer recharge time
EP	F-3	5 ms	Absorb Cam A contact bounce
ESD	F-3	150 us	Delay between ESZ & ESI
MS	F-3	150 us	T.D. to Set Storage
DEA	F-3	150 us	T.D. for KB to rise or fall
MZ (1)-MZ(12)	F-3	2 ms	Generate Stor. Clear Pulse
EGD	F-4	14 us	Calls for ESI, ESZ & EZ
PMD1	F-4	14 us	T.D. to condition a Gate (M-D)
EDPZ	F-4	14 us	T.D. to allow Stor. Set Lines to normalize
CD	F-5	50 us	T.D. to allow RIG1 to be registered
PAMD	F-6	250 us	T.D. to allow KB to rise
EZ	F-6	450 us	T.D. for Zeroize

CALCULATOR CRANK UP

Plate 50C

This circuit is located in the Power Control end of the Computer. The term crank up refers to the sequence of operation necessary to turn on the fans, bring up the tube filaments and supply the D C voltages once the On button is depressed. The A_1, B_1, C_1, A_2, B_2 and C_2 lines represent the AC supply required to operate the Computer. In a single phase system the A_1, B_1 and C_1 lines are all connected. In a three phase system the A_1, B_1 and C_1 lines are separate.

K201

Line C_2 through fuse F209 is connected to the On button. Depression of the On button supplies this AC voltage through the Off button to the coil of K201. K201 is energized and the AC line returns through F210 to line B_1. Contacts 4 and 5 and 7 and 8 make on K201. Contacts 4 and 5 on K201 become a holding circuit through the Off button for K201.

Fans

Line A_2 through F203, F201 and contacts 7 and 8 of K201 energizes K204. K204 AC supply returns on line A_1. The contacts on K204 transfer so the AC from line A_2 through F203 will pass through the closed contacts on K204 to operate the Fan Motors.

K202

Line A_2 through F203, F201 contacts 7 and 8 on K201, and 1 and 3 contacts on the Thermostat energizes K202. K202 AC supply returns on line A_1. The contacts on K202 are used as the return for all transformer primaries used in the filament supply and DC voltage supply. Line C_2 through F208 passes through a 17 ohm 300 watt resistor to supply the primaries of the filament transformers T26 and T27. Lines B_2 and A_2 in a like manner supply filament transformers T26C, T28, T21, T26A and T26B. The supply to these transformer primaries is reduced through the 17 ohm resistors so that the filament voltage is only partial. Transformer T29 on line B_2 is used to supply 115 volt AC to the outlet, Lumilines and Selector Relays.

TD201

Line A_2 through F203, F201, contacts 7 and 8 on K201 and 1 and 3 contacts on the Thermostat energizes the Hold Coil for TD 201 and through the 120 second contact energizes TD201. TD201 is a time delay unit which completes a series of 3 circuits over a preset time interval. The Hold Coil is a mechanical hold to prevent the contacts closed by TD201 from reopening when TD201 is de-energized by the 120 second contact.

1. Circuit #1 - 10 seconds

   10 seconds after TD201 is energized these contacts transfer.

The same AC supply as that to TD201 passes through these contacts to energize K203. The contacts on K203 will shunt out the 17 ohm resistors which allows the filament voltages to rise to their proper value.

2. Circuit #3 - 60 seconds

60 seconds after TD201 energizes these contacts are transferred. Line A_2 through F202 contacts 3 and 4 of K203 and circuit #3 contacts on TD201 energizes K205. The contacts of K205 transfer preparing for the circuit #2 operation.

3. Circuit #2 - 90 seconds

90 seconds after TD201 energizes these contacts are transferred. Line B_2 through F204 contacts 5 and 6 of K203, F206, circuit #2 contacts on TD201, K205 contacts, Plugboard and Service Interlocks energizes TD202. This same AC supply passes through the closed 5 second contact on TD202 to energize K206. The contacts on K206 transfer so that line C_2, through F207, will energize the primaries of the transformers T22, T24, and T25. These transformers supply the minus DC voltage circuits. Each DC voltage, upon reaching its proper value, pulls in a relay. These relays, K115, K114, K113, K112, K118, K111 and K210, have an AC supply, from the 5 second TD202 contact, pass through their contacts to energize K207. All minus voltages must be up to their proper level in order for K207 to be energized. K207 has its contacts transfer so that line B_2 through F205 can energize the primaries of the transformers T23 and T30. These transformers supply the plus DC voltage circuits. The two plus DC voltages, upon reaching their proper value, energize K116 and K117. The AC supply to TD202 now bypasses the 5 second contact on TD202 to the Plus Voltage Check. The AC supply passes through the Plus Voltage Check to the Common Voltage Check. The AC supply at the Common Voltage Check holds in K206 and also goes through the minus voltage contacts to the Minus Voltage Check to hold in K207. The 5 second contact on TD202 now opens but the DC voltages are now kept available through their own interlock. Any of the DC voltages dropping out will automatically drop out all the other DC voltages. In case of a blown fuse in any one of the DC voltage circuits the fuse neon will only be lit for approximately 5 seconds due to the supply to K206 and K207 being removed by the 5 second contact TD202. TD202 remains energized. In order for the fuse neon to refire either the Service or Plugboard Interlock must be broken and remade so TD202 can drop out and then pull in again to resupply the DC voltage circuits.

4. 120 seconds

120 seconds after TD201 is energized this contact opens. TD201 is de-energized but circuits 1, 2 and 3 remain closed by the mechanical action of the Hold Coil.

The crank up is completed, the Ready light is lit on the Punch Operators Panel and the Computer is ready to calculate.

POWER SUPPLY VOLTAGES

Plates 51C and 52C

These plates show the connections and components required to rectify the positive and negative DC voltages. All DC voltages are full wave rectified. The voltage check system as explained on plate 50 is shown so the relay operation can be seen.

The -165, -90, -15, -375, +75 and +150 volt supplies have their filter capacitors partially charged through resistors. Each voltage supply when at their proper level pulls in a relay whose contacts shunt out the charging resistor.

The control circuit mounted at the top of the -165V Capacitor assembly is for the purpose of eliminating overloads on the EL3C Rectifier tube, which would otherwise be present when the filter capacitor bank charges.

At the instant T-22 becomes energized, charging current flows to capacitor C203, through resistors R201, R202 and R203. These resistors limit the current flow to a safe value for the tube.

As the -165V line on the output of F219 increases its voltage in a negative direction, R207 passes current to C201, charging same. As the charge reaches the voltage required to operate K209, the relay closes, and shorts out R203. At this time, an increased current flows through R201 and R202, charging the capacitor C203 further.

The closing of K209 also starts a new charging time interval when contacts 7 and 8 close. This permits C202 to be charged through R208 and K210 then operates. Contacts 3 and 5 (paralleled) and 4 and 6 (paralleled) then short out R201 and R202, allowing full current charge of capacitor bank C203.

K208 contacts are used to discharge C201 and C202 through R204 and R205 so that full charging time is available in the following charging cycle, should it follow immediately.

These circuits are checked as follows:

1. All relay contacts should be clean and have proper wiping action. They must make very good contact.

2. Resistors R201, R202, R203, R207 and R208 should be checked.

3. Timing of K209 and K210 should be checked, and if found to be short, C201 and C202 should be changed. K209 should pull in approximately .2 seconds after T-22 is energized. K210 should pull in .9 seconds after K209 closes.

Relay K119 contacts 4 and 5 and K112 contacts 5 and 6 are used to break the 115 volt AC supply to the Selector Power Chassis whenever the Service or Plugboard Interlocks are broken.

The transformer primary windings for both filament and D.C. supplies have an auxiliary winding which permits closer adjustment of the output voltage on the

secondary side. All transformer primaries are numbered similarly; therefore, any transformer adjustment, filament or D.C. can be made according to plate 51 or 52.

The Line voltage should first be measured and then the transformer primaries may be connected using plate 51 or 52 as a guide. Some corrections may be necessary to offset transformer variations.

Line Voltage	5 - 6 Coil	Primary Connections
230	Do not use	Line to 4
226	use	Line to 5, 6 to 4
224	use	Line to 6, 5 to 3
220	Do not use	Line to 3
216	use	Line to 5, 6 to 3
212	use	Line to 6, 5 to 2
208	Do not use	Line to 2

When it is not necessary to use Terminals #5 or #6, leave one end of the jumper wire connected to Tap #5 or #6 and the other to a tap not being used for the line.

CAUTION: Never connect the jumper wire from Terminal #5 to #6.

The filament voltages should be at 6.3 Volts ± .2 Volts at the chassis male contacts or at the socket of the Rectifier or Thyratron Tube requiring a 6.3 Volt filament supply. The Rectifier Tubes requiring a 2.5 Volt filament supply should have 2.5 Volts ± .01 Volts at their socket.

No adjustment should be attempted without the use of a low scale A.C. meter of 2% accuracy or better since the usual accuracy of the field service meters is not better than 5%.

The D. C. voltages should be adjusted within 2% except -60 which is allowed 10%.

The current available to the Punch Actuators can be increased from 2 to 3 ma. by adjustment of the -165 Volt Supply so that with a maximum value in Storage the -165 Volt value will still be very near -165 Volts.

The following procedure should be observed when adjusting the -165 Volt Supply:

1. The line voltage should be at its nominal value, all Storages cleared, and the Field Board removed.

2. Univac - 120

   Set the -165 Volt Supply to -169 plus (+) or minus (-) 2 Volts.

   Univac - 60

   Set the -165 Volt Supply to -167 plus (+) or minus (-) 2 Volts.

3. When all Storages in all columns have an even value, the -165 Volt supply should read very close to -165 Volts.

4. If the line voltage is above or below the nominal value, then the plus (+) or minus (-) 150 Volt line can be used as a guide. If, for example, both read very nearly the same and are 2 Volts low, then the -165 Volt Supply reading will also be 2 Volts low. Therefore, if adjustment is being made on a Univac 120 the -165 line would be set at -167 Volts (plus (+) or minus (-) 2 Volts) and when all Storages are set it would then drop to -163 Volts.

PUNCH POWER SUPPLY

Plate 53C

The Punch has two transformers and two selenium rectifier bridges to give a 70 volt full wave rectified DC supply. These supplies are 70 R for Punch Relays and 70 C for Punch Clutch and Brake circuits. The motor is driven by a 230 volt supply. Line 1 and line 2 are used to operate the AC solenoids in the Punch.

The motor and 70 volt supplies are operative only when the On switch is effective on the Operators Panel.

Plate 14B shows the physical location of the Power Supply and Punch Relays. This section is located on a hinged door on the left hand side of the Punch.

PUNCH CLUTCH AND BRAKE OPERATION

Plate 54C

Clutch

The Clutch used in the Punch is electro-mechanical. There must be a voltage supply to the Clutch in order to function. The Clutch can be energized by three methods.

1. Card Feed Start Switch when the Computer is not calculating.
2. Trip Pulse at the completion of a calculation.
3. Card Release and Unit Switch joint operation at all times.

Each of the three methods will be explained individually. The Brake Release Relay K11 is energized in parallel to the Clutch, excluding resistor R50.

Card Feed Start Switch

The operation of the Start Switch applies ground through the switch to contacts 10 and 11 on K4 to charge C31 and energize the Single Cycle Relay, K3, while C31 is charging. The 70C volt supply goes through R6 to L1 to contacts 5 and 6 of K1 (K1 is energized whenever the Punch Motor is running and no card jam is present) to contacts 3 and 4 of K3 to contacts 5 and 6 of K18 (K18 is de-energized when no calculation is occuring) to contacts 4 and 5 of K10 to ground. Clutch, L1, is now energized and the Punch will cycle. K3, being capacitively energized, will not remain energized so an alternate method must be provided to keep the Clutch, L1, energized when K3 de-energizes.

The Clutch is retained energized by the 70C supply through R6 to L1 to contacts 5 and 6 of K1 to Cam M (290-116) then Cam N (28-214) to ground. Cams M and N are both needed so that the stopping time of the Punch can be altered without affecting the pickup time of Cam M. The Punch does not stop as soon as Cam N breaks since the Brake must be applied. The Brake operation is explained under a later heading.

The operation of the Start Switch can also energize the Shut Off Relay, K5. There is an On-Off switch on the Operators Panel called Auto Start. This switch is generally in the On position. The On position assures the Punch of automatic cycling by a Trip Pulse. In the event only one card at a time is to be fed, the Auto Start switch is placed in the Off position. When the Auto Start switch is in the On position and the Start Switch is operated, ground is supplied to the Shut Off Relay, K5, causing K5 to energize. K5 sets up its own holding circuit. A 70R volt supply through K5 to contacts 3 and 4 on K5 to contacts 7 and 8 on K3 to Full Receiver contacts, to Full Chip Basket contacts, to No Card Sensing contacts, to Stop Switch contacts, to ground enables K5 to remain energized. Any condition which breaks this hold circuit de-energizes K5 and prevents a Trip Pulse from energizing the Clutch. Releasing the Start Switch discharges C31 through R12.

Trip Pulse

A Trip Pulse is released from the Computer whenever the calculation of a card is

completed. The Trip Thyratron Pulse passes through contact 3 and 4 of K1 to contacts 6 and 5 of K2 (K2 is energized by Cam K when the Punch cycles and the DC voltages are present in the Computer with the VAD Relay reset and held through the Unit-Clear Switches) to K16 to +150 volts to energize the Trip Pulse Relay, K16. K16 sets up a holding circuit from +150 volts through K16 to contacts 9 and 10 on K16 through Cam L (114-75) through Unit-Clear switches to ground.

The Clutch can now be energized by a 70C volt supply through R6 to L1 to contacts 5 and 6 on K1 (Cams M and N usually are broken at this time) to contacts 6 and 7 on K5 (energized by Start Switch operation) to contacts 12 and 13 on K16 to ground. This enables the Punch to again cycle and at 290° of Punch Time Cams M and N continue to hold the Clutch energized.

Card Release and Unit Switch

The Card Release and Unit Switches must be operated jointly to be effective in energizing the Card Release Relay, K4. The contacts on K4 not only enable the Clutch to energize but also energizes the Skip Solenoid and prevents a Sort Solenoid and Non-Reset Solenoid operation.

The Card Release Relay, K4 is energized by ground through operated Unit and Card Release Switches through K4 to 70R volt supply. Contacts 9 and 10 on K4 charge C31 to energize K3 while C31 is charging. The Clutch can now be energized. The 70C supply through R6 to L1 to contacts 5 and 6 on K1 (Cams M and N are open) to contacts 3 and 4 on K3 to contacts 12 and 13 on K4 to contact 6 on K18 to contacts 4 and 5 on K10 to ground allow the Clutch to energize. Once the Punch has started to cycle, Cams M and N keep the Clutch energized.

Brake

The Brake Magnet is energized automatically whenever the Clutch is de-energized. The Brake Magnet does not remain energized once the Punch is stopped. The Brake Release Relay is energized in parallel with the Clutch and it is the Brake Release Relay, K11, de-energizing that signals the Brake is to be applied.

The Brake Release Relay, K11, is energized together with the Clutch and contacts 3 and 4 on K11 enable whatever charge may be present on C3 to discharge through R16. The Clutch and K11 will de-energize when Cam N opens and no Trip Pulse has occurred. C3 will charge through contacts 4 and 5 of K11 at a Time Constant determined by R5. K10 is in parallel with R5 and will be energized while C3 is charging. The 70C volt supply through R6 to L2 to contacts 14 and 15 of K16 to contacts 3 and 4 of K10 to ground will enable the Brake Magnet to energize. As soon as C3 is charged K10 de-energizes and the circuit for the Brake Magnet is broken causing the Brake Magnet to de-energize. The Punch is now stopped. Any incoming Trip Pulse will again energize the Clutch and Brake Release Relay. The Brake Release Relay being energized will discharge C3.

In the event the Stop Switch was operated to prevent any further Punch cycling a Trip Pulse would still energize the Trip Pulse Relay, K16, so another path is required to operate the Brake Magnet, L2. The Stop Switch operation will de-energize K5 so the 70C supply through R6 to L2 to contacts 14 and 15 on K5, instead of 14 and 15 on K16, to contacts 3 and 4 on K10 to ground will energize the Brake Magnet.

Unit and Clear Switches to Punch Position

The operation of these two switches jointly will break the hold circuit for the Trip Pulse Relay, K16, and the B+ Failure Relay, K2, as well as reset the Hi-Lo Relay in the VAD Chassis. In the event a problem is to be repeated after a Trip Pulse was received at K16, all Selector Relays, except any on Selector Hold, will not remain energized since the Control Common is broken. Operation of the Unit and Clear Switches de-energizing the Trip Pulse Relay, K16, causes the Control Common to again become effective.

Unit and Clear Switches to Calc. Position

The operation of these two switches jointly causes the Manual Clear Relay to de-energize as long as these switches are held operative. The Manual Clear Relay, being de-energized, will clear all Storages as well as de-energize all Selector Relays and Select Thyratrons and cutoff the Timer.

Start Pulse

This pulse is used to signal the Computer that a card has been sensed and, therefore, calculation can begin.

Ground through Cam A (334-30) to the no card sensing switch to the RC of EP in the Computer, kicking EP right.

When no card is sensed the No Card Sensing Switch opens from 310° - 60° which nullifies any attempt from Cam A to start a calculation.

Non-Calculate Pulse

Two cycles of the Punch are required before a card is sensed after being fed from the Feed Magazine. The first cycle of the Punch comes from operation of the Start Switch. The second cycle comes from the Non-Calculate Pulse. This is the only time the Non-Calculate Pulse can occur.

On the first cycle of the Punch, when Cam A closes, the No Card Sensing Switch is transferred because no card is in the Sensing Section.

The transferred contacts of the No Card Sensing Switch are connected to the Empty Magazine Switch. Cards are in the Feed Magazine so the Empty Magazine Switch is closed. The ground from Cam A will now go to the RC of ATT, triggering ATT right as shown on plate 30 . ATT, going right creates a Trip Pulse to automatically trip the Punch into its second cycle at which time this first card will be sensed. In the event a misfeed occurs at the throat the Non-Calculate Pulse will not be effective because the Shut Off Relay, K5, would de-energize preventing the Clutch, L1, from being energized even though the Trip Pulse Relay, K16, may energize.

SORT, SKIP AND SET HOLD

Plate 55C

Sort

The Sort operation is begun in the Computer when either the Sort I (ASA1), Sort II (ASA2) or ØF Sort (ARA1) Thyratrons are fired. A Sort Operation is controlled by branching in the Program. The plates of all three Sort Thyratrons are connected to the Sort Pulse Relay, K7.

The final result is to energize the Sort Solenoid which opens the Front Receiving Magazine.

A Sort Pulse will energize the Sort Pulse Relay, K7, transferring its contacts. Contacts 5 and 6 of K7 are used as a holding circuit for K7 through contacts 9 and 10 of K13.

The card whose calculation created the Sort Pulse is released by a Trip Pulse between 268° - 275°. At 334° of the next card cycle Cam E closing supplies ground through contacts 3 and 4 of K7 to K13, energizing the Sort Relay, K13. The contacts of K13 transfer. Contacts 9 and 10 of K13 open to break the hold circuit for the Sort Pulse Relay, K7, causing K7 to de-energize. The Sort Relay, K13, is held energized by contacts 5 and 6 of K13, contacts 4 and 5 of K4 and the contacts controlled by L7 to ground.

At 139° Cam F closes. The Sort Solenoid, L7, is energized from Line 1 to contacts 7 and 8 of K4 to contacts 3 and 4 of K13, to L7, to Cam F, to Line 2. L7 energizing mechanically transfers two sets of contacts. One set of contacts opens to break the hold circuit on K13. The Sort Solenoid, L7, is now held in from Line 1 to contacts 7 and 8 of K4, to L7, to Cam F, to Line 2.

Cam F opens at 235° to break the hold circuit on L7 causing L7 to de-energize.

This two step procedure is required in a Sort Operation because the card is a complete Base Cycle away from the Receiving Magazine when the Sort Signal is released. This procedure also allows cards in sequence to all use Sort.

Skip

The purpose of Skip is to prevent punching by retaining the Set Bar Section in a retracted condition. This is done whenever the Skip Solenoid is energized.

The Skip Field is generally plugged from 70R through a Sensing Switch to the Bus. Cam H closes at 140° to pass the 70R voltage supply to the Skip Relay, K14, causing K14 to energize through Cam J which closed at 133°. Cam H is used to protect the Sensing Switches from making hot. The contacts on K14 transfer and contacts 7 and 8 on K14 are used to hold the Skip Relay, K14, energized through Cam J.

Line 1 through contacts 3 and 4 of K14 energizes the Skip Solenoid, L6, when Cam I closes at 287° which is the beginning of the next Punch Cycle. At 287° Cam I closes to energize the Skip Solenoid, L6. At this time the Punch is using the high

part of the Set Bar Retract Cam so operation of L6 locks the mechanism in this position. Cam I breaks at 73° but by this time the pressure prevents restoration of L6 linkage until the Punch arrives at the high part of the Set Bar Retract Cam. At 94° Cam J opens and the Skip Relay, K14, de-energizes.

Skip Program

This operation is identical to Skip Field as to the end result. In this operation Cam H is not used since Skip Program does not use a Sensing Switch. Skip Program is located on the Program Board. Selector Relay contacts are to be used to carry the 70R volt supply across the Skip Program hub. This operation could be used to prevent punching from the Program Control in place of a Control Hole.

Set Hold

The purpose of Set Hold is to prevent any Tower Retraction. The Non-Reset Solenoid, when energized, disables the Tower Retraction Linkage. The Set Hold generally operates in conjunction with Skip but could be operated independently.

The Set Hold hub has a 70R volt supply if Skip is operative and Cam H is closed. Set Hold can use either a Sensing Switch or a direct jumper to supply the 70R volts to K15. Cam J was closed at 133° so the Non-Reset Relay, K15, will energize. The Non-Reset Relay, K15, is held energized by its transferred contacts 7 and 8 through Cam J to ground.

Line 1 through contacts 3 and 4 of K15 and contacts 14 and 15 of K4 energizes the Non-Reset Solenoid L5, when Cam I closes at 287° which is the beginning of the next Punch Cycle. At 287° Cam I closes to energize the Non-Reset Solenoid, L5. At this time the Punch is on the low part of the Tower Retract Cam so the retract linkage is free to be disabled. Cam I breaks at 73° but by this time the Tower Retract Cam is fully operative so the retract linkage remains disabled. At 94° Cam J opens and the Non-Reset Relay, K15, de-energizes.

In the event Set Hold is to be used independent of Skip, only a Selector Relay contact should be used. The common of the relay contact should be plugged to a 70R volt bus (Skip Field) and the select contact to the K15 side of the Set Hold bus.

REPRODUCE AND SECONDARY REPRODUCE

Plate 56C

This plate shows the circuitry required to perform a Reproduce or Secondary Reproduce Operation. Relays K8, K12, K7, K2 and K9 are located in the Punch. Relays K211 and K213 are located in the Power Control.

A Reproduce Operation will clear all old Reproduce information by energizing the Reset Solenoids and then set up new information by pulsing the R hubs.

A Secondary Reproduce will only add in new information by pulsing the Secondary Reproduce Common.

The two types of Reproduce Operations enable information to be picked up from two cards but only one Reproduce Field is set up from each card.

In the event one card had both Reproduce and Secondary Reproduce controls only Secondary Reproduce would be effective.

Reproduce

The Reproduce hub can be plugged directly or, as shown, through a Sensing Switch. Once the Sensing Switch has closed there is a 70R voltage supply through contacts 4 and 5 of K8 to K12, through contacts 9 and 10 of K7 to Cam E to ground. Cam E is closed from 334° - 70°. Once Cam E closes the Reproduce Clear Relay, K12, is energized. Contacts 3 and 4 of K12 transfer to put an AC supply (Line 1) to the Reset Solenoids. The Reset Solenoids perform a mechanical operation to insure all Actuators will be reset by normal Tower Retraction.

Normally the B+ Failure Relay, K2, is energized but whenever B+ is removed in the Computer K2 drops out. K2 being de-energized, automatically, through its contacts 7 and 8, operates the Reset Solenoids L3 and L4. Whenever Plugboards are changed L3 and L4 pull in to automatically clear the Tower of any Reproduce information.

At 70° Cam E opens and the Reproduce Clear Relay, K12, de-energizes. The same 70R voltage supply from the Repr. hub also goes through K9 to Cam D to ground. Cam D is closed from 89° - 280°. Between 70° and 89° the Tower is retracted leaving all Actuators in the Tower normalized. At 89° Cam D closes to energize the Reproduce Set Relay, K9. Contacts 5 and 6 of K9 transfer to put +150 volts to K211.

A Trip Pulse from the Computer starts with stages ATT or ART, Either ARA3 or ATA will then conduct and since K9 is energized the Reproduce Power Relay, K211, will now energize. The contacts of K211 transfer changing the primary of T31 from ground to -165 volts. This change on the primary of T31 induces a lesser voltage (8:1) on the secondary of T31. The positive pulse on the secondary of T31 is fed to the common contacts of K213. K213 is de-energized so the positive pulse is released on the non-select contacts of K213 to the R position on the Field Board.

The R hub is plugged to the C hub of the column that is to be reproduced from. The R hub can also be plugged to the H position of the columns reproduced into, if the Reproduce information is to be retained for more than one card.

Secondary Reproduce

The Secondary Reproduce hub is plugged through a Sensing Switch to the Control Common. The closing of the Sensing Switch allows the Sec. Repr. hub to be grounded when Cam B is closed. Grounding the Sec. Repr. hub energizes the Repr. Transfer Relay, K213, and the Secondary Reproduce Relay, K8. K8 being energized transfers its contacts to prevent operation of K12, Reproduce Clear. Contacts 3 and 4 of K8 puts a 70R voltage supply through K9 to Cam D to ground. Cam D is closed from 89° - 280°. Any Reproduce information in the Tower is not retracted during this operation. At 89° Cam D closes to energize the Reproduce Set Relay, K9. Contacts 5 and 6 of K9 transfer to put +150 volts to K211.

A Trip Pulse from the Computer starts with stages ATT or ART. Either ARA3 or ATA will then conduct and since K9 is energized the Reproduce Power Relay, K211, will now energize. The contacts of K211 transfer changing the primary of T31 from ground to -165 volts. This change on the primary of T31 induces a lesser voltage (8:1) on the secondary of T31. The positive pulse on the secondary of T31 is fed to the common contacts of K213. K213 is energized during Secondary Reproduce so the select contacts of K213 feed the positive pulse to the Secondary Reproduce Common on the Field Board.

The Sec. Repr. Common is plugged to the C hubs of the columns to be reproduced from. The Repr. Common can also be plugged to the H hubs of the columns to be reproduced into if the information is to be held for more than one card.

The Sec. Repr. Common should never be plugged to the R hub as this would defeat the separation of the two operations.

POWER SUPPLY

Plate 59C

The Power Supply is located on the right end of the Computer. This section contains the components required to rectify the DC Voltages required in the Computer Circuitry.

The Power Supply is shown on plate 59. Above TB114 is where all the rectifier tubes are located. Transformer T21 is the filament transformer for these rectifier tubes. TB117 is the terminal for adjustment of the primary of T21 for proper rectifier filament voltage.

TB113 has the secondary connections for T25 for -375 and -60 volt supplies.

TB112 has the primary connections for;

1. T25 for adjustment of -15, -60, -375 and -25 volt supplies.
2. T24 for adjustment of -90 and -150 volt supplies.
3. T30 and the rest of T30 is on TB111 for adjustment of the +75 volt supply.

TB111 has the primary connections for;

1. Remainder of T30 for adjustment of the +75 volt supply.
2. T22 for adjustment of the -165 volt supply.
3. T23 for adjustment of the +150 volt supply.

The primary adjustments are shown on plate 51, 52.

A blown resistor on this panel generally indicates a filament to cathode short in a tube supplied from the filament voltage which had used the blown resistor.

TB118 has the secondary connections for T24 for -90 and -150 volt supplies.

TB119 has the secondary connections for;

1. T30 for the +75 volt supply.
2. T22 for the -165 volt supply.
3. T23 for the +150 volt supply.

TB122 is used to connect the -15 volt and -25 volt selenium rectifiers.

TB110 has one side of the -165 volt supply choke L22, terminals for the Plus and Minus Voltage Check and all DC voltage terminals except -165 and -40 volts.

The Fuse Panel contains the fuses for the DC voltage supplies except -165 whose fuse is behind the Fuse Panel in the Power Control. The Fuse Panel is hinged to swing forward and behind this Panel are the relays used in the Plus and Minus Voltage

Check as explained on plate 50. K119 is also located in this section. K119 breaks the 115 volt AC supply to the Selector Relays whenever the DC Voltages are not present.

TB121 contains the DC voltage connections from the various chokes before being fused. L27 (-15), L23 (-90), L24 (-150) and L22 (-165) choke connections are on TB121.

TB120 contains the connections for L28 (+75), L21 (+150), L26 (-375) and L25 (-60) chokes.

POWER CONTROL

Plates 61C and 62C

The Power Control section of the Computer is located at the left end below the PTP Panel.

Directly below the PTP Panel on plate 61 is the Voltmeter Panel. On this panel are located an AC Voltmeter (M203), Running Time Meter (M202) and a Voltmeter (M201). Below the meters are two switches S204 and S203. S204 is used to read the AC voltages and S203 is used to read the DC voltages.

The Voltmeter Panel is hinged to swing forward. Behind the Voltmeter Panel, on the left, is the Reference Regulator Chassis which is the -40 Volt regulated supply. R212 is used to adjust for -40 volts. Behind the Voltmeter Panel, on the right, is the Timing Assembly which is used in the Calculator Crank Up and is explained in detail on plate 50.

On plate 62 the Power Control Section continues showing the RCS Chassis Assembly located below the Voltmeter Panel. V211, V212, V213 and V214 are the Select Thyratrons 1 to 4 respectively. Cages CG203 and CG204 are the grid bias and cathode returns for the Select Thyratrons. K211 is the Reproduce Power Relay. K212 is the Manual Clear Relay. K213 is the Reproduce Transfer Relay. K214 is a spare relay. T28 is the Filament Supply Transformer for the Select Thyratrons and -40 volt supply tubes. T31 Transformer is the Reproduce Pulse Transformer and CR203 is a selenium rectifier across the primary of T31. TB204 on terminals 10 through 15 are the primary taps for T28 to adjust for proper filament voltage.

Relays K202 and K203 are on the rear deck and K204, K206 and K207 on the front deck. These relays are used in the Calculator Crank Up and are explained in detail in plate 50.

The Fuse Panel from F201 to F210 are also shown in detail in the Calculator Crank Up on plate 50.

The Fuse Panel is hinged to swing forward and behind this Fuse Panel, though not shown, are components used in the -165 volt supply which are shown on plate 51 within the dotted line area.

Below the Fuse Panel is the filter capacitor assembly for the -165 volt supply.

TB208 and TB209 are connected by cable to the Punch.

Factory print 1940250 shows the wiring on the Power Control.

COMPUTER WIRING DISTRIBUTION

Plate 65C

This plate shows the wiring to the various sections of the Computer. The detailed wiring in the various sections can be found on the factory prints as labeled. The chassis that the various sections control are shown on plates 57 and 58 . By use of this plate, plates 57 and 58 and the factory prints, it is possible to trace the wiring within the Computer.

The factory print numbers each contain 3 prints. The 3 prints show all wiring within a specific section.

This plate is for reference purposes to assist in tracing the Computer wiring. For example, suppose all J Section connections are to be traced. Factory print #1940400 will show all J Section wiring. This plate shows that;

1. T26D and T27 transformers supply the filaments of J section.
2. J section connects to E section via the J Blocks.
3. J section connects to J429 in the D section.
4. J section connects to the Storage Door.
5. J Blocks in J Section connect to the Minus and Input Neons.
6. J Section connects to J Block 430 in Power Supply to pick up D.C. supply.

ELECTRONIC COMPUTER

UNIVAC 60 & 120

ALPHA STAGE INDEX

STAGE NAME	CAGE TYPE	CHASSIS LOCATION	STAGE NAME	CAGE TYPE	CHASSIS LOCATION
Ø9C	DD-20	ØF	ACT	T -1	OCL1
Ø9C1	X	ØF	AGA	AA-2	OCL2
Ø9M	DD-1	ØF	AGD	DD-7	OCL2
Ø9SM	DD-1	ØF	AGF1	F -3	OCL2
Ø9SM1	DD-7	ØF	AGF1'	RC-13	OCL2
ØC2	GA-7	ØF	AGF2	F -3	OCL2
ØESP	AA-1	ØF	AGF2'	RC-13	OCL2
ØEZ	GG-21	ØF	AGK	K -3	OCL2
ØEZ1	GG-2	ØF	AGT	T -4	OCL2
ØF1	T -1	ØF	AGTZ	DA-2	OCL2
ØF2	GA-1	ØF	ANRI	RC-42	OCL1
ØF3	GA-1	ØF	ANR2	RC-42	OCL1
ØF4	GG-18	ØF	AP3	S -1	OCL2
ØF5	G(-)-2	ØF	APC1	RC-14	OCL2
ØFD1	F -1	ØF	APC2	RC-22	OCL2
ØFD3	X	ØF	APC3	RC-14	OCL2
ØFM	RC-17	ØF	APD1	DD-1	OCL1
ØFR1	DD-1	ØF	APD2	DD-1	OCL1
ØFR2	DD-7	ØF	APD3	DD-1	OCL1
ØFS	F -1	ØF	APD4	DD-1	OCL1
ØFZD	F -3	ØF	APGA	GG-4	OCL1
ØFZT	RC-19	ØF	APGB	GG-4	OCL1
ØLD1	RC-1	ØF	APGL	RC-2	OCL1
ØLD2	X	ØF	APGM	RC-2	OCL1
ØMD	T -1	ØF	APMA	AA-2	OCL1
ØRS	T -5	ØF	APMB	AA-2	OCL1
ØRSZ	GG-4	ØF	APT1	T -1	OCL1
ØSR	T -1	ØF	APT2	T -1	OCL1
AAD	DD-1	OCL1	APT3	T -1	OCL1
AAF1	F -3	OCL1	APT4	T -1	OCL1
AAF2	F -3	OCL1	ARA1	DD-7	OCL2
AAF2'	RC-13	OCL1	ARA2	RC-31	OCL2
AAG	GG-4	OCL1	ARA3	X	OCL2
AAGL	RC-2	OCL1	ARG	GG-1	OCL2
AAK1	DD-7	OCL1	ARGI	AA-2	OCL2
AAK2	DD-7	OCL1	ARM	AA-15	OCL2
AAM	AA-2	OCL1	ARR	RC-1	OCL2
AAR	RC-13	OCL1	ART	T -1	OCL2
AAT1	T -1	OCL1	ARY	DD-7	OCL2
AAT2	T -1	OCL1	ARZ	DD-1	OCL2
AC	DA-2	ACC	ASA1	RC-2	OCL1
ACG	GG-4	OCL1	ASA2	RC-2	OCL1
ACI	AA-2	OCL1	ASC	DD-1	OCL1
ACI'	X	OCL1	ASD	DD-1	OCL1
ACM	DA-5	OCL1	ASG	GG-4	OCL1

STAGE NAME	CAGE TYPE	CHASSIS LOCATION
ASM	AA-2	OCL1
AST1	T -1	OCL1
AST2	T -1	OCL1
ATA	X	OCL1
ATM1	DA-5	OCL1
ATM2	AA-2	OCL1
ATR	RC-14	OCL1
ATT	T -4	OCL1
B11+	K -2	SB
B11-	K -2	SB
B11+1	RC-27	SB
B11-1	RC-27	SB
BA+	K -2	SB
BA-	K -2	SB
BA+1	RC-27	SB
BA-1	RC-27	SB
BM+	K -2	SB
BM-	K -2	SB
BM+1	RC-27	SB
BM-1	RC-27	SB
CØCS	T -1	CTL
CØD	F -2	CTL
CØDA	F -2	CTL
CØDD	DD-1	CTL
CØDE	DD-7	CTL
CØDG	GG-1	CTL
CØG	GG-21	CTL
CØPG	GG-1	CCTL
C11M	S -1	CCT
C17	LL-3	IO
C35	X	IO
C9D	F -2	CTL
C9G	GA-1	CTL
C9R	X	RIG
C9T	T -1	CTL
CA	DD-8	DCR
CA1	RC-1	DCR
CAS	RC-1	CCT
CB	S -1	DCR
CCC	DD-1	CCT
CCM	DD-1	CCT
CD	F -5	RIG
CDA	AA-10	RIG
CGA	DD-24	CCT
CM	M -2	DCR
CMA	DA-1	DCR
CO9	X	IO
CPMD	DD-7	CTL
CS	GG-2	DCR
CSK	C -1	DCR
CT	T -1	DCR
CT1	T -3	CCT
CT2	T -3	CCT
CT4	T -3	CCT
CT8	T -3	CCT
CT1Ø	T -1	CCT
CT11	T -1	CCT
CTG	GG-1	CCT
CTSG	GG-22	CCT
CX	GG-6	DCR
D2-14	GG-24	DCR
D2-4C	GG-24	DCR
D8-16C	GG-24	DCR
D8-16T	GG-24	DCR
DA1-16	AA-16	DCL
DAM	T -4	DCL
DAS	T -4	DCL
DAX	T -3	DCL
DB2	AA-1	DCR
DB4	AA-15	DCR
DB8	AA-1	DCR
DB16	GA-3	DCR
DBC	K -3	DCL
DBT	K -3	DCL
DC1	T -3	DCR
DC2	T -3	DCR
DC4	T -3	DCR
DC8	T -3	DCR
DC16	T -3	DCR
DCC	T -4	DCR
DCCD	F -1	DCR
DCCL	X	DCR
DCK	RC-49	CCT
DCK1	RC-49	CCT
DCK2	RC-49	CCT
DEA	F -3	DCL
DEA1	AA-2	DCL
DEA2	AA-2	DCL
DEM	S -1	DCL
DG	GG-29	DCL
DI1	GG-23	DCR
DIC	GA-7	DCR
DK	T -3	DCL
DKG	GG-22	DCL
DMD	DD-1	DCL
DMG	GG-1	DCL
DMP	S -1	DCL
DN12'	RC-22	DCR
DN2-16'	X	DCR
DN4'	X	DCR
DN48'	RC-50	DCR
DNB-16	X	DCR
DP1	F -1	DCR
DP2	F -1	DCR
DP4	F -1	DCR
DP8	F -1	DCR

	STAGE NAME	CAGE TYPE	CHASSIS LOCATION
	DP16	F -1	DCR
	DPG1	GA-11	DCL
	DPG2	GA-11	DCL
	DRB	T -4	DCL
	DRP	S -1	DCL
	DRR1	RC-53	VAD
	DRR2	X	VAD
	DRR3	X	VAD
	DRR4	RC-53	VAD
	DRS	T -1	DCL
	EØCA	GA-6	SB
	EØCB	DD-12	SB
	EBG	GG-6	ZCL
	EBM	K -3	ZCL
(1, 2)	EBM	X	SS
(3, 4)	EBM	X	SS
	EBP	K -3	ZCL
(1, 2)	EBP	X	SS
(3, 4)	EBP	X	SS
	EBS	T -1	ZCL
(1, 4)	EC	RC-23	SS
	ECB1	DD-1	CTL
	ECB2	RC-54	CTL
	ECS	AA-1	CTL
(1, 2)	ED	GG-4	SS
(3, 4)	ED	GG-4	SS
	EDPZ	F -4	CTL
	EGD	F -4	SCL
	EIA	DD-7	DCL
	EIA1	X	DCL
	EIA2	X	DCL
	EIA3	X	DCL
	EID	DD-7	DCL
	EID1	X	DCL
	EID2	X	DCL
	EIM	DD-7	DCL
	EIM1	X	DCL
	EIM2	X	DCL
	EIS	DD-7	DCL
	EIS1	X	DCL
	EIS2	X	DCL
	EM	T -4	CTL
	EMA	DD-7	CTL
	EMDC	GA-9	CTL
	EMDZ	F -3	CTL
(1, 2)	EMF	RC-2	SS
(3, 4)	EMF	RC-2	SS
	EMK	K -3	CTL
	EMZ	F -3	CTL
	EMZ'	RC-19	CTL
	ENM	AA-6	CTL
	ENM1	AA-6	CTL

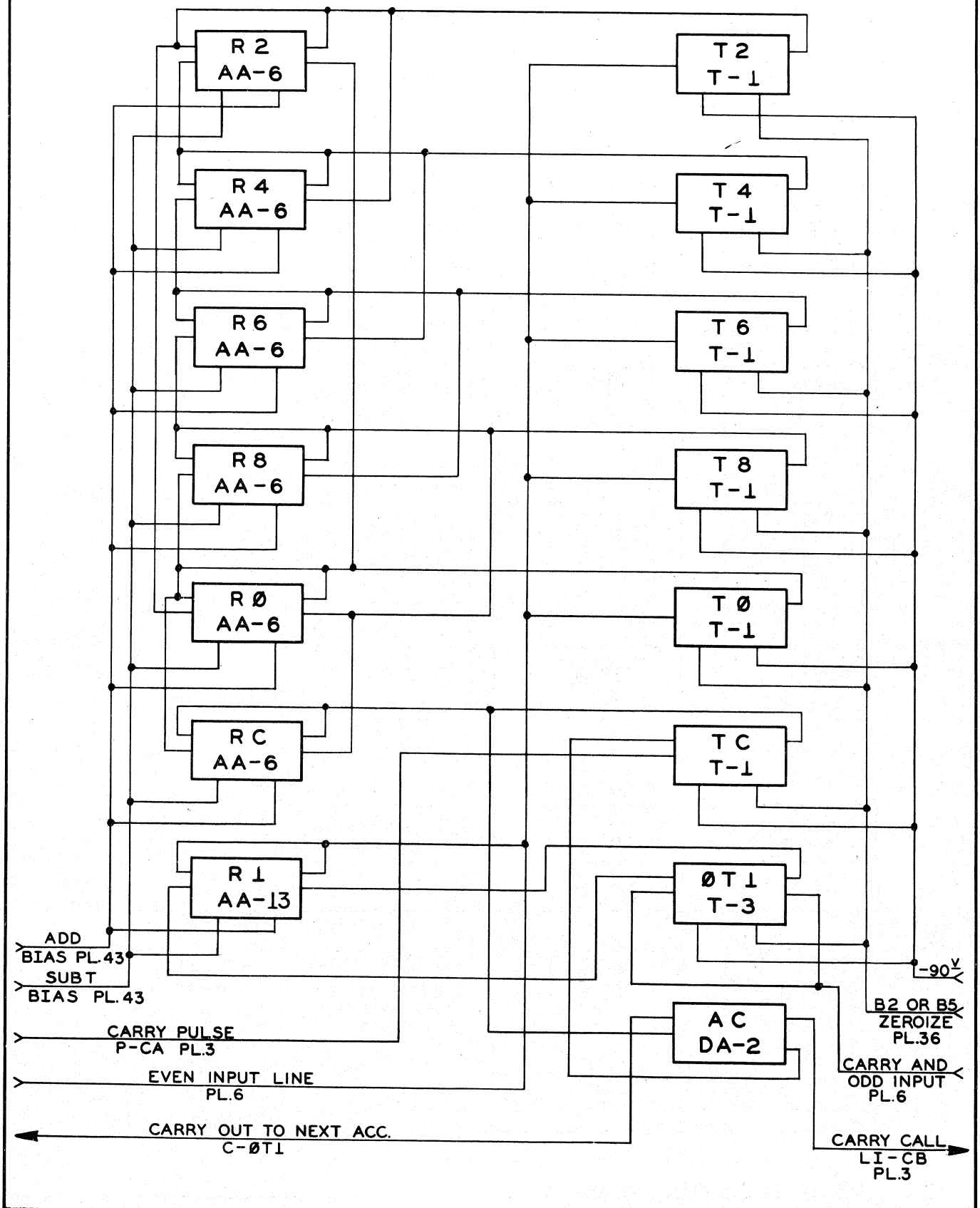
	STAGE NAME	CAGE TYPE	CHASSIS LOCATION
	EP	F -3	SCL
	EP'	RC-19	SCL
	EP1	DD-7	DCL
	EP2	DD-7	DCL
	EP3	T -4	SCL
	EP3C	RC-16	SCL
	EP4	F -3	SCL
	EP4'	RC-11	SCL
	EP5	GG-28	SCL
(1, 2)	EPF	X	SS
(3, 4)	EPF	X	SS
	EPG	AA-11	CTL
	EPM	T -4	CTL
	EPMA	DD-7	CTL
	EPP	T -4	CTL
	EPP1	DD-7	DCL
	EPP2	DD-7	DCL
	EPPM	X	DCL
	EPR	RC-14	SCL
	EPS	T -4	CTL
	EPX	DD-4	SCL
	EPX'	RC-9	SCL
	EPZ	F -3	CTL
	EPZC	RC-11	CTL
	ER	T -4	CTL
	ERA	DD-1	CTL
	ERAZ	DD-7	CTL
(1, 2)	ERF	X	SS
(3, 4)	ERF	X	SS
	ERK	K -3	CTL
	ES	T -4	CTL
(1)	ES	T -1	SS
(2)	ES	T -1	SS
(3)	ES	T -1	SS
(4)	ES	T -1	SS
	ESA	DD-1	CTL
	ESB1	DD-1	SCL
	ESCG	GA-9	CTL
	ESD	F -3	SCL
(1, 2)	ESF	DD-9	SS
(3, 4)	ESF	DD-9	SS
	ESI1	AA-11	SCL
	ESI2	RC-1	SCL
	ESI3	RC-19	SCL
	ESIA	AA-16	SCL
	ESK	K -3	CTL
	ESZ	AA-2	SCL
	ESZ1	AA-2	SCL
	ESZA	AA-16	SCL
	EZ	F -6	CTL
	EZB2	F -2	CTL
	EZB5	F -2	CTL

STAGE NAME	CAGE TYPE	CHASSIS LOCATION
EZB5'	RC-55	CTL
EZG	AA-2	CTL
FA (1, 2)	DD-14	STL
FB (1, 2)	DD-17	STL
FC (1)	DD-22	STL
FC (2)	RC-45	STL
FD (1, 2)	X	STL
FK-1	K -13	STL
FK-2	K -13	STL
I-1-11	GG-7	RIG
I35	GG-28	IO
I79	GG-28	IO
I9	AA-4	IO
IA9	DL-1	IO
ICC	RC-40	ZCL
ICL	F -2	ZCL
ICP	RC-23	ZCL
INV	DD-1	VAD
IO9	AA-3	IO
IOC	RC-48	CCT
IOCK	D -3	CCT
IS-1	DK-1	IO
IS-3	DK-1	IO
IS-5	DK-1	IO
IS-7	DK-1	IO
IS-9	DK-1	IO
KB (1)	K -8	KB
KB (2)	K -8	KB
KB (3)	K -8	KB
KB (4)	K -8	KB
KB (5)	K -8	KB
KB (6)	K -8	KB
KB (7)	K -8	KB
KB (8)	K -8	KB
KB (9)	K -8	KB
KB (10)	K -8	KB
KB (11)	K -8	KB
KB (12)	K -8	KB
KBA (1, 2)	DD-14	KB
KBA (3, 4)	DD-14	KB
KBA (5, 6)	DD-14	KB
KBA (7, 8)	DD-14	KB
KBA (9, 10)	DD-14	KB
KBA (11, 12)	DD-14	KB
KBR (1, 2)	X	KB
KBR (3, 4)	X	KB
KBR (5, 6)	X	KB
KBR (7, 8)	X	KB
KBR (9, 10)	X	KB
KBR (11, 12)	X	KB
M (S1)	RC-40	STL
M (S1) A	RC-40	STL
M (S2)	RC-40	STL
M (S2) A	RC-40	STL
MØCC	X	IO
M9	X	IO
M13	X	IO
M17	X	IO
M35	X	IO
M57	RC-30	IO
MA (1, 2)	K -12	STL
MA9	D -3	IO
MC (1)	RC-31	STL
MC (2)	RC-31	STL
MC1	GG-20	ØF
MC2	T -1	ØF
MC3	GG-4	ØF
MC4	DD-7	ØF
MC4L	X	ØF
MC5	DD-1	ØF
MC6	DA-1	ØF
MC7	DD-7	ØF
MC8	DD-7	ØF
MCP1	RC-14	RIG
MCP2	RC-14	RIG
MCX	X	ØF
ME	K -14	IO
MF (1, 2)	RC-39	STL
MKD (1)	RC-37	STL
ML (S1, 2)	RC-46	STL
MO	K -14	IO
MR (S1, 2)	DD-18	STL
MS	F -3	DCL
MS'	X	DCL
MSA	DA-5	DCL
MSD	DD-14	CCT
MSI	DD-1	DCL
MSK	K -6	DCL
MSKA	RC-14	ZCL
MSKK	C -3	ZCL
MSKP	RC-45	ZCL
MST	T -2	DCL
MXR	DD-7	VAD
MXR3	RC-16	VAD
MZ (1)	F -3	STL
MZ (2)	F -3	STL
MZ (A)	GG-8	STL
MZR	DD-7	DCL
MZT	T -4	DCL
OTP	RC-45	VAD
OTP1	DD-7	VAD
P115	T -2	MD
P11C	DA-7	MD
P11G	K -3	MD

STAGE NAME	CAGE TYPE	CHASSIS LOCATION
PABA	DD-7	SB
PABA1	DD-7	SB
PABS	DD-7	SB
PABS1	DD-7	SB
PAC	T -3	ØF
PAM	T -1	SB
PAMD	F -6	CTL
PAT	T -3	ØF
PC1	T -3	MD
PC2	T -3	MD
PC4	T -3	MD
PC8	T -3	MD
PC16	T -3	MD
PCG	GA-7	MD
PD1	T -4	MD
PD1M	RC-1	MD
PD2	T -4	MD
PD2D	F -1	MD
PD3	T -1	MD
PDA	DD-13	MD
PDAM	F -1	SB
PDB	T -2	MD
PDM	GA-6	MD
PDM3	AA-9	MD
PDMS	GG-2	MD
PDN	T -2	MD
PDND	F -1	MD
PDP	S -1	MD
PDS	T -4	MD
PDT	T -4	MD
PDX	GG-2	MD
PGMD	GA-4	MD
PIAS	RC-17	ØF
PIMD	RC-17	ØF
PMØ	S -1	MD
PMØD	F -1	MD
PM1	T -2	MD
PM2	T -1	MD
PM3	F -1	MD
PM12	GG-6	MD
PM22	DD-12	MD
PM23	DA-6	MD
PMBT	T -1	MD
PMD1	F -4	MD
PMD2	F -1	MD
PMDR	GG-2	MD
PMDZ	T -4	MD
PMG	GG-1	MD
PMM	AA-2	MD
PMP	S -1	MD
PMS	DD-3	MD

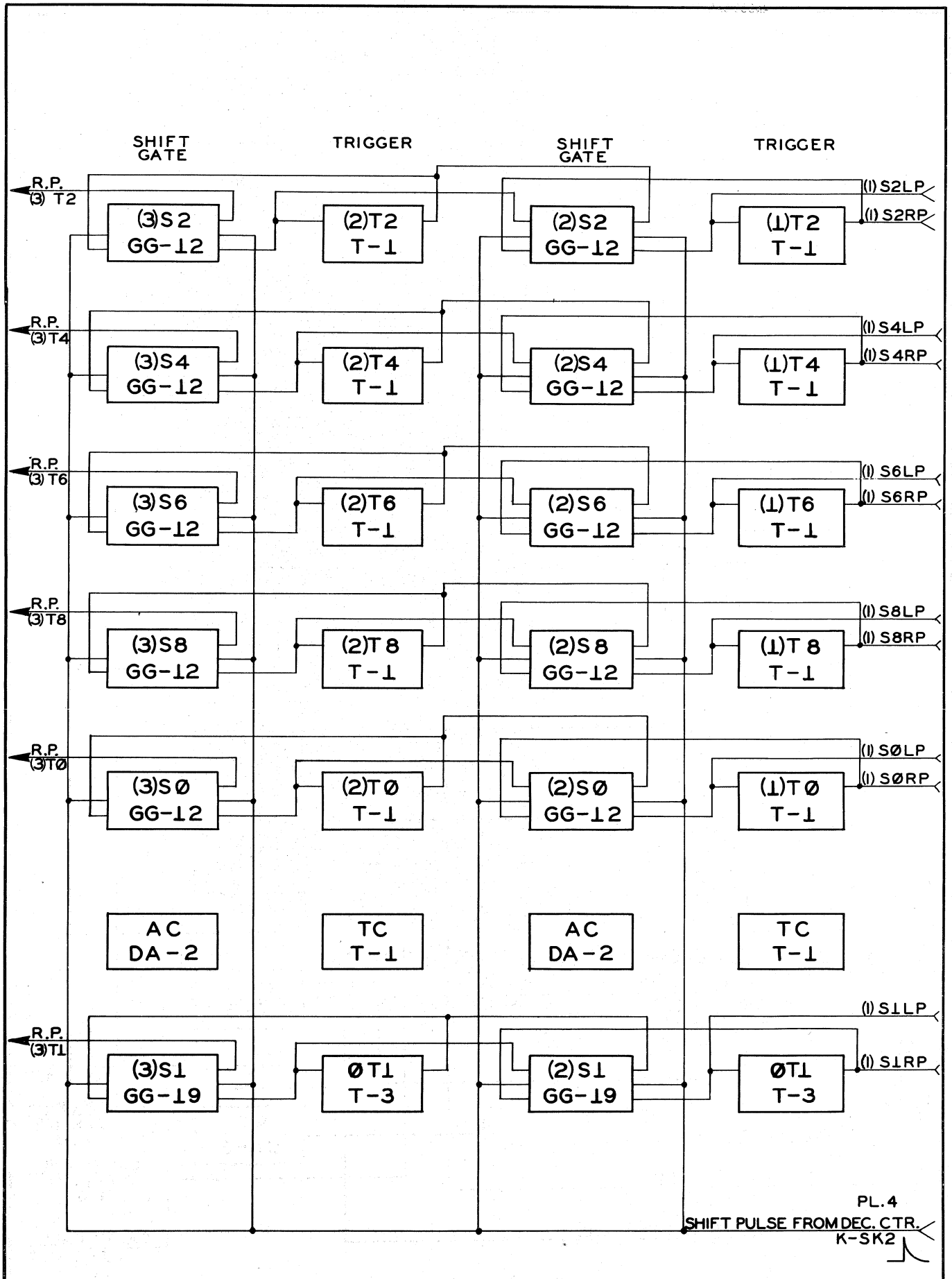
	STAGE NAME	CAGE TYPE	CHASSIS LOCATION
	PPI	DD-21	ØF
	PS	GG-1	ØF
	PS11	S -1	MD
	PSA	DD-1	SB
	PSAC	LL-2	SB
	PSG	DD-1	MD
	PSGK	K -3	MD
	PSIG	GA-1	ØF
	PSOC	GG-1	CCT
	PT1	T -4	SCL
	PT2	GG-22	SCL
	PT3	F -1	SCL
	PT4	S -1	SCL
	PT5	RC-14	ZCL
(1, 4)	PTR	RC-42	SS
	PX	X	RIG
	PZG	GA-7	MD
	RØ	AA-6	ACC
	R1	AA-13	ACC
	R1	T -4	RIG
	R1' 1'	K -4	RIG
	R1' 8	AA-8	RIG
	R1M	DA-3	RIG
	R2	AA-6	ACC
	R2	T -3	RIG
	R4	AA-6	ACC
	R4	T -3	RIG
	R6	AA-6	ACC
	R8	AA-6	ACC
	R8	M -2	RIG
	R42	AA-10	RIG
	R11	K -4	RIG
	R22	K -4	RIG
	R44	K -4	RIG
	R66	K -4	RIG
	R88	K -4	RIG
	RB	AA-14	SB
	RBK	RC-18	SB
	RC	AA-6	ACC
	RD	F -2	RIG
	RS	F -1	RIG
	SØ	GG-12	ACC
	S (1)	X	STL
	S (2)	X	STL
	S1	GG-19	ACC
	S2	GG-12	ACC
	S4	GG-12	ACC
	S6	GG-12	ACC
	S8	GG-12	ACC
	SCK	RC-16	DCR
	SCK1	RC-1	DCR

STAGE NAME	CAGE TYPE	CHASSIS LOCATION
SG	GA-8	DCR
SI-1	RC-11	MD
SI-2	X	DCL
SK1	C -2	DCR
SK2	RC-52	DCR
SK3	RC-51	DCR
SKBH	DD-14	CCT
SKBK	K -14	CCT
SM	M -1	DCR
SMA	-A-3	DCR
SMC	X	DCR
SMG	AA-1	DCR
SRC (1)	RC-35	STL
SRC (2)	RC-35	STL
SRC (A)	R -5	STL
SSG (S1, 2)	KK-1	STL
SSK	RC-23	CCT
SSRO	DK-1	CCT
SZK	C -1	CTL
TØ	T -1	ACC
T1	T -3	ACC
T1	T -3	TCR
T2	T -1	ACC
T2	T -1	TCR
T2	T -3	TCR
T4	T -1	ACC
T4	T -3	TCR
T6	T -1	ACC
T8	T -1	ACC
T1Ø	T -3	TCR
T20	T -3	TCR
T2Ø	T -1	TCR
T4Ø	T -3	TCR
TB	T -2	TCR
TC	T -1	ACC
TC1	T -3	TCR
TC2	T -3	TCR
TDG	GG-14	TCR
TG	GK-1	TCR
THY1	RC-46	VAD
THY2	RC-9	VAD
TK	K -3	TCR
TS	T -2	TCR
TSA	AA-1	TCR
TSAL	RC-1	TCR
TSP	S -1	TCR
TUG	GG-14	TCR
VTB2	X	ZCL
VTB5	X	ZCL
VTIC	X	ZCL
ZB52	R -1	ZCL
ZD52	DD-23	CTL
ZR2	R -3	ZCL
ZR5	R -3	ZCL



ADDITION & SUBTRACTION

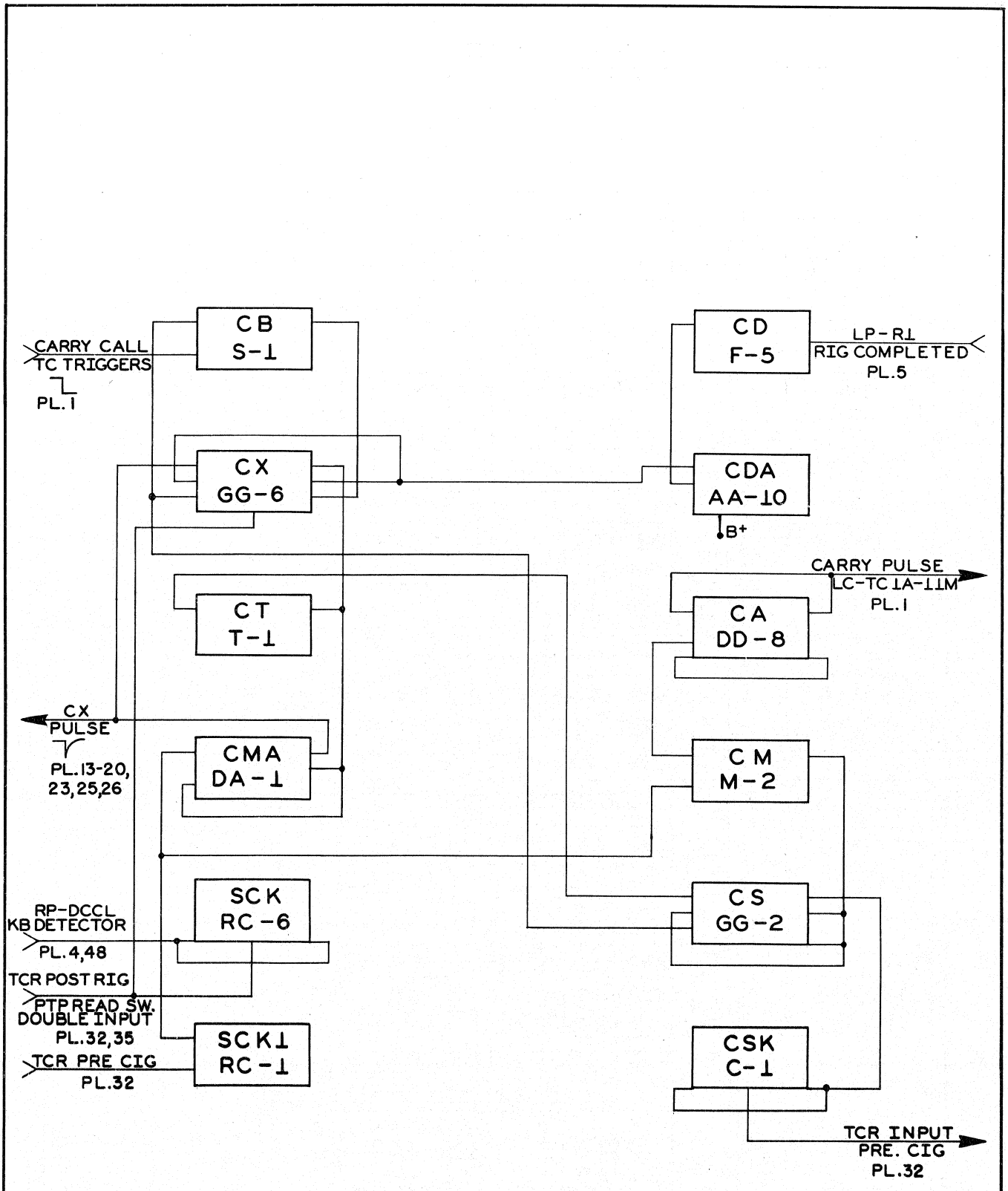
PLATE 1C



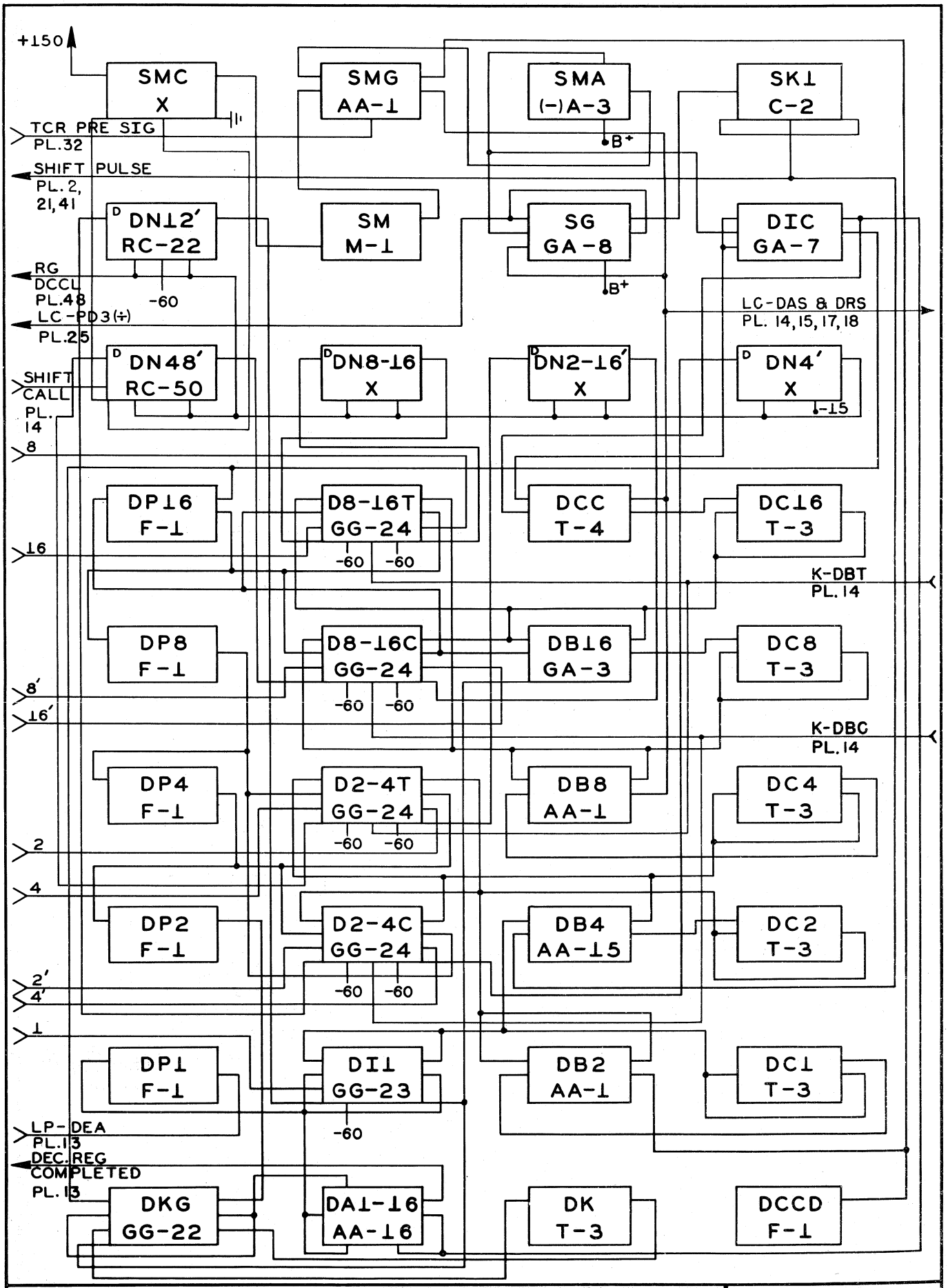
NOTE: COL. 11M CONNECTED TO COL. 1A

ACCUMULATOR SHIFT MECHANISM

PLATE 2C

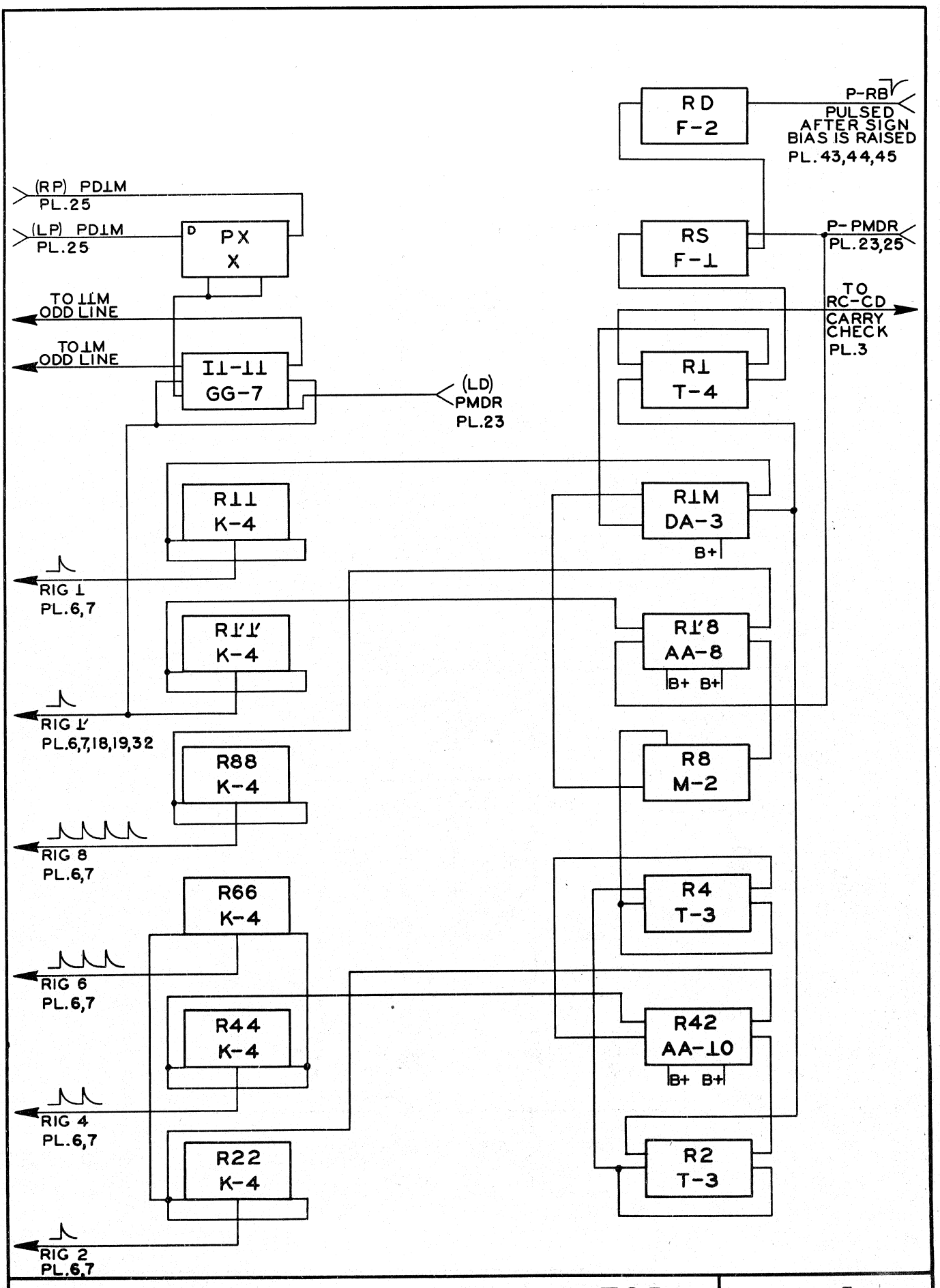


CARRY INPUT GENERATOR | PLATE 3C

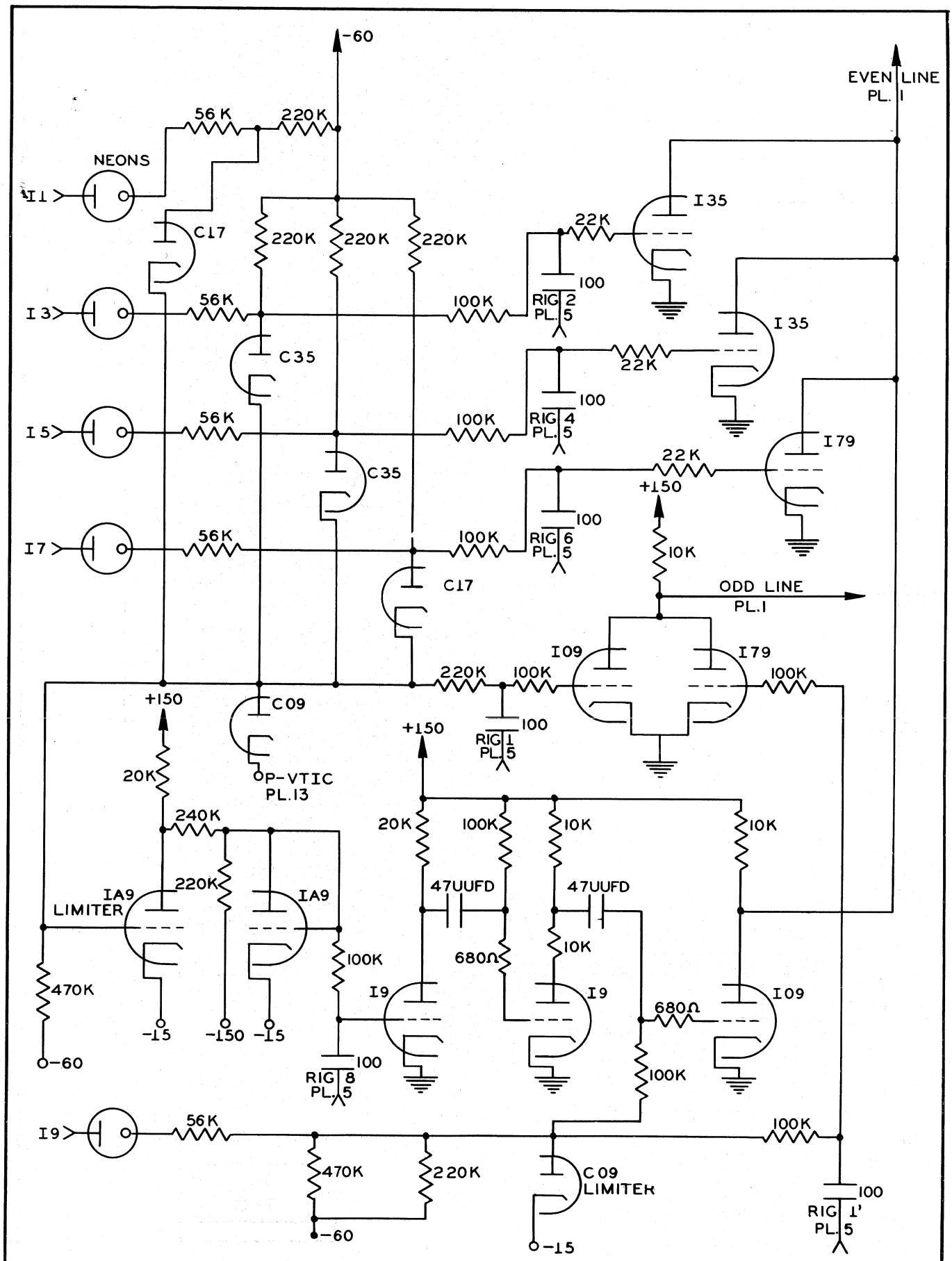


DECIMAL REGISTRATION & SHIFT OPERATION

PLATE 4 C

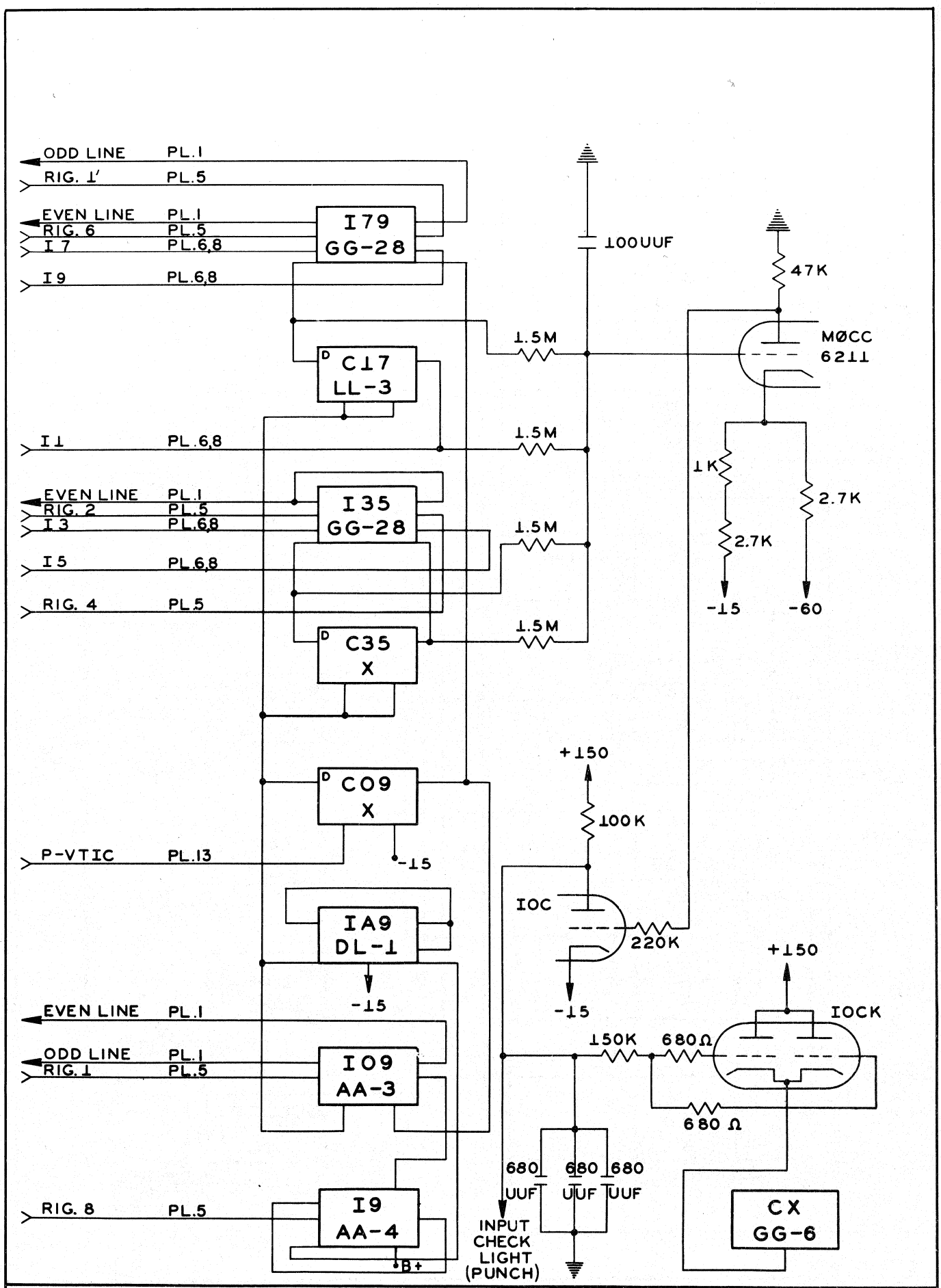


REGISTRATION INPUT GENERATOR | PLATE 5C



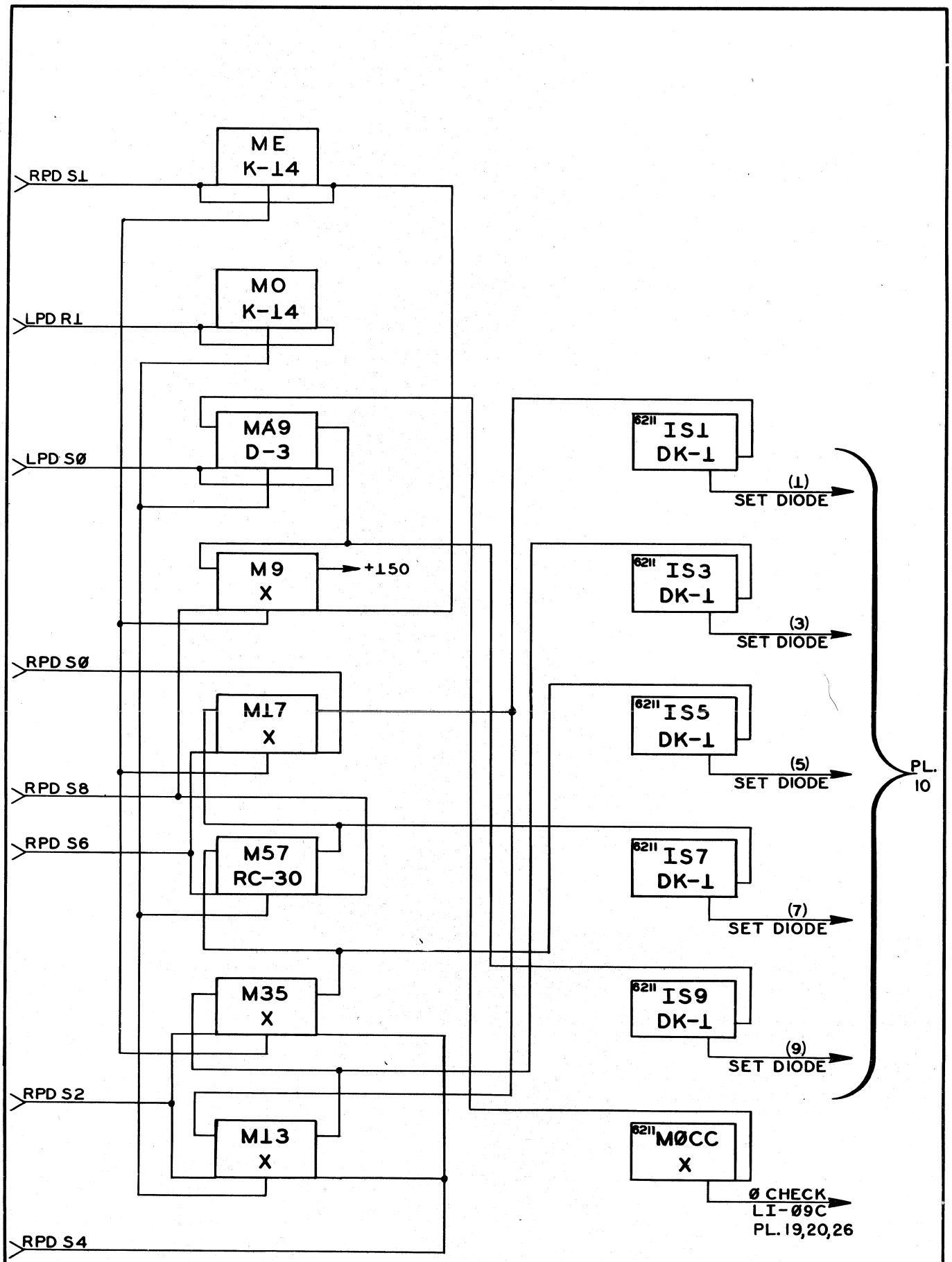
INPUT CIRCUIT

PLATE 6 C



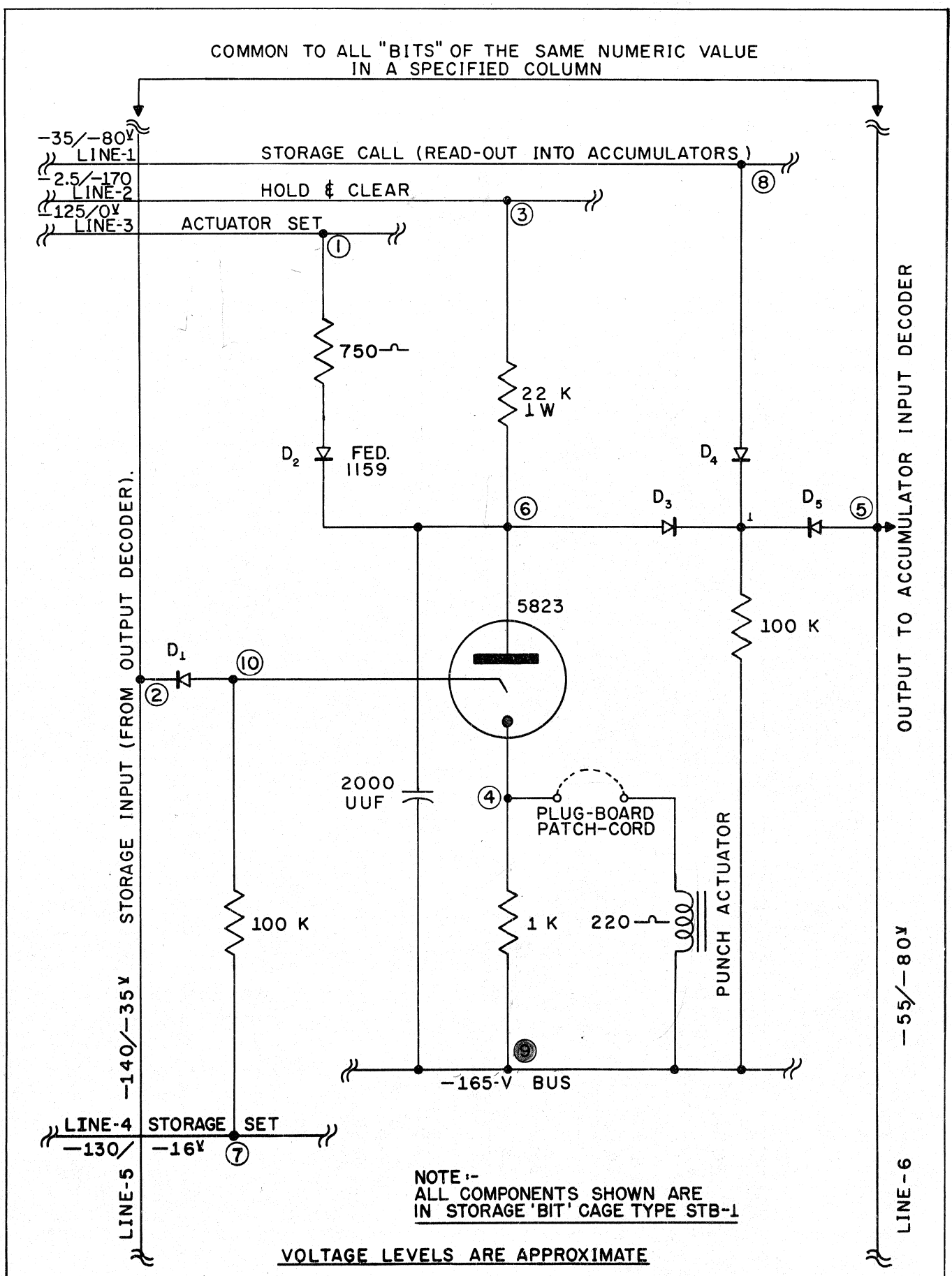
DOUBLE INPUT (ALPHA) CHECK

PLATE 7C



OUTPUT DECODER

PLATE 8 C



STORAGE BIT CONTROLS.	PLATE 9C

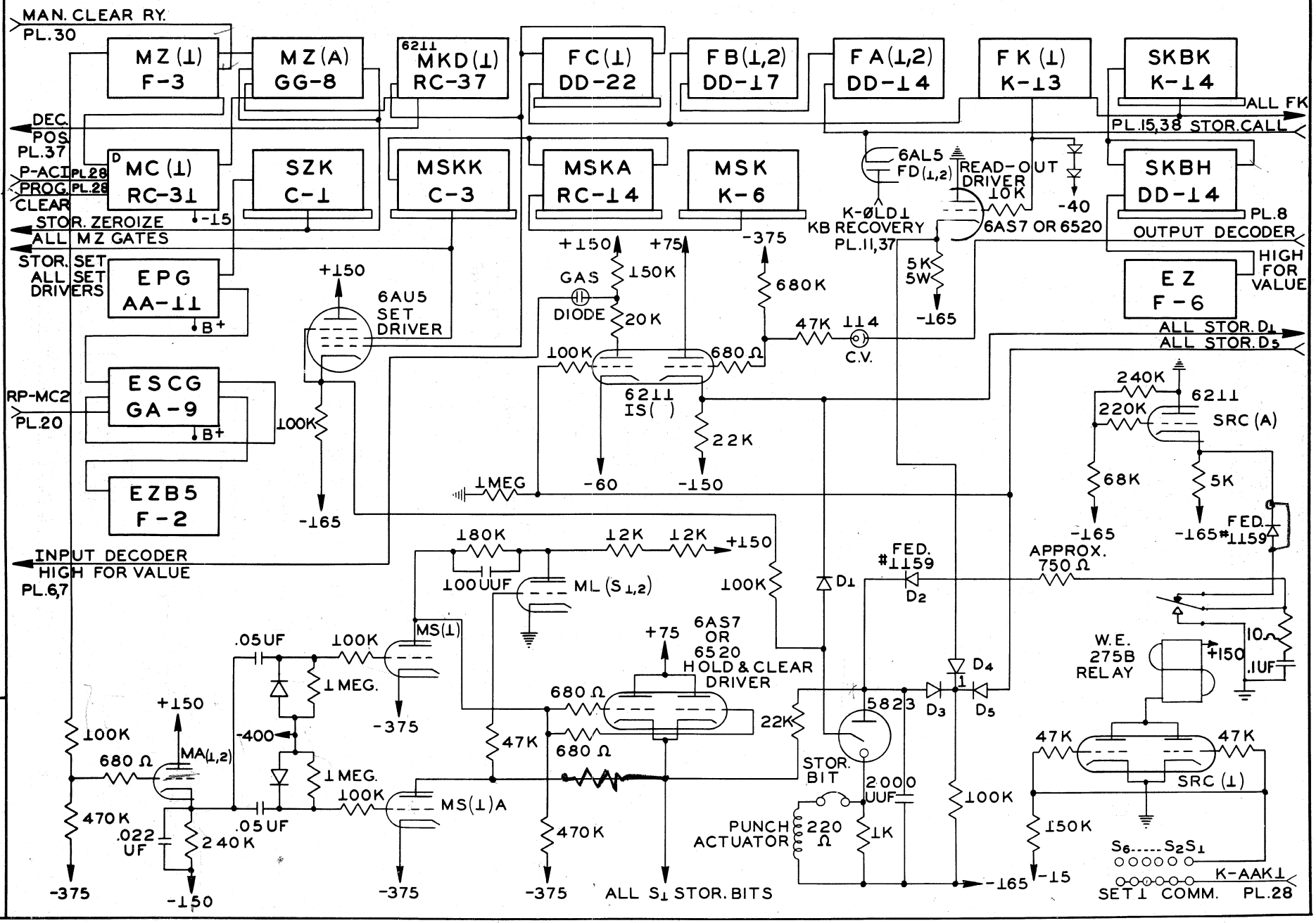
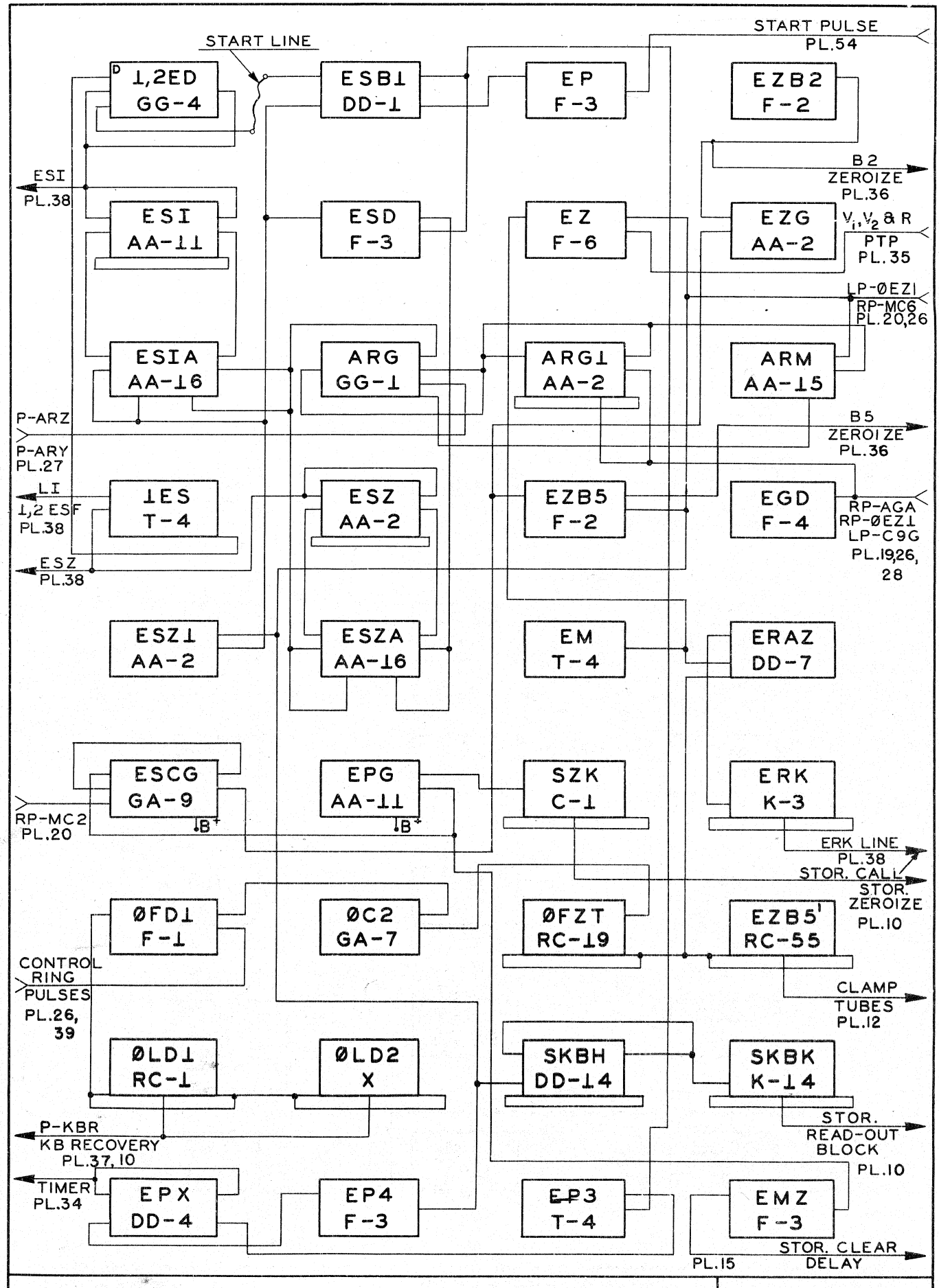
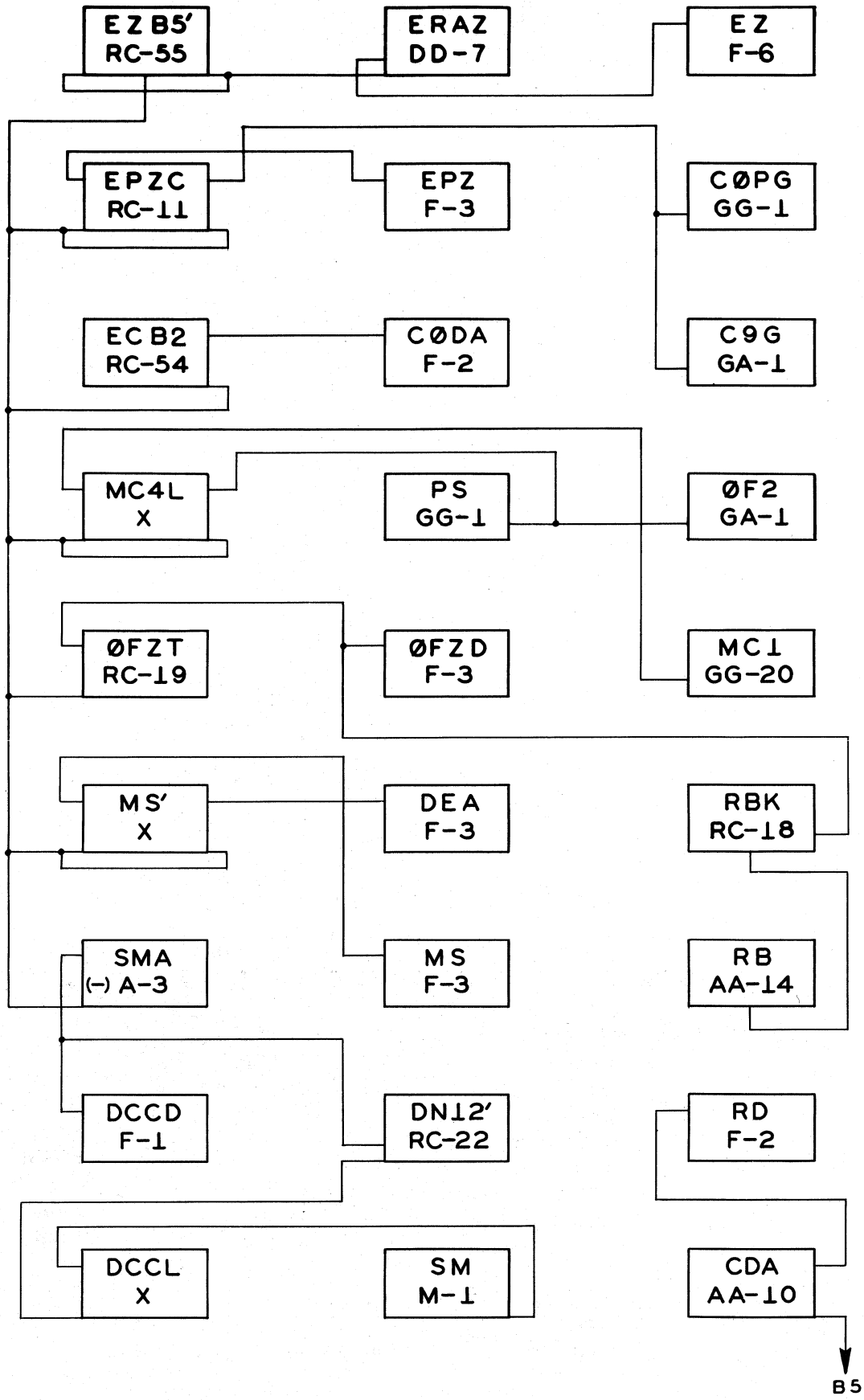

MAN. CLEAR RY. PL.30
MZ (1) F-3
MZ (A) GG-8
6211 MKD (1) RC-37
FC (1) DD-22
FB (1,2) DD-17
FA (1,2) DD-14
FK (1) K-13
SKBK K-14
ALL FK
PL.15,38 STOR.CALL
DEC. POS. PL.37
P-ACI PL.28
PROG. PL.28
CLEAR STOR. ZEROIZE
ALL MZ GATES
D MC (1) RC-31
-15
SZK C-1
MSKK C-3
MSKA RC-14
MSK K-6
6AL5 FD (1,2)
READ-OUT DRIVER
10K
-40
K-ØLD1 KB RECOVERY PL.11,37
6AS7 OR 6520
SKBH DD-14
PL.8 OUTPUT DECODER
HIGH FOR VALUE
STOR. SET ALL SET DRIVERS
EPG AA-11
B+
+150
6AU5 SET DRIVER
+150
+75
-375
GAS
DIODE
150K
20K
680K
5K 5W
-165
EZ F-6
47K
114
C.V.
ALL STOR. D1
ALL STOR. D5
100K
680Ω
6211 IS( )
22K
-60
-150
1MEG
240K
220K
6211 SRC (A)
68K
5K
-165
-165
FED. #1159
RP-MC2 PL.20
ESCG GA-9
B+
100K
-165
EZB5 F-2
INPUT DECODER HIGH FOR VALUE PL.6,7
180K
12K
12K
+150
100UUF
ML (S1,2)
100K
D1
FED. #1159
D2
APPROX. 750Ω
.05UF
100K
MS(1)
1 MEG.
-375
+75
6AS7 OR 6520 HOLD & CLEAR DRIVER
W.E. 275B RELAY
10
+150
.1UF
680Ω
D4
1
5823
D3
D5
+150
100K
680Ω
MA(1,2)
-400
47K
680Ω
22K
47K
47K
SRC (1)
1 MEG.
100K
MS(1)A
STOR. BIT
2000 UUF
100K
470K
.022 UF
240K
.05UF
470K
PUNCH ACTUATOR
220Ω
1K
150K
S6.....S2S1
K-AAK1
-375
-150
-375
-375
ALL S1 STOR. BITS
-165
-15
SET 1 COMM. PL.28

PLATE 10 C



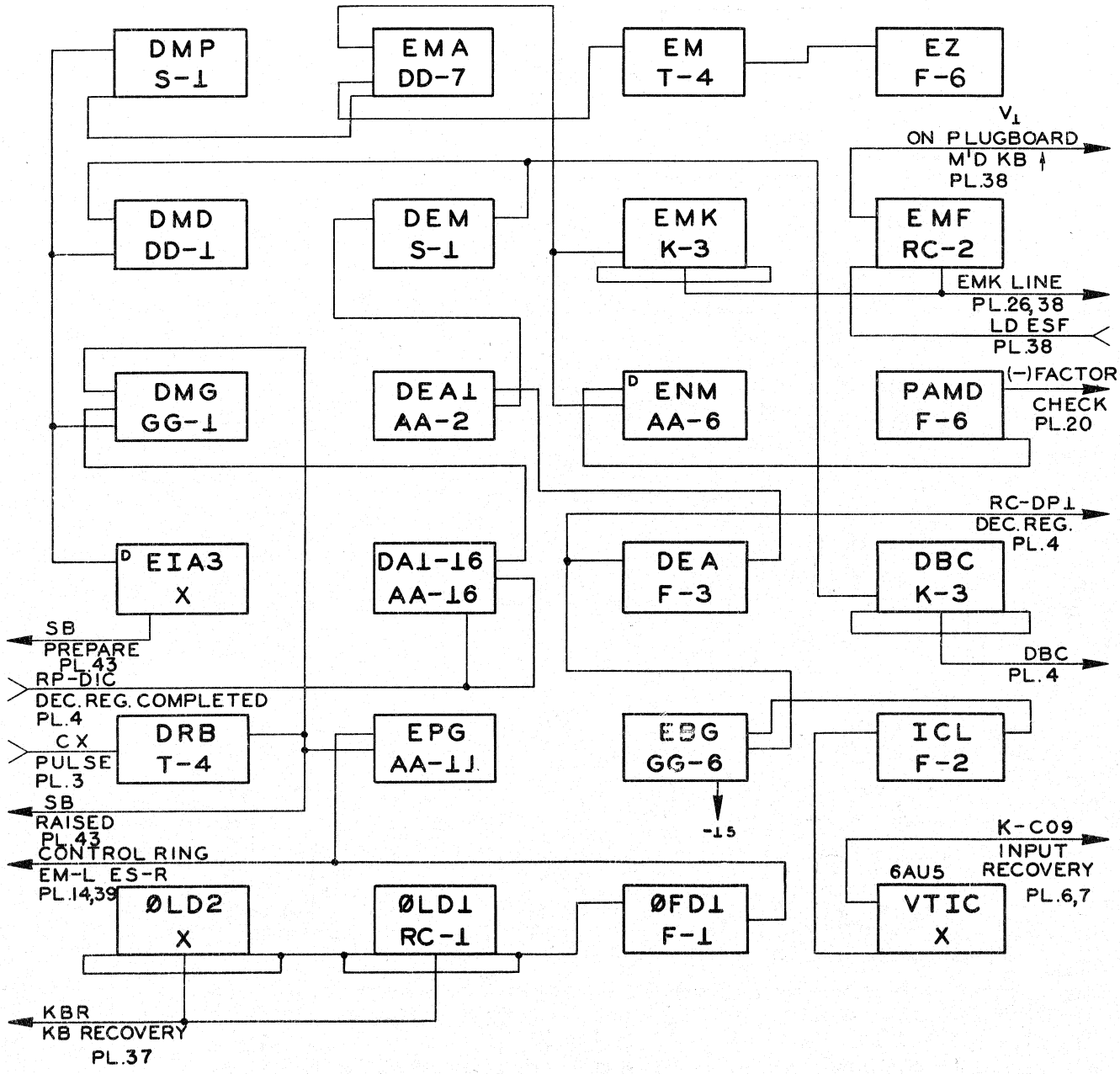
CALCULATOR ZEROIZE

PLATE 11C



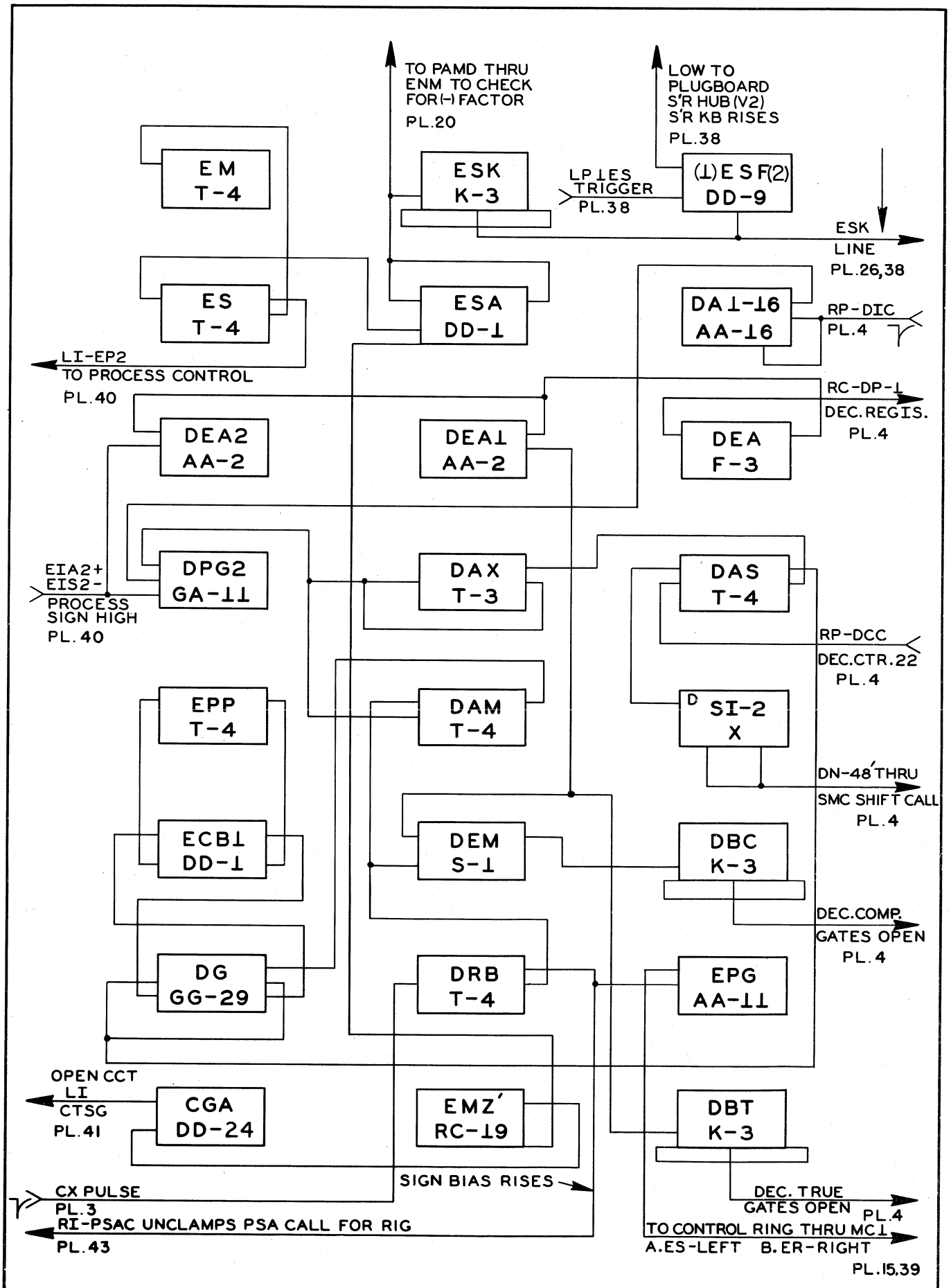
CLAMP CIRCUITS

PLATE 12 C



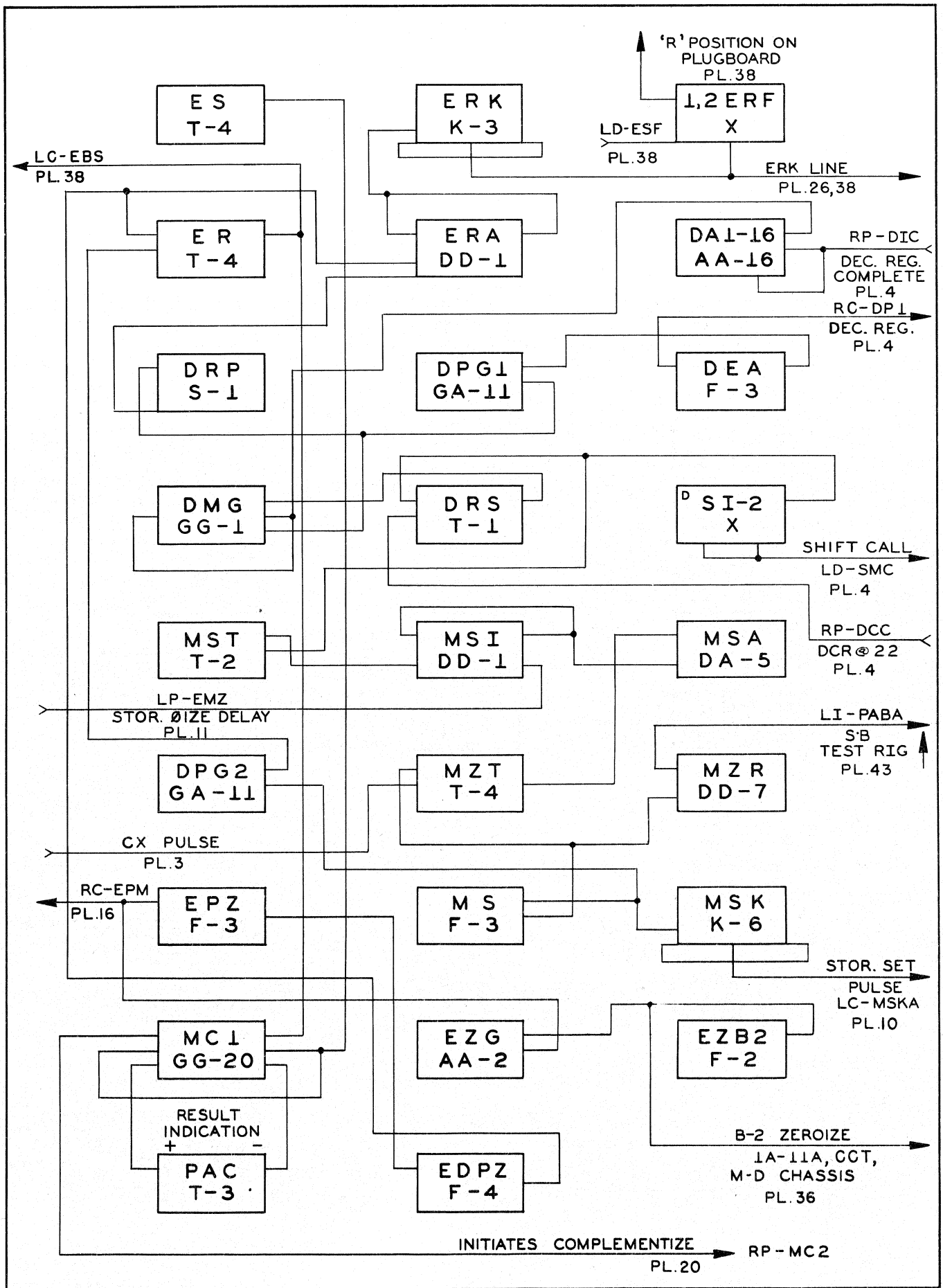
MINIDEND REGISTRATION

PLATE 13 C



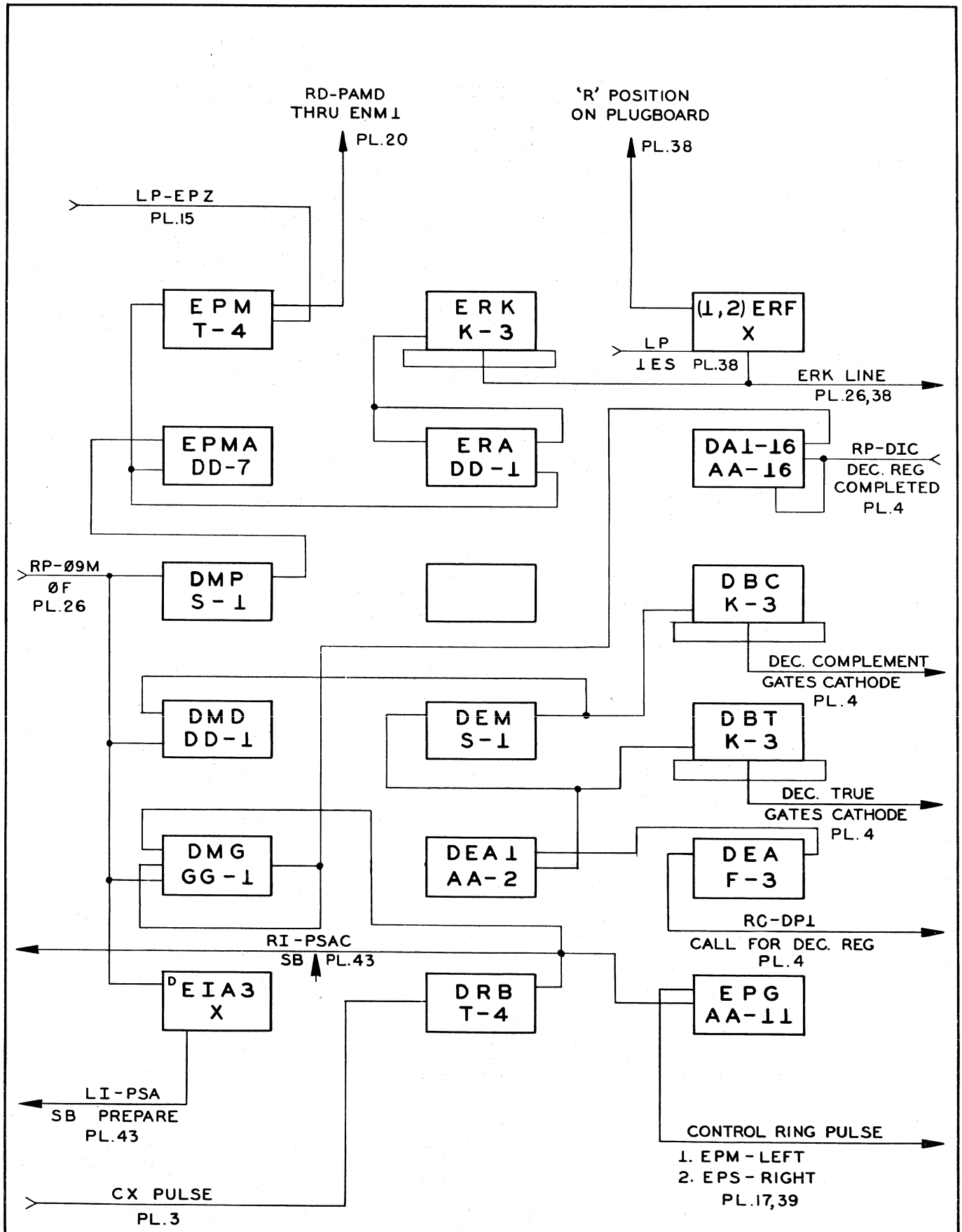
SUBVISOR REGISTRATION

PLATE 14 C



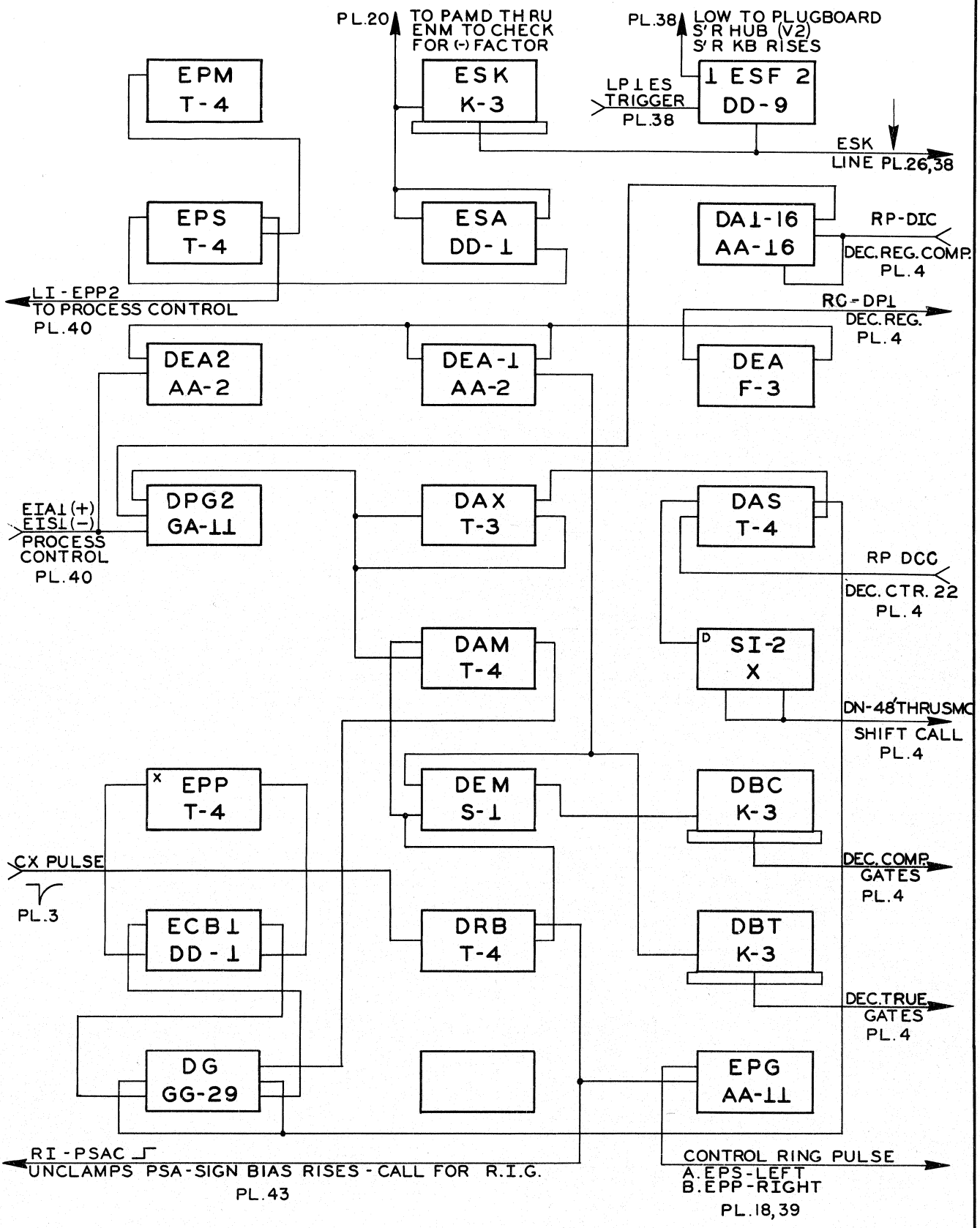
RESULT TO STORAGE

PLATE 15 C



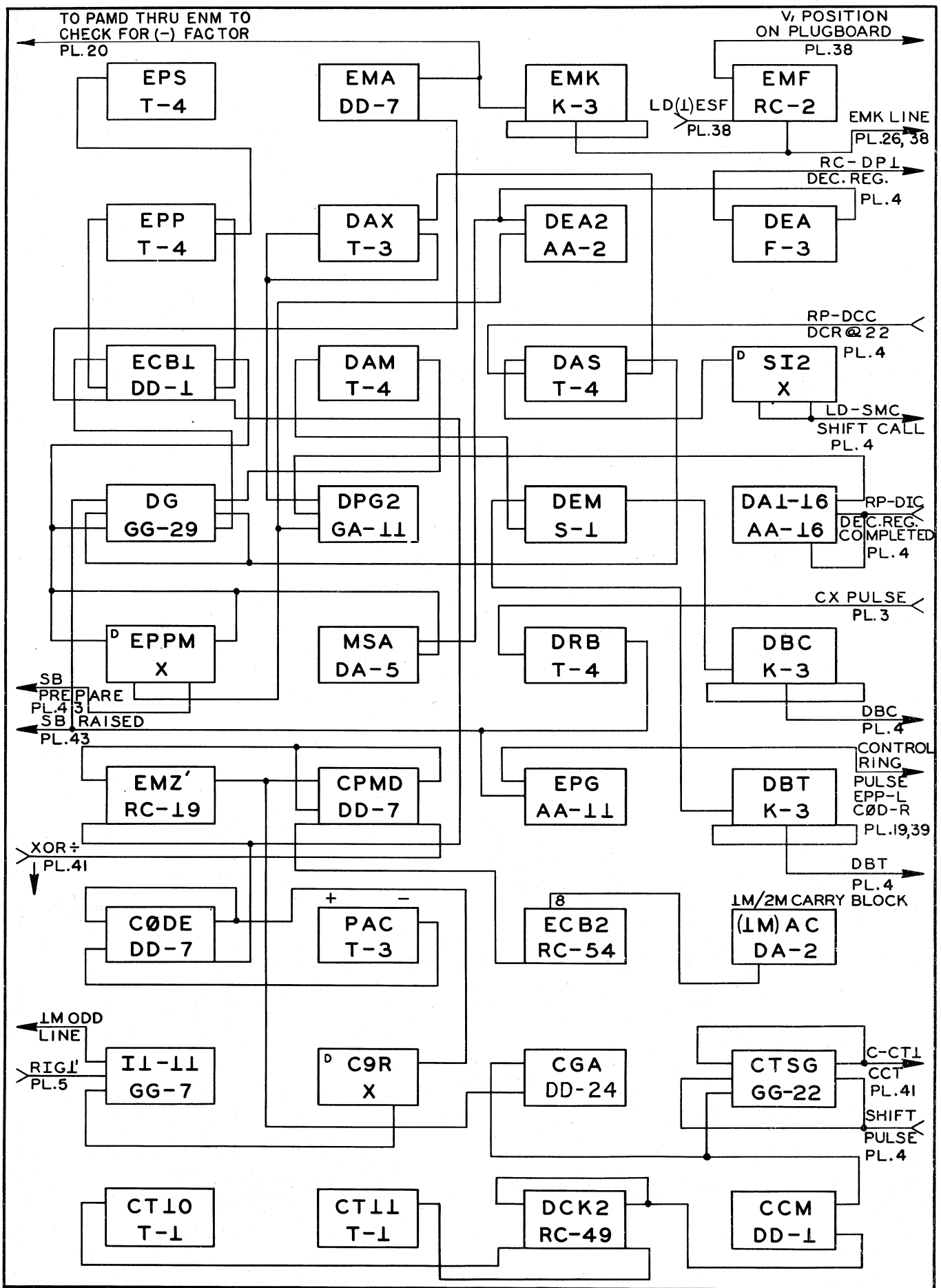
PROOF MINIDEND-STORAGE REGISTRATION

PLATE 16 C



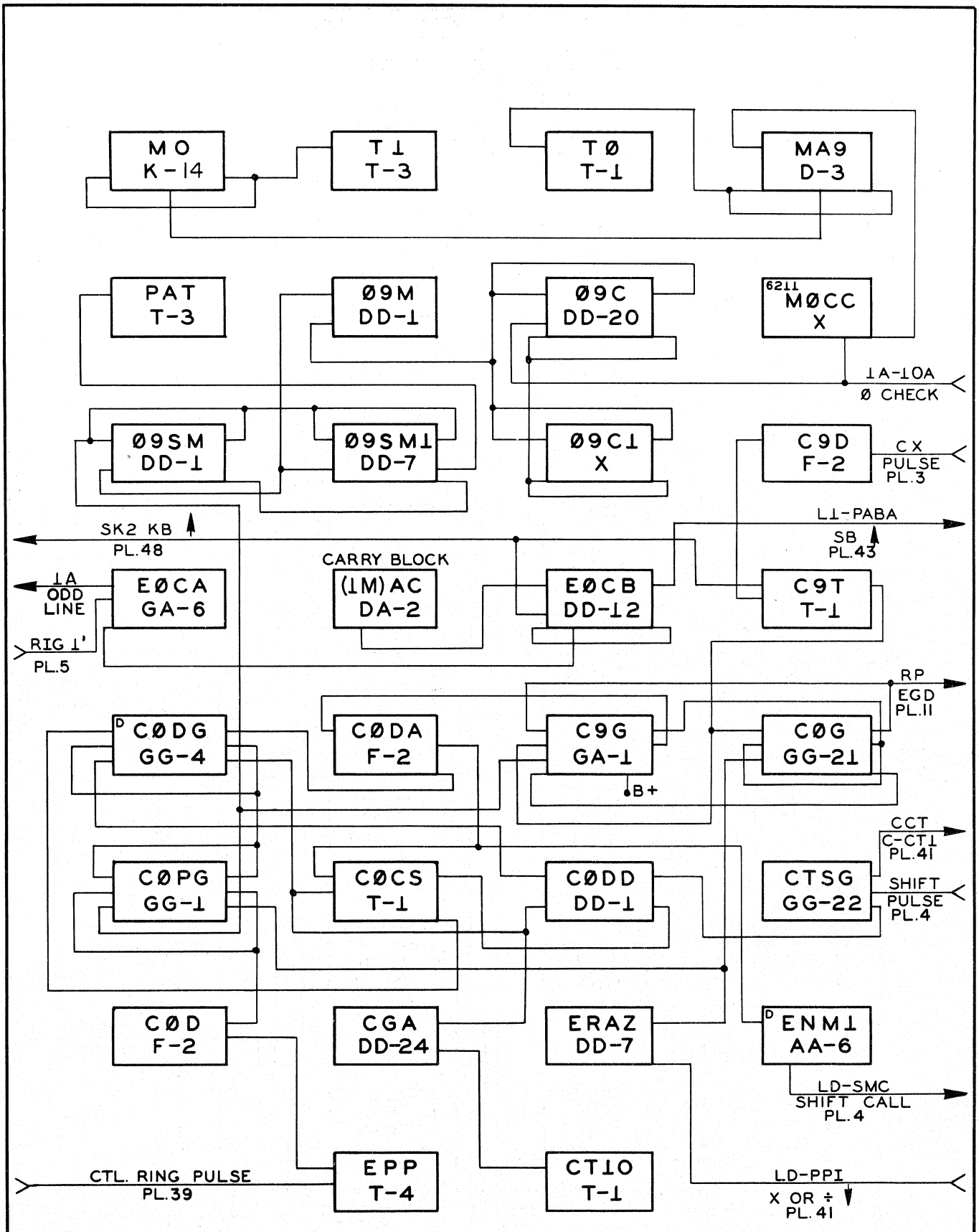
PROOF SUBVISOR-SUBVISOR REGISTRATION

PLATE 17 C



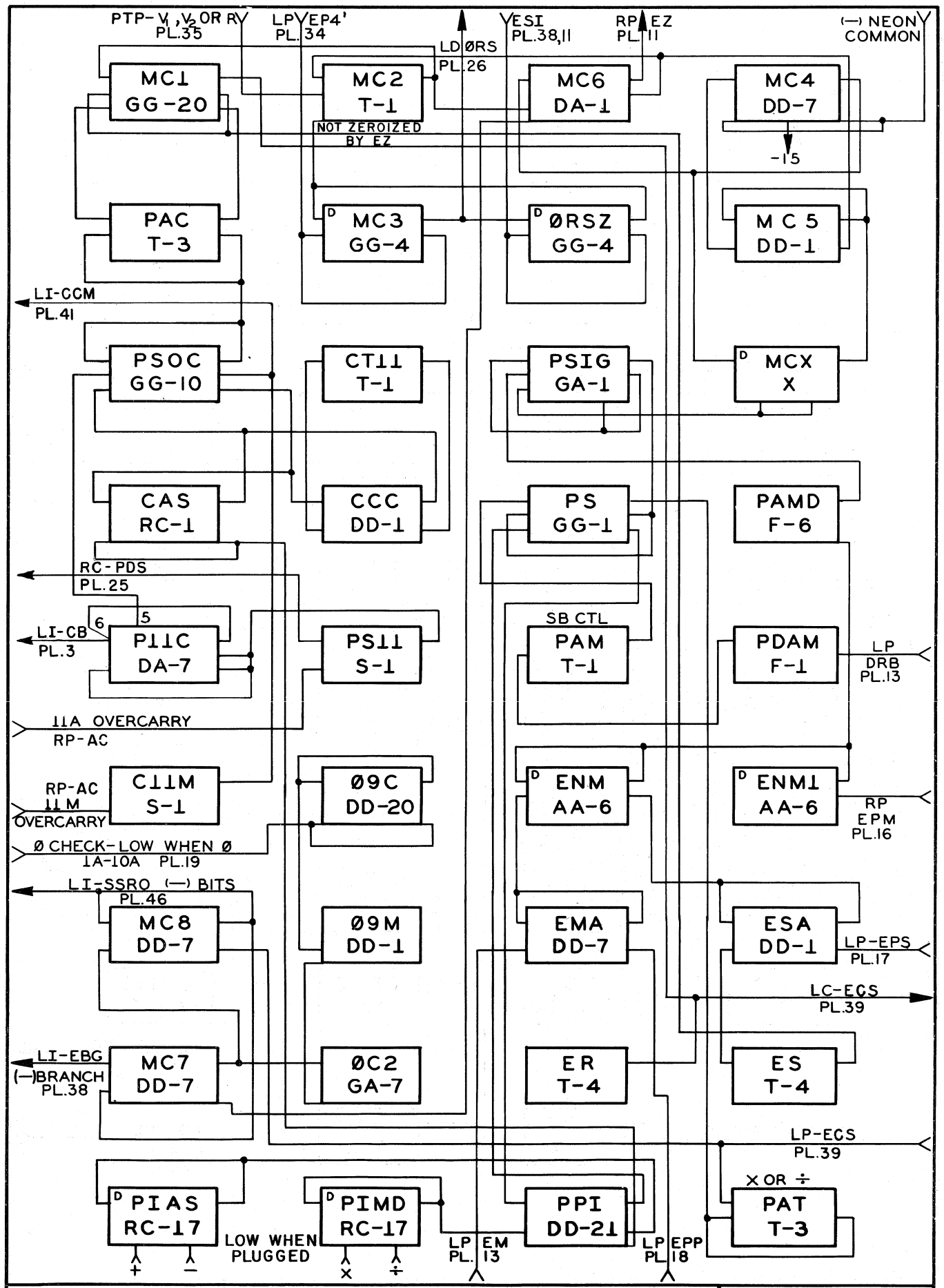
MINIDEND SUBTRACTION

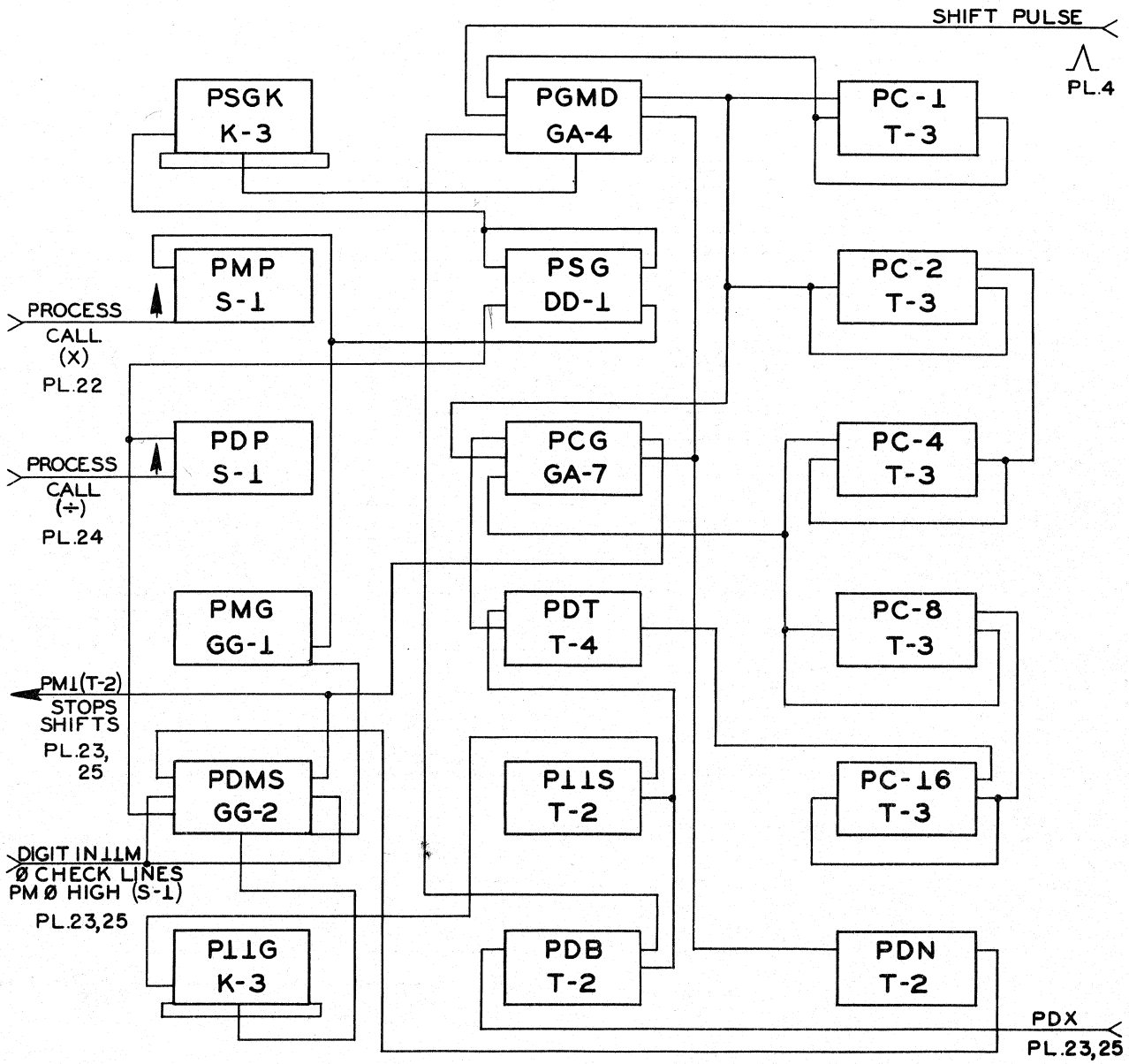
PLATE 18 C



ZERO CHECK

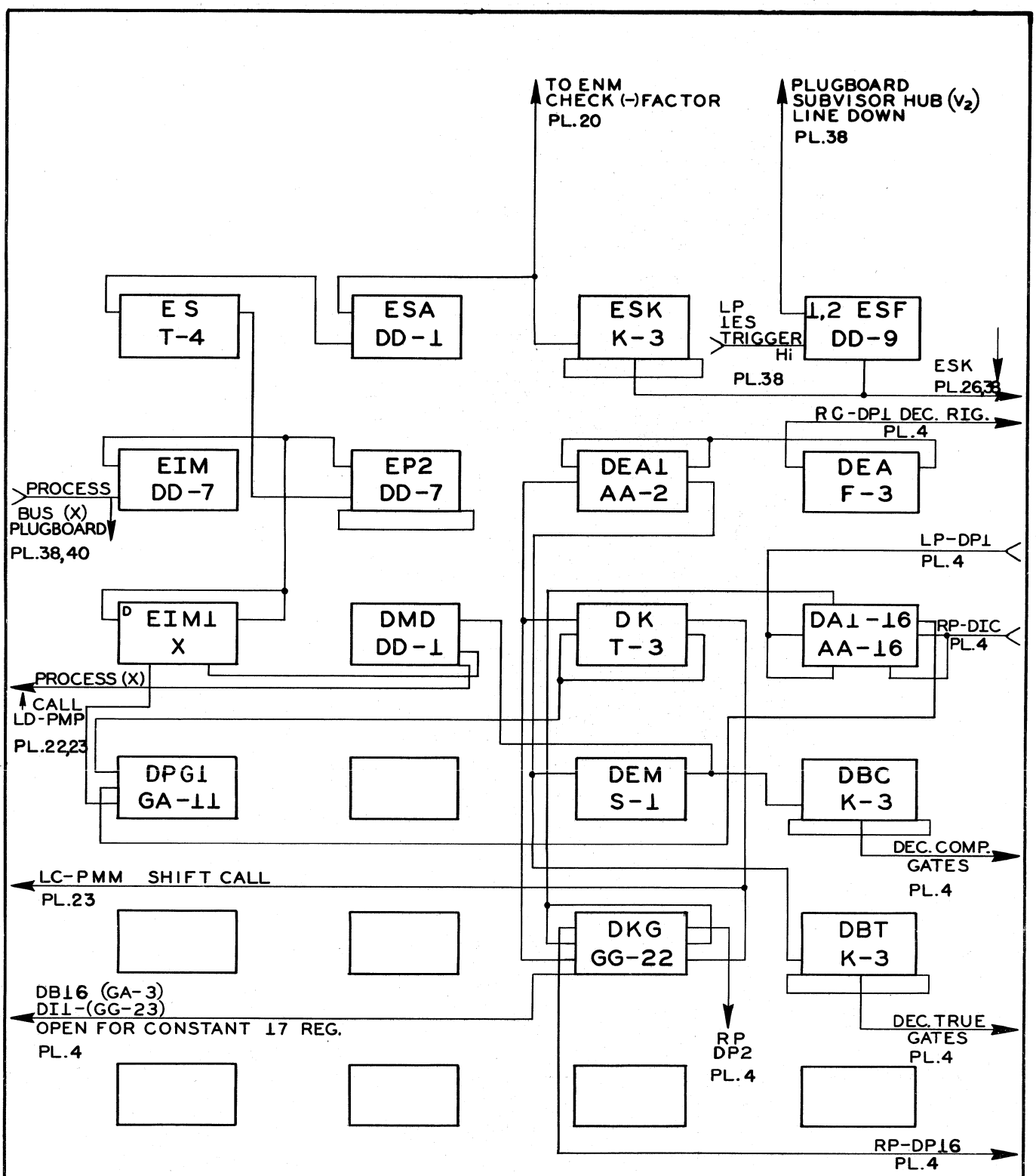
PLATE 19 C


PTP-V1,V2 OR RV
PL.35
LP EP4'
PL.34
LD ØRS
PL.26
ESI
PL.38,11
RP EZ
PL.11
(—) NEON COMMON
MC1 GG-20
MC2 T-1
NOT ZEROIZED BY EZ
MC6 DA-1
MC4 DD-7
-15
PAC T-3
D MC3 GG-4
D ØRSZ GG-4
MC5 DD-1
LI-CCM PL.41
PSOC GG-10
CT11 T-1
PSIG GA-1
D MCX X
CAS RC-1
CCC DD-1
PS GG-1
PAMD F-6
RC-PDS PL.25
6
5
LI-CB PL.3
P11C DA-7
PS11 S-1
SB CTL
PAM T-1
PDAM F-1
LP DRB PL.13
11A OVERCARRY
RP-AC
RP-AC 11M OVERCARRY
C11M S-1
Ø9C DD-20
D ENM AA-6
D ENM1 AA-6
RP EPM PL.16
Ø CHECK-LOW WHEN Ø 1A-10A PL.19
LI-SSRO (—) BITS PL.46
MC8 DD-7
Ø9M DD-1
EMA DD-7
ESA DD-1
LP-EPS PL.17
LC-ECS PL.39
LI-EBG (—)BRANCH PL.38
MC7 DD-7
ØC2 GA-7
ER T-4
ES T-4
LP-ECS PL.39
D PIAS RC-17
D PIMD RC-17
PPI DD-21
X OR ÷
PAT T-3
LOW WHEN PLUGGED
+
—
×
÷
LP EM PL.13
LP EPP PL.18
COMPLEMENTIZE
PLATE 20 C



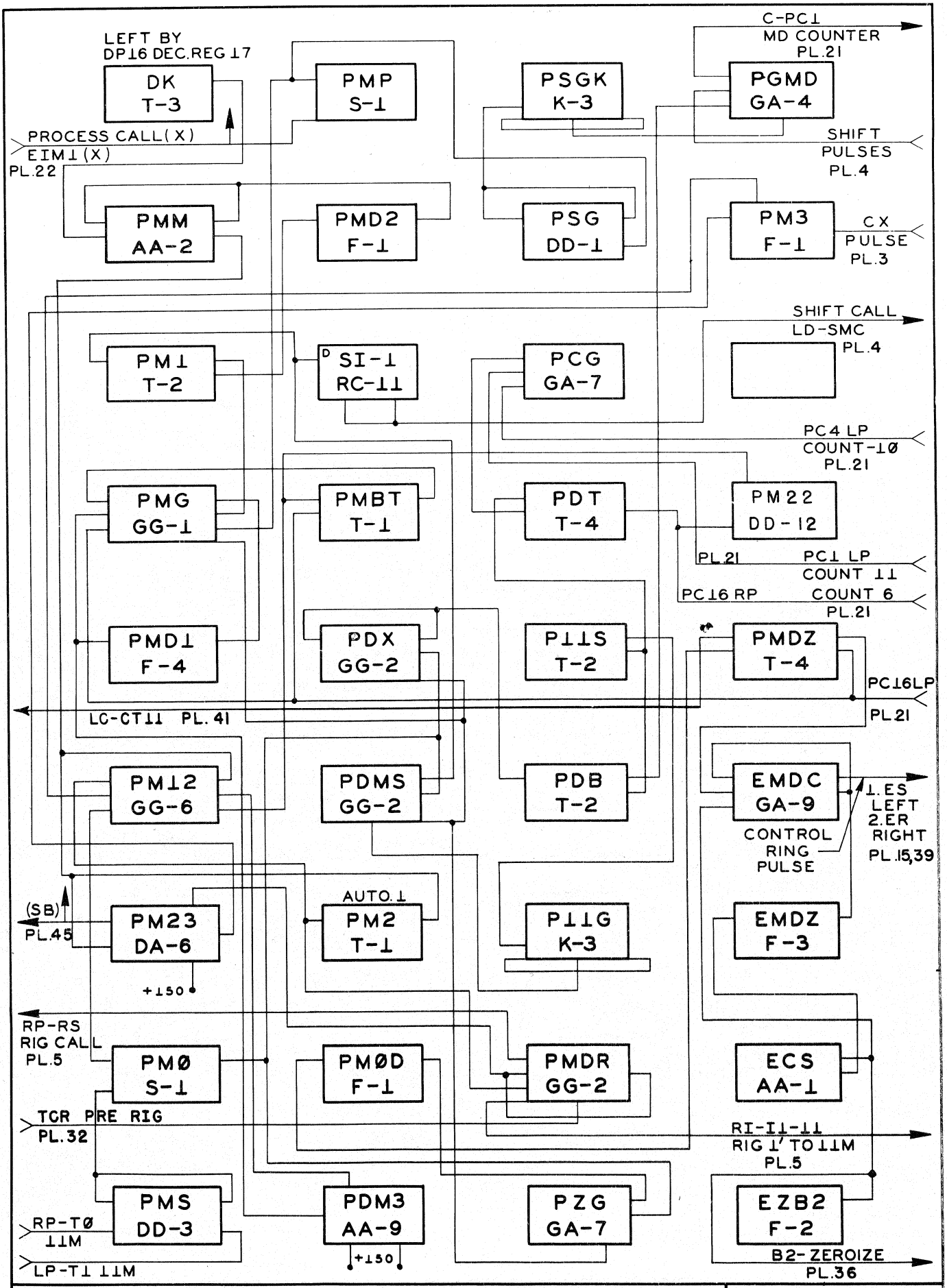
MULTIPLICATION DIVISION COUNTER

PLATE 21 C



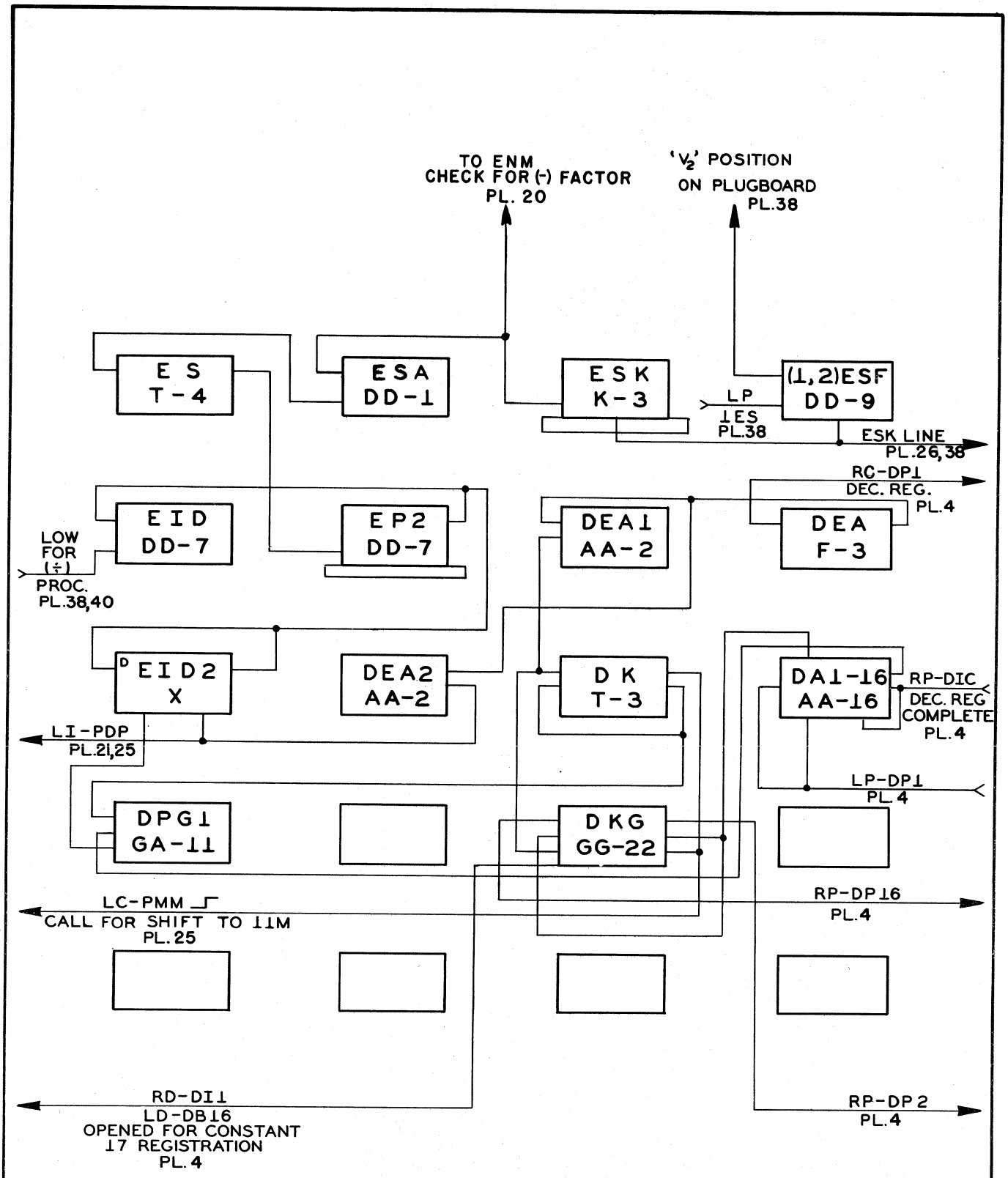
MULTIPLICATION PROCESS CALL

PLATE 22C



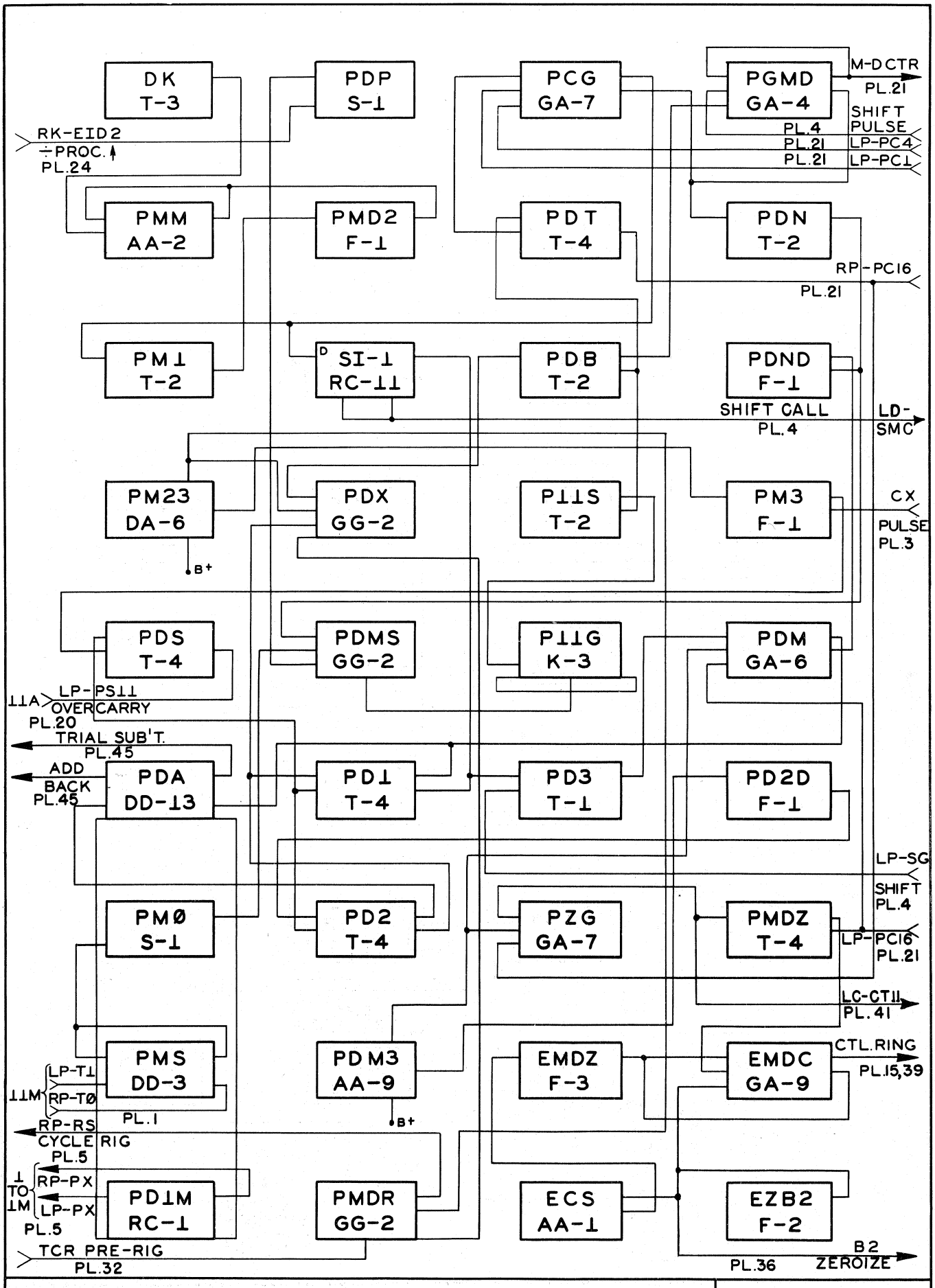
MULTIPLICATION PROCESS

PLATE 23 C



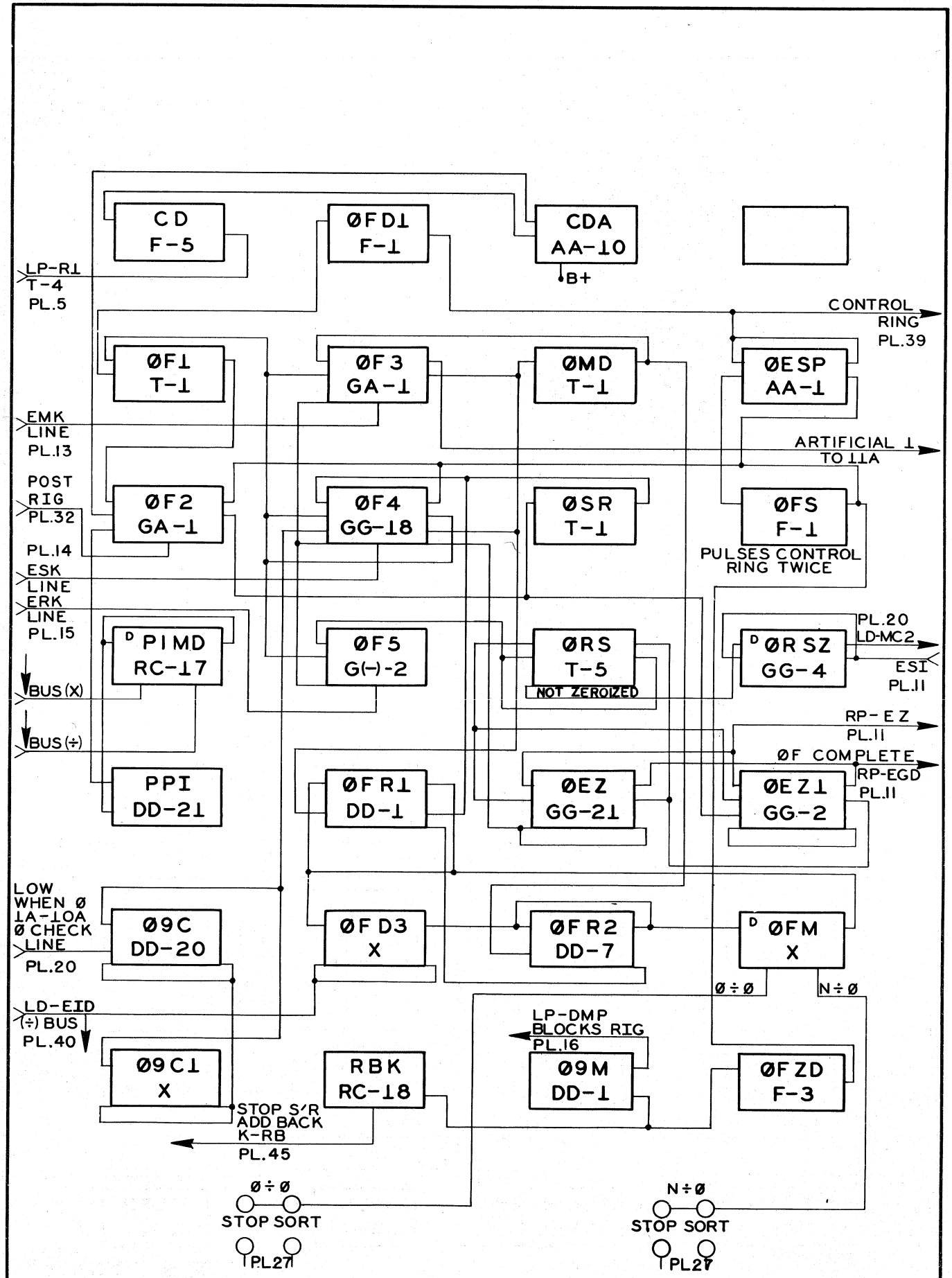
DIVISION PROCESS CALL

PLATE 24 C



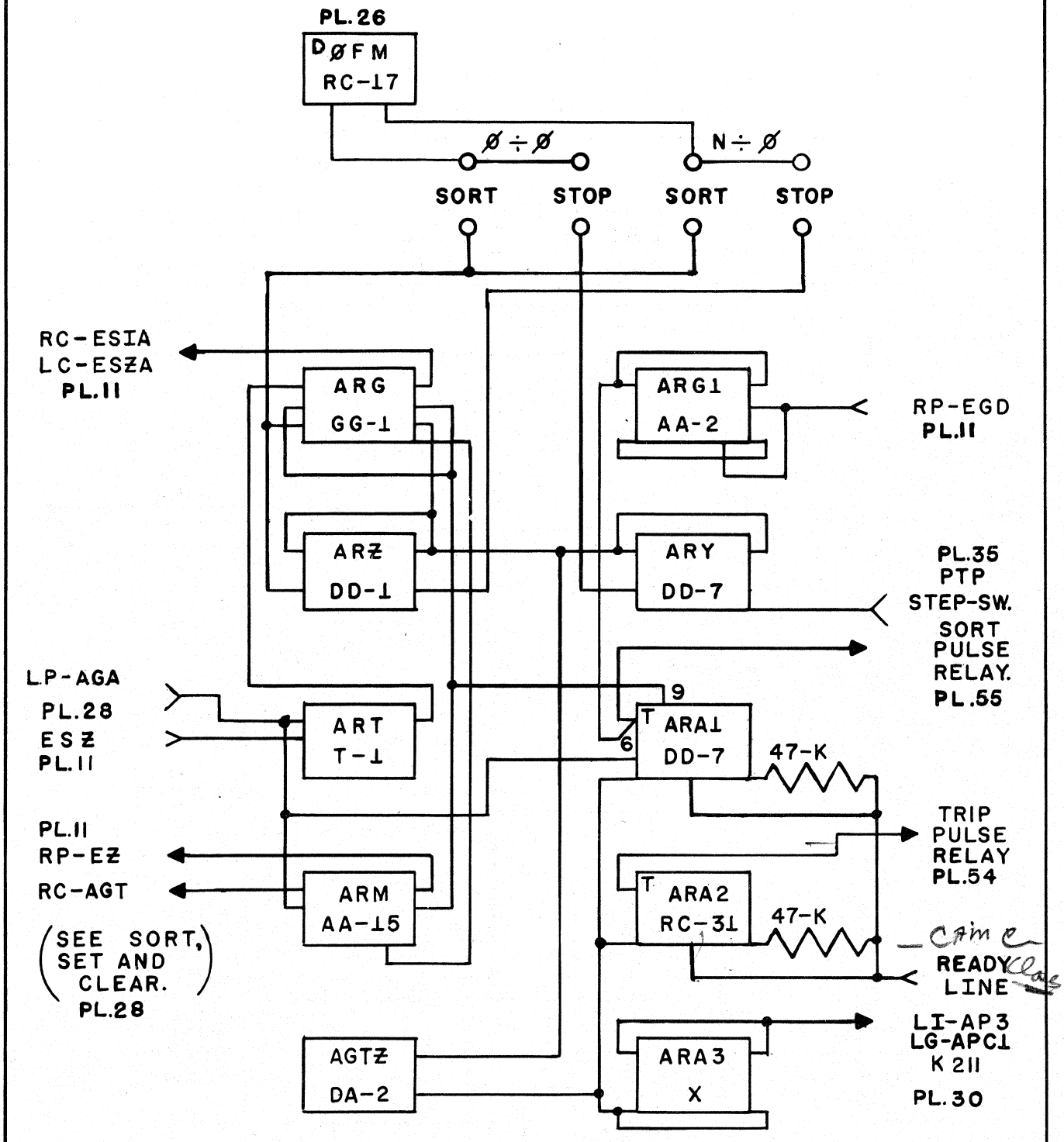
DIVISION PROCESS

PLATE 25 C

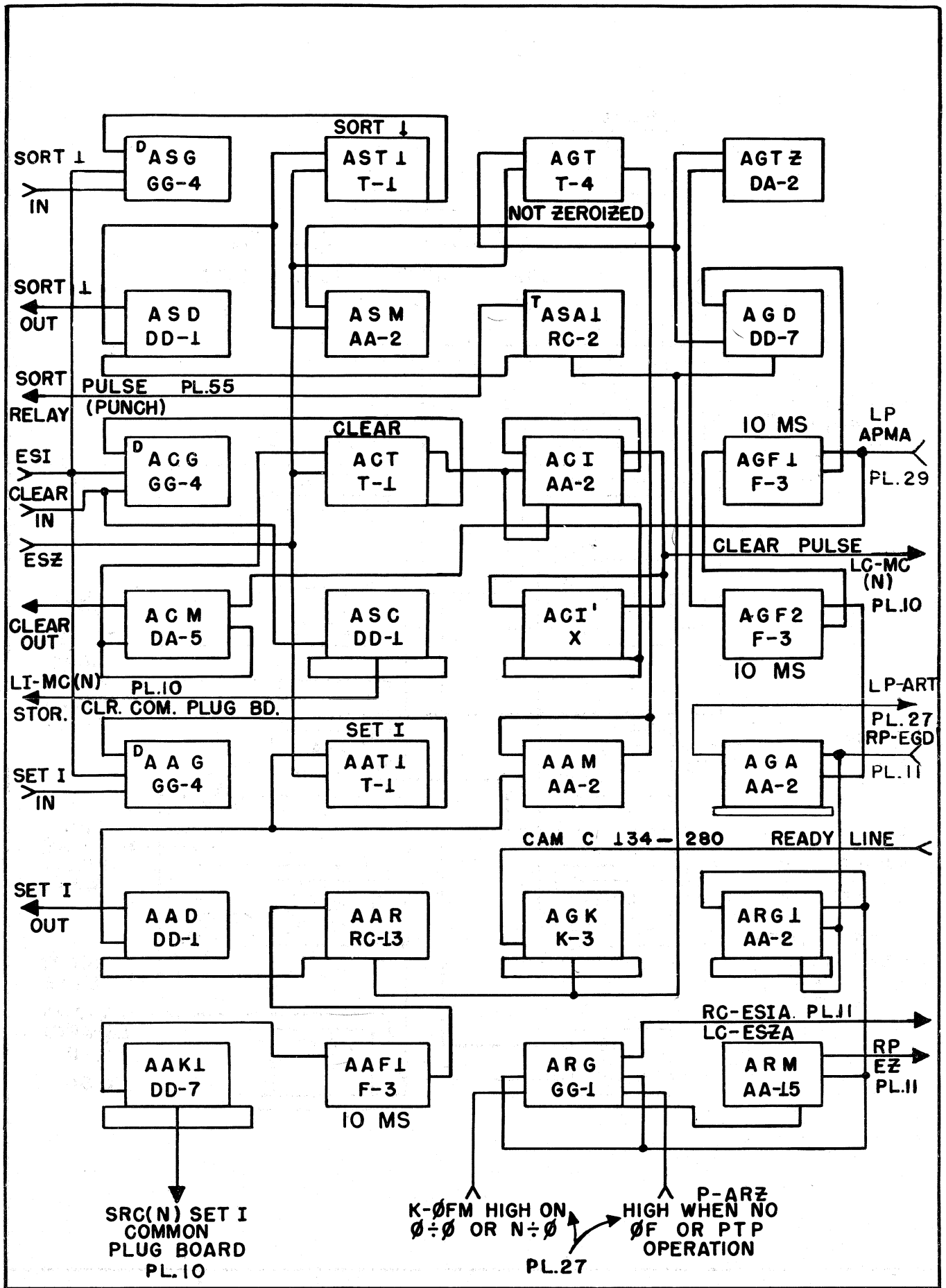


ØF MULTIPLICATION – DIVISION

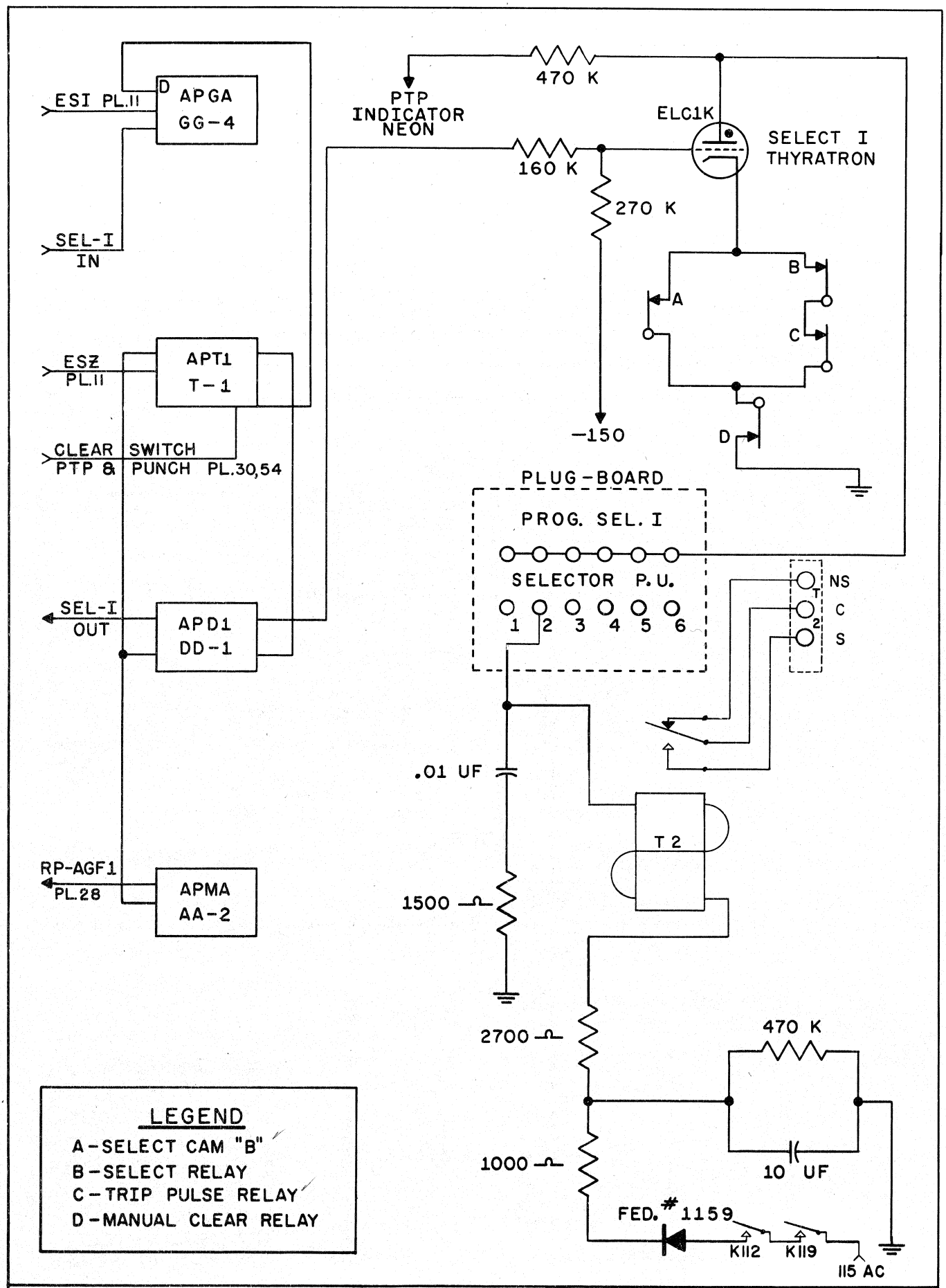
PLATE 26 C



ZERO FACTOR — SORT AND TRIP | PLATE 27C

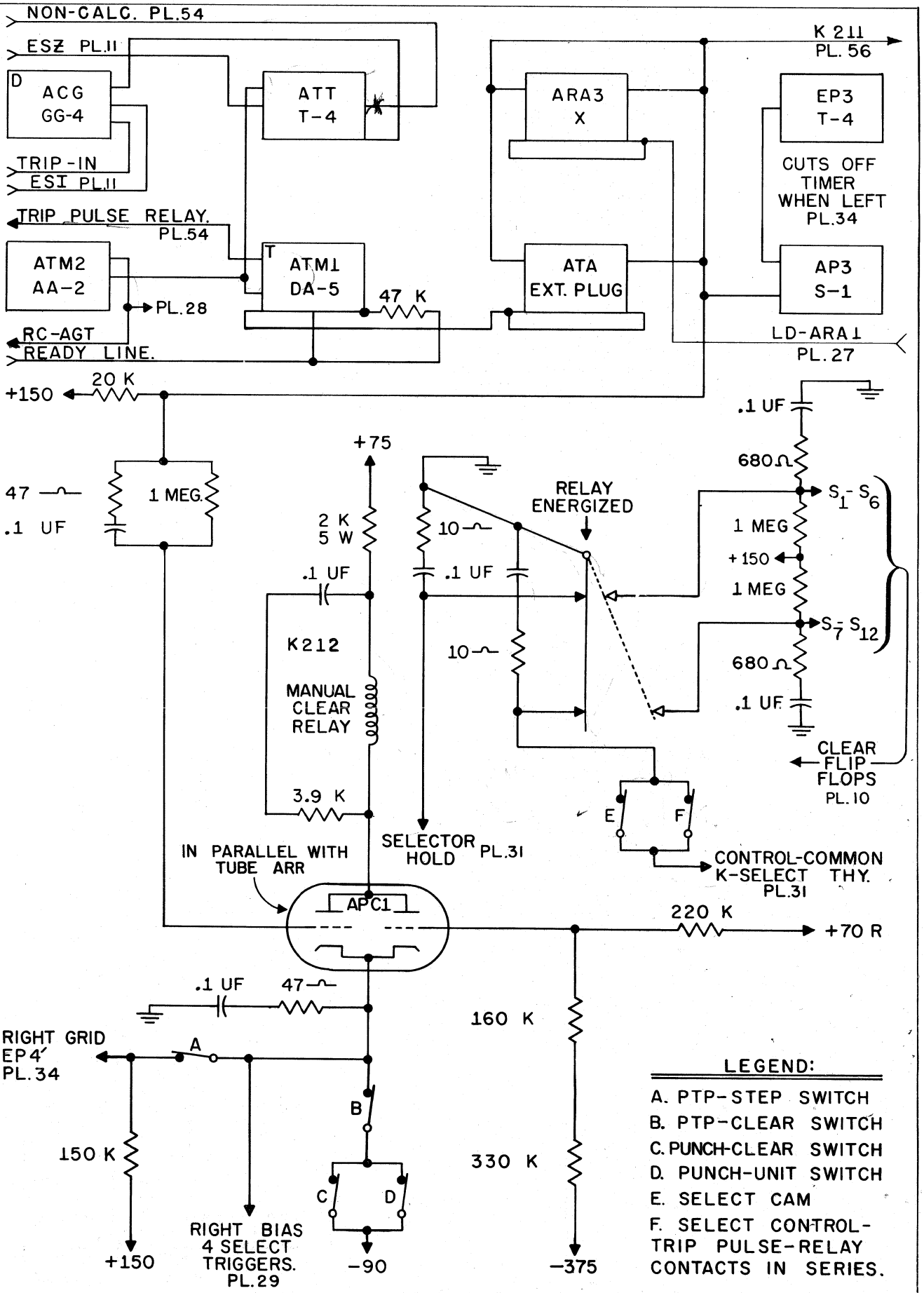


SORT I, SET I & CLEAR | PLATE 28C



SELECT 1 STEP

PLATE 29 C

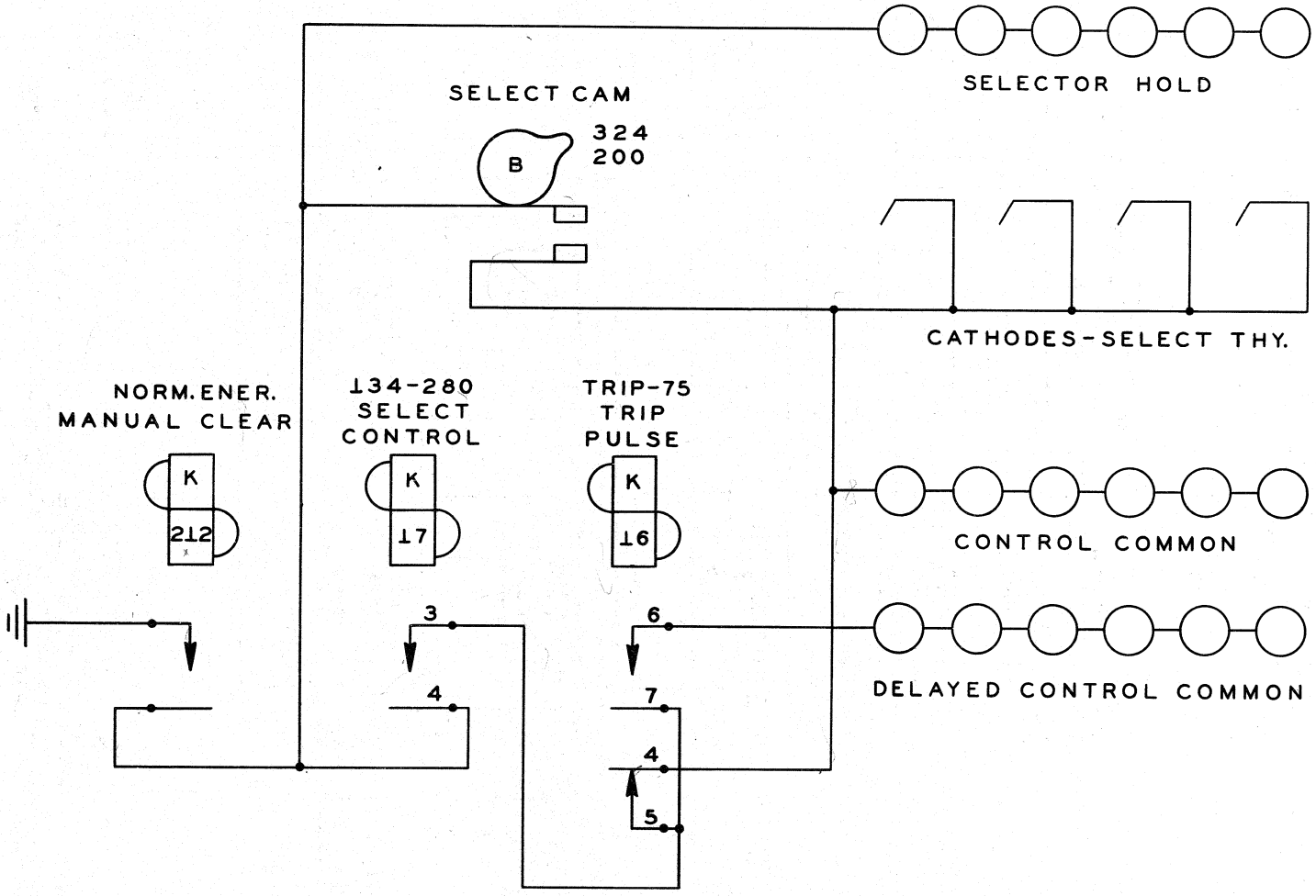


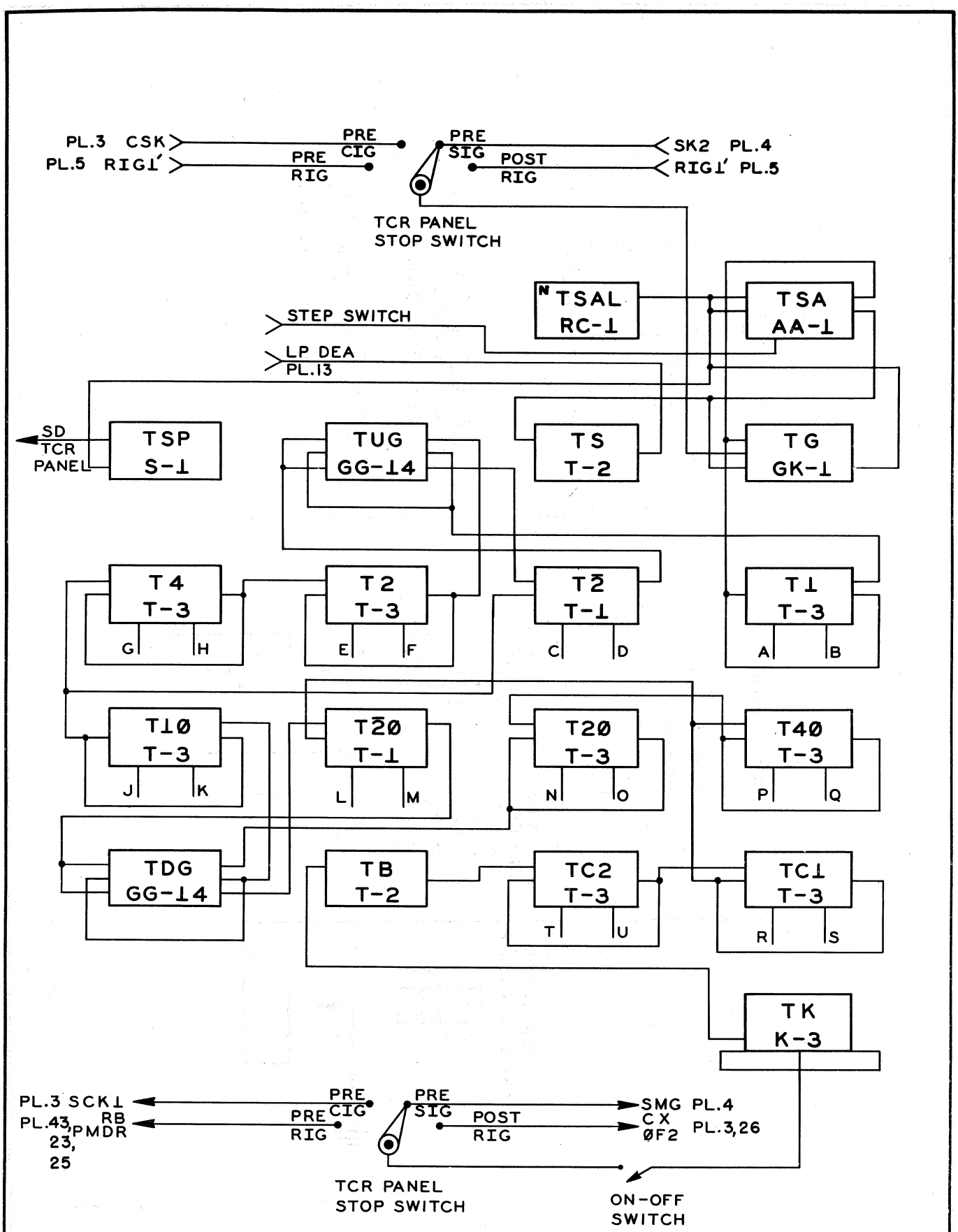
TRIP CIRCUIT

PLATE 30 C

SELECTOR RELAY CONTROL

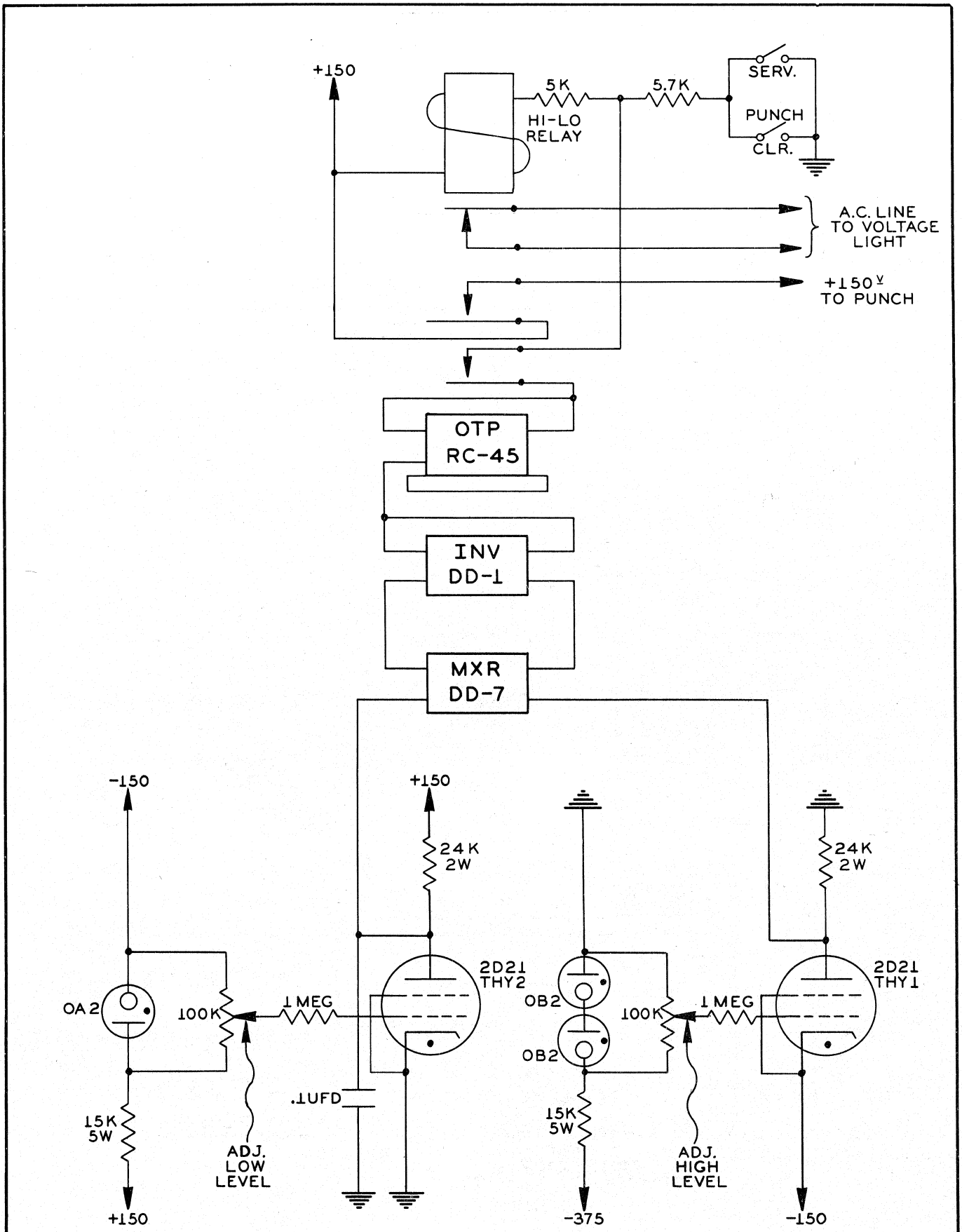
PLATE 31C





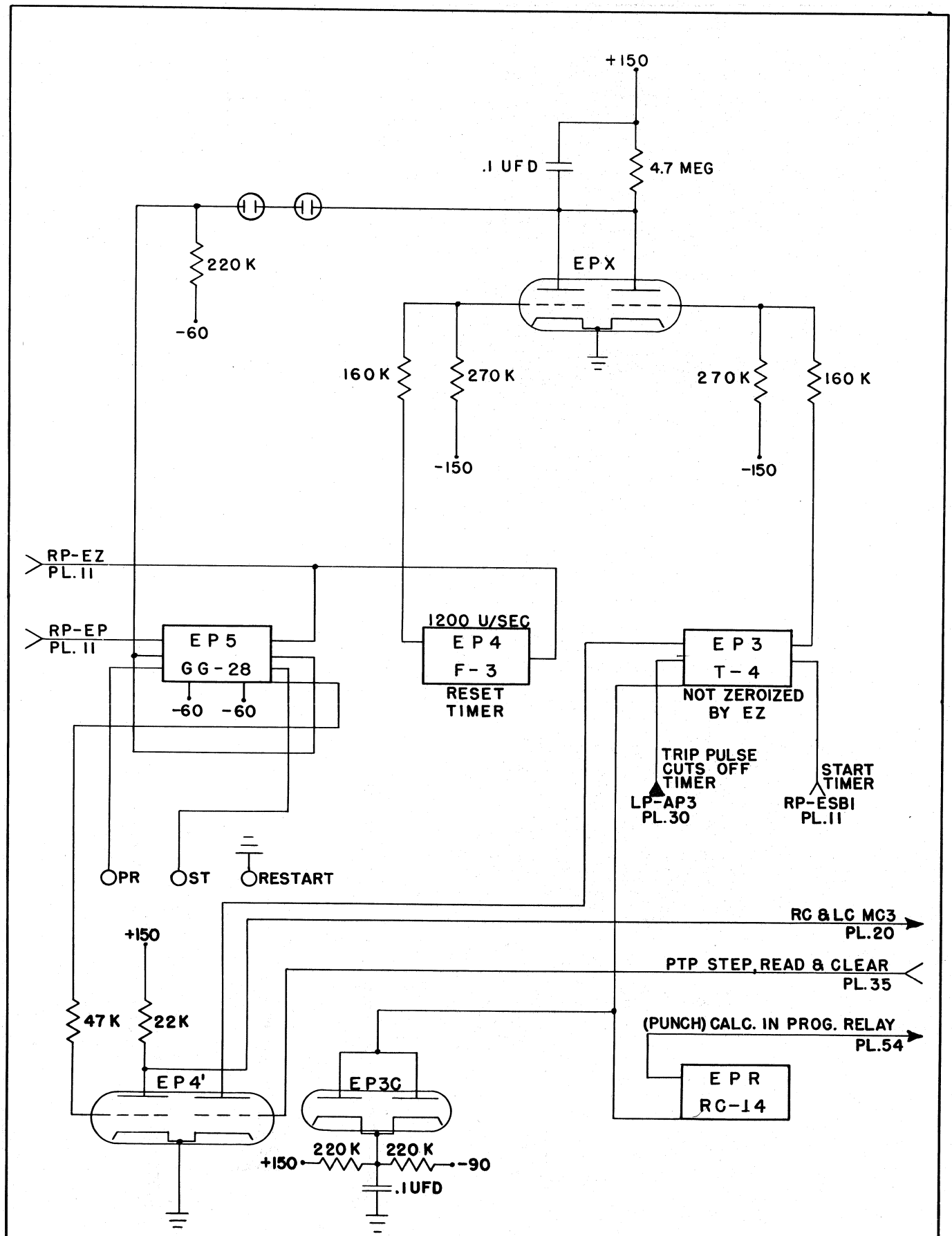
TEST COUNTER

PLATE 32 C

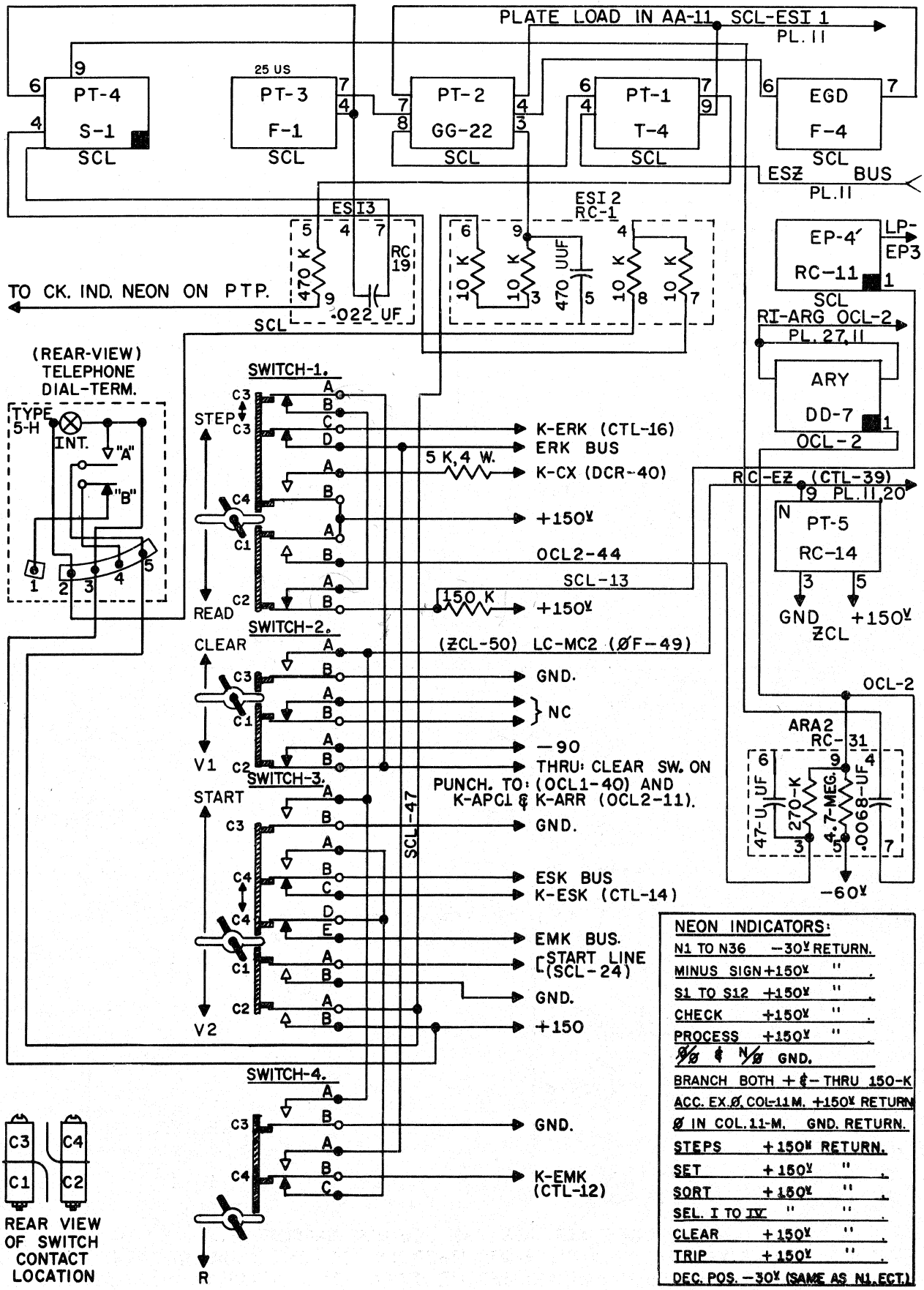


VOLTAGE ABNORMALITY DETECTOR

PLATE 33 C

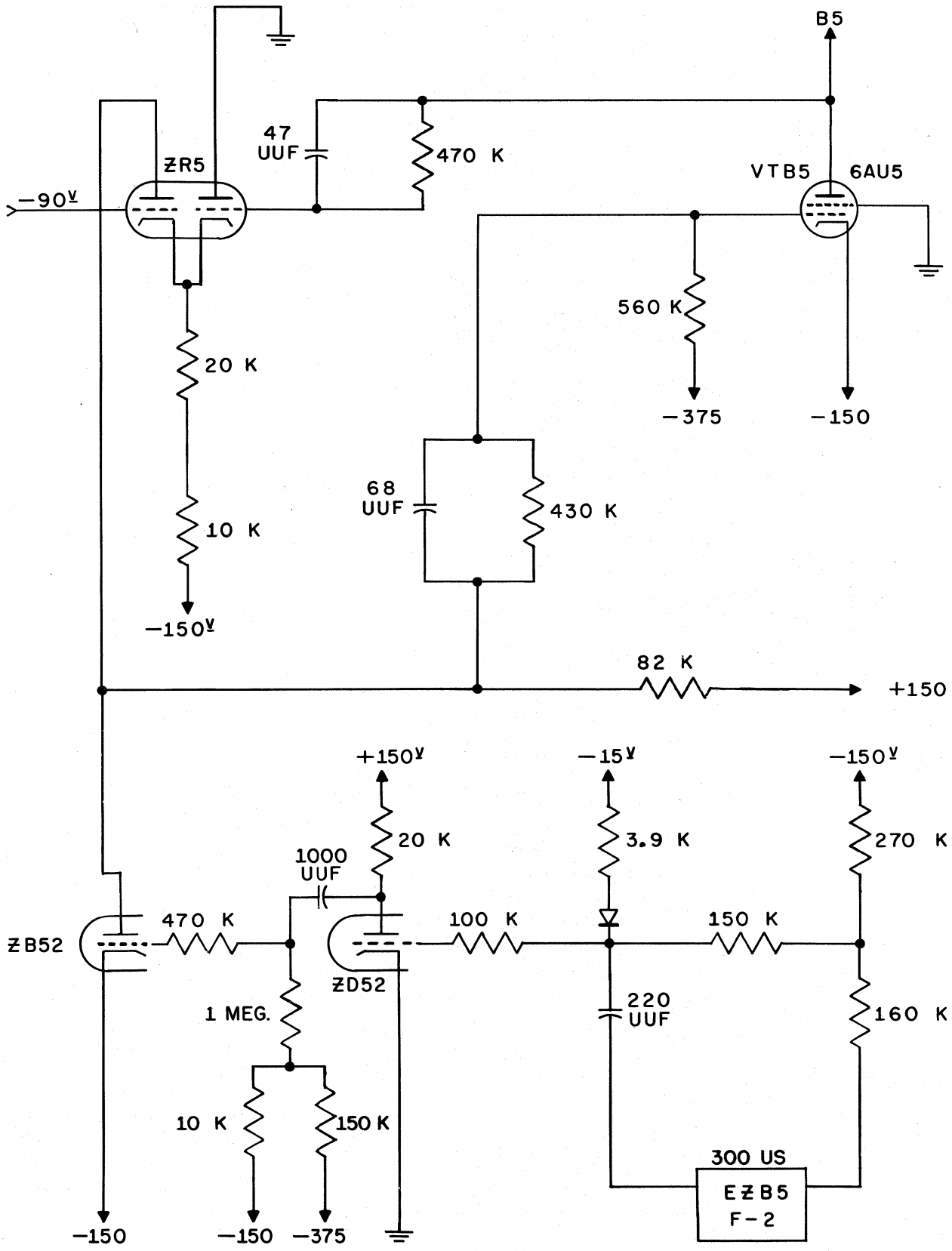


AUTOMATIC CIRCUIT TIMER 300 M/SEC. | PLATE 34 C



PROGRAM TEST PANEL OPERATION

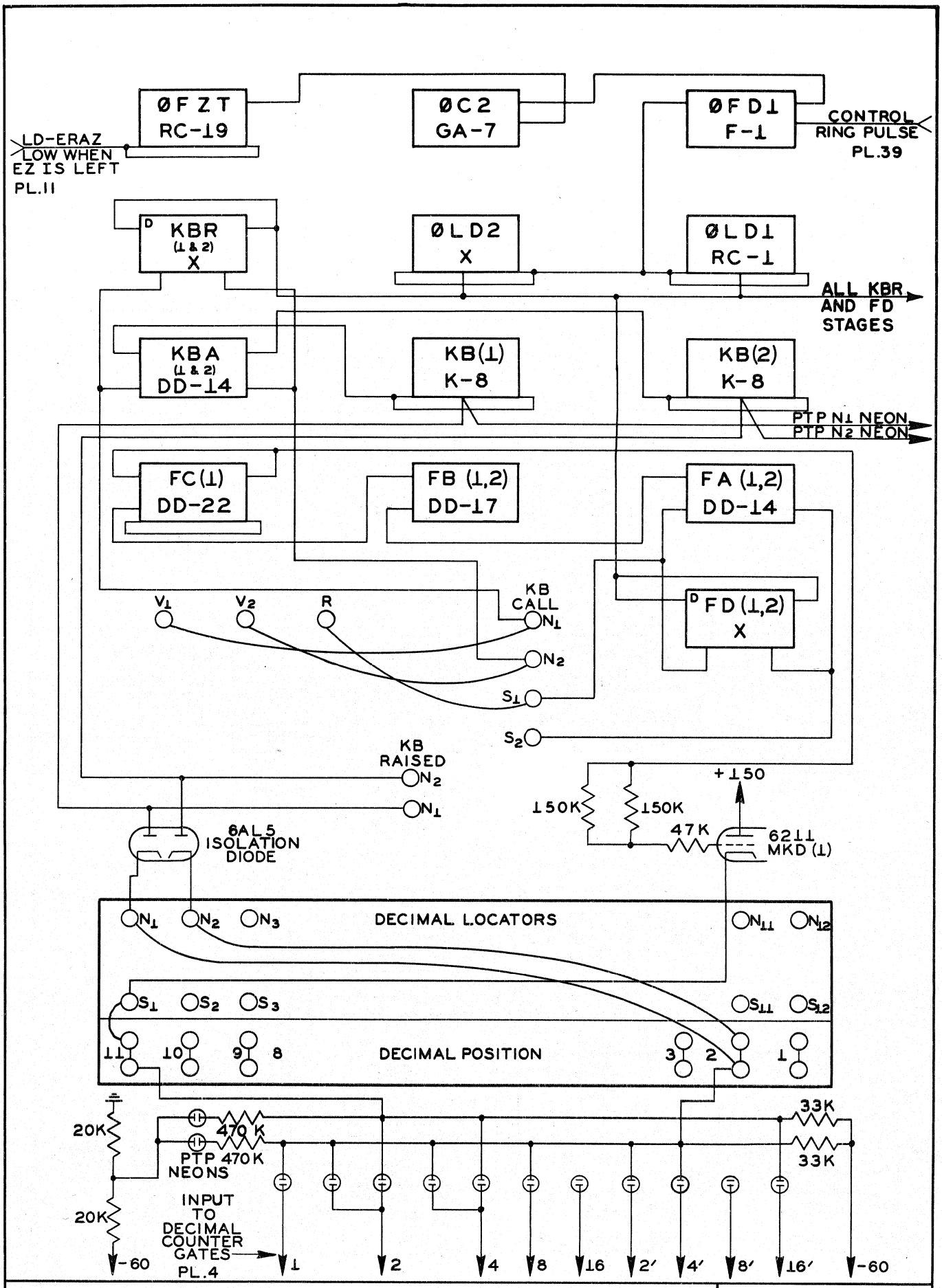
PLATE 35 C



B-2 DOES NOT USE THE 220 UUF CAPACITOR.
B-5 START IS DELAYED APPROXIMATELY 60-US TO ALLOW THE MC4L CLAMP TO BECOME EFFECTIVE ON MC1.

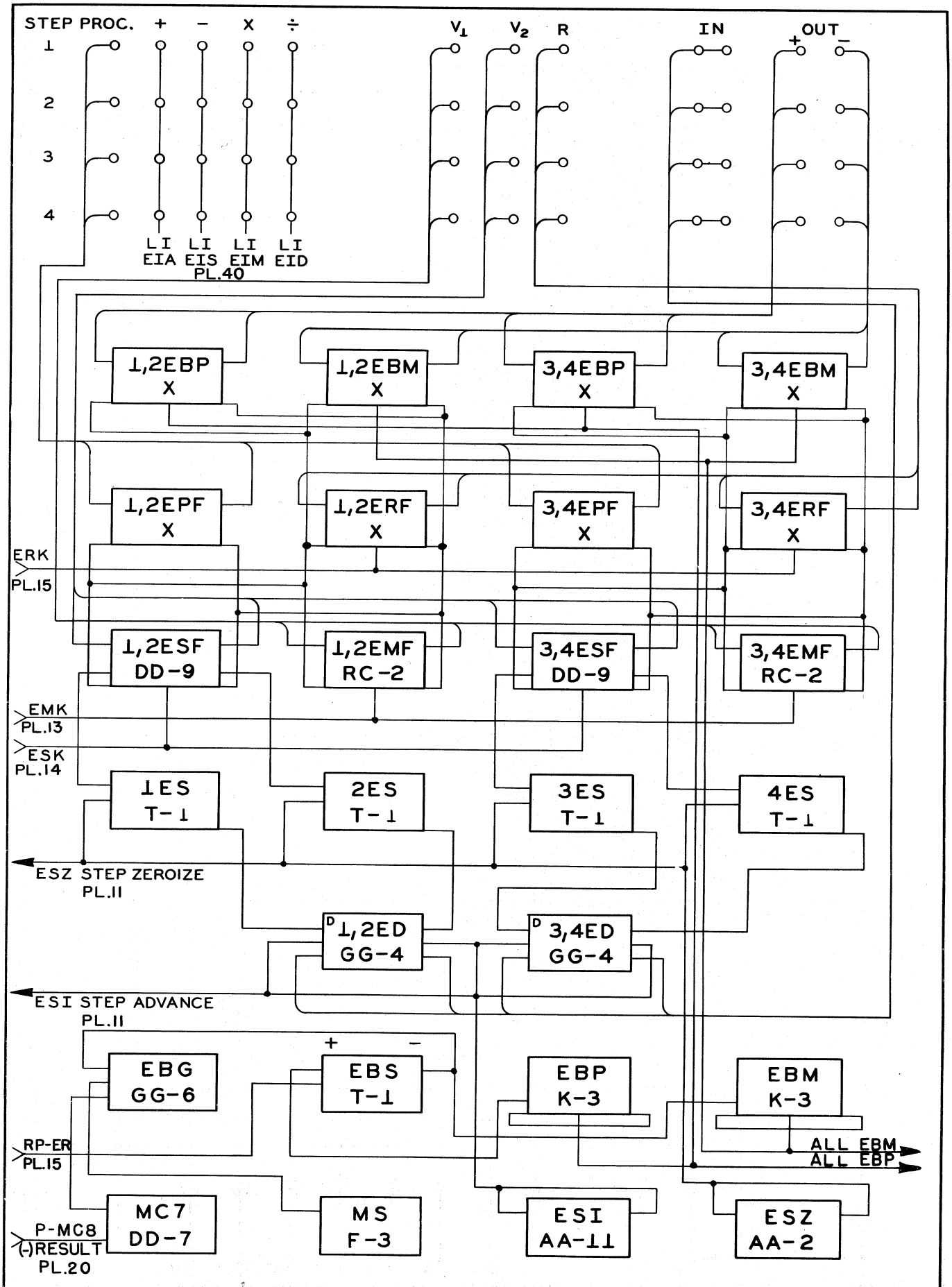
B2-B5 ZEROIZE

PLATE 36 C



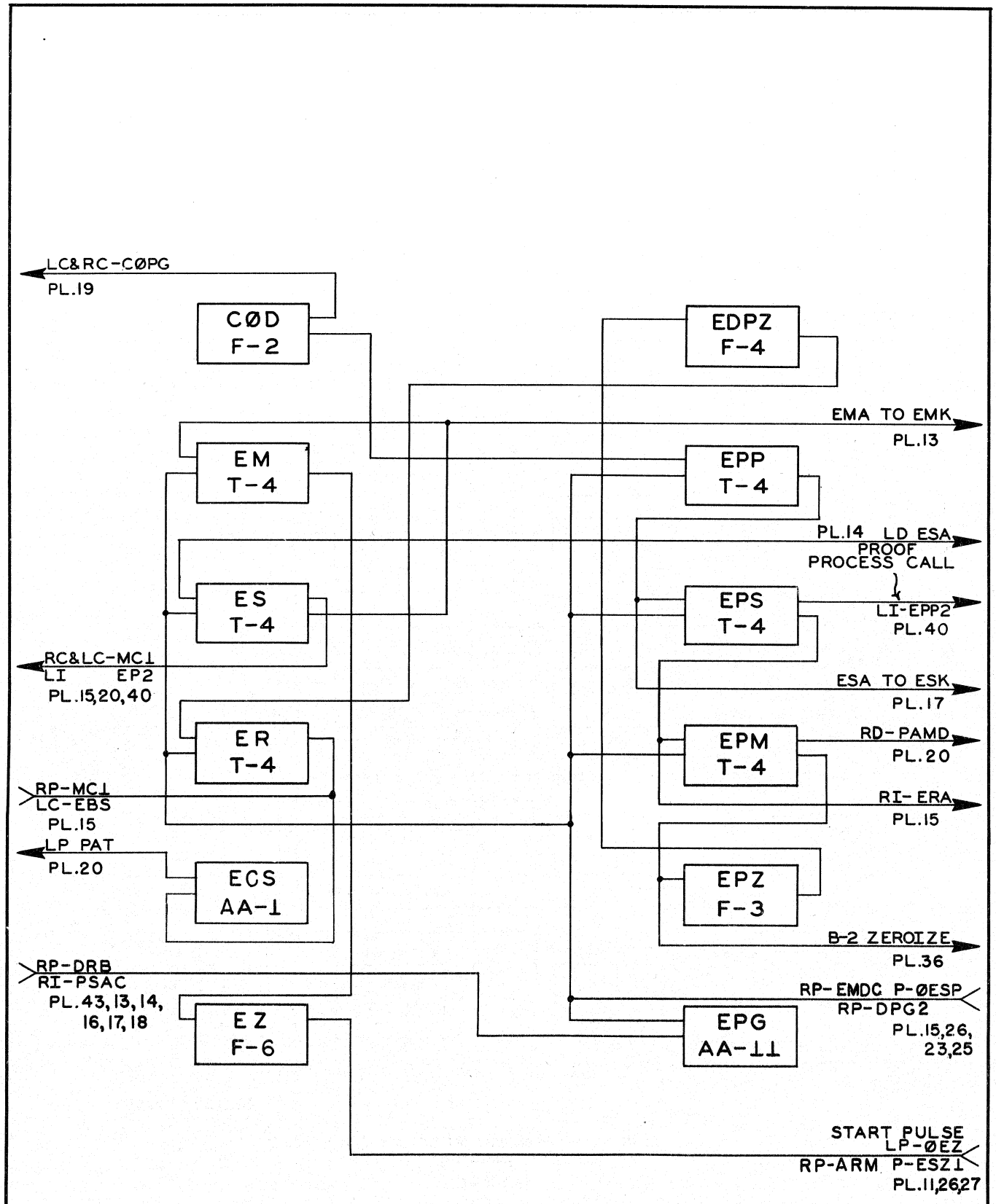
KB RECOVERY & DECIMAL CONTROL

PLATE 37 C



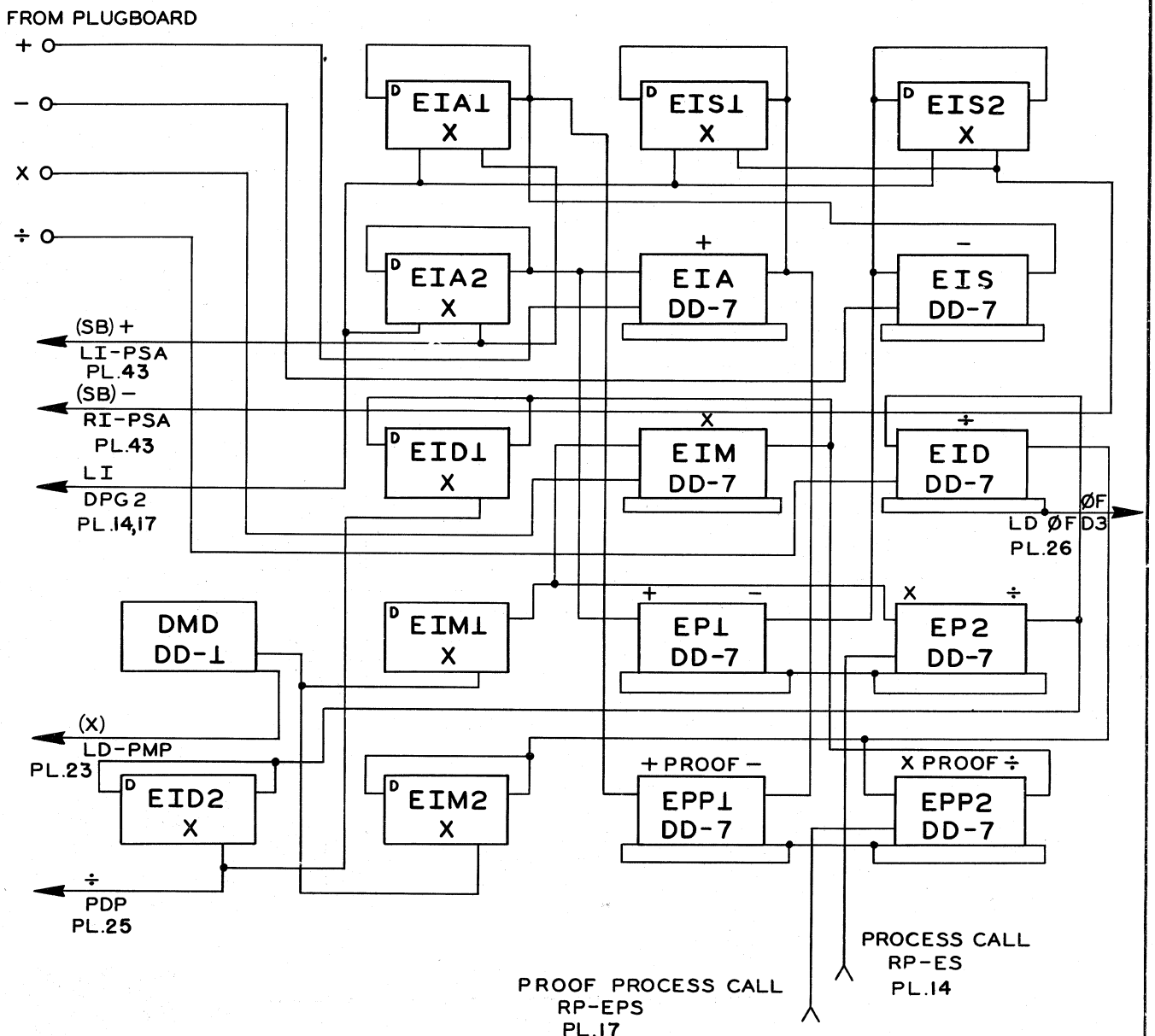
PLUGBOARD CONTROL

PLATE 38 C



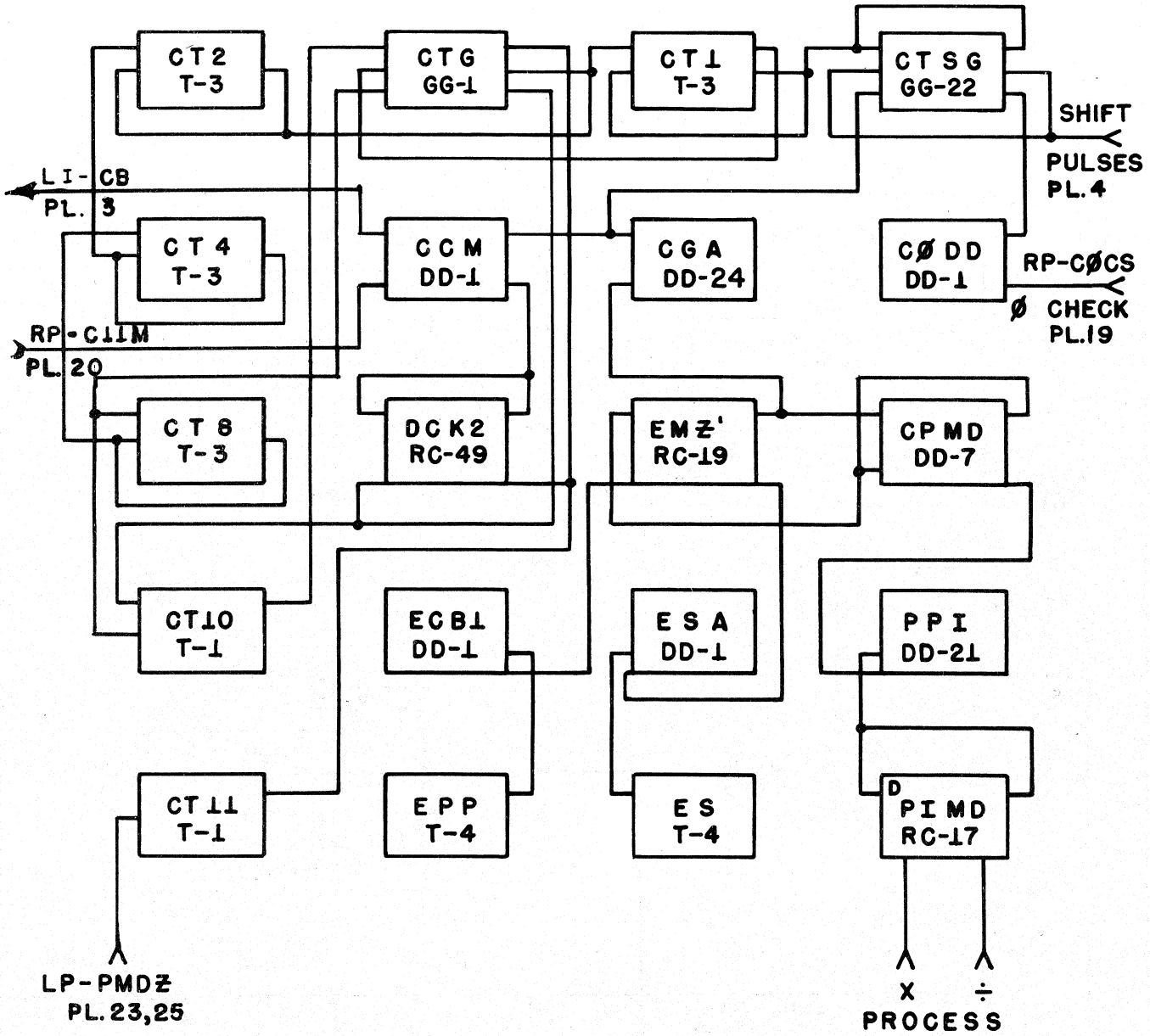
CONTROL RING

PLATE 39 C

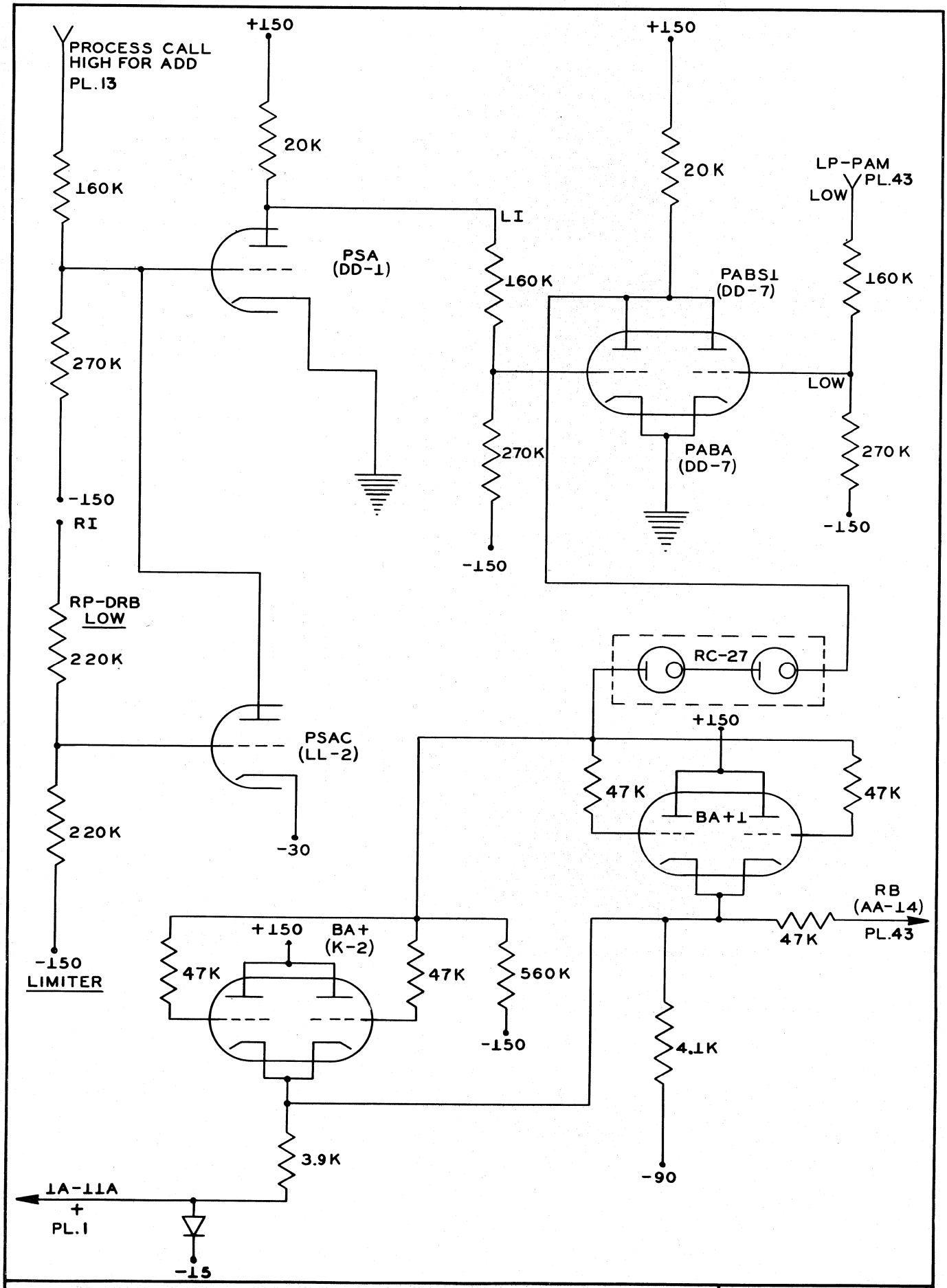


PROCESS CONTROL

PLATE 40 C

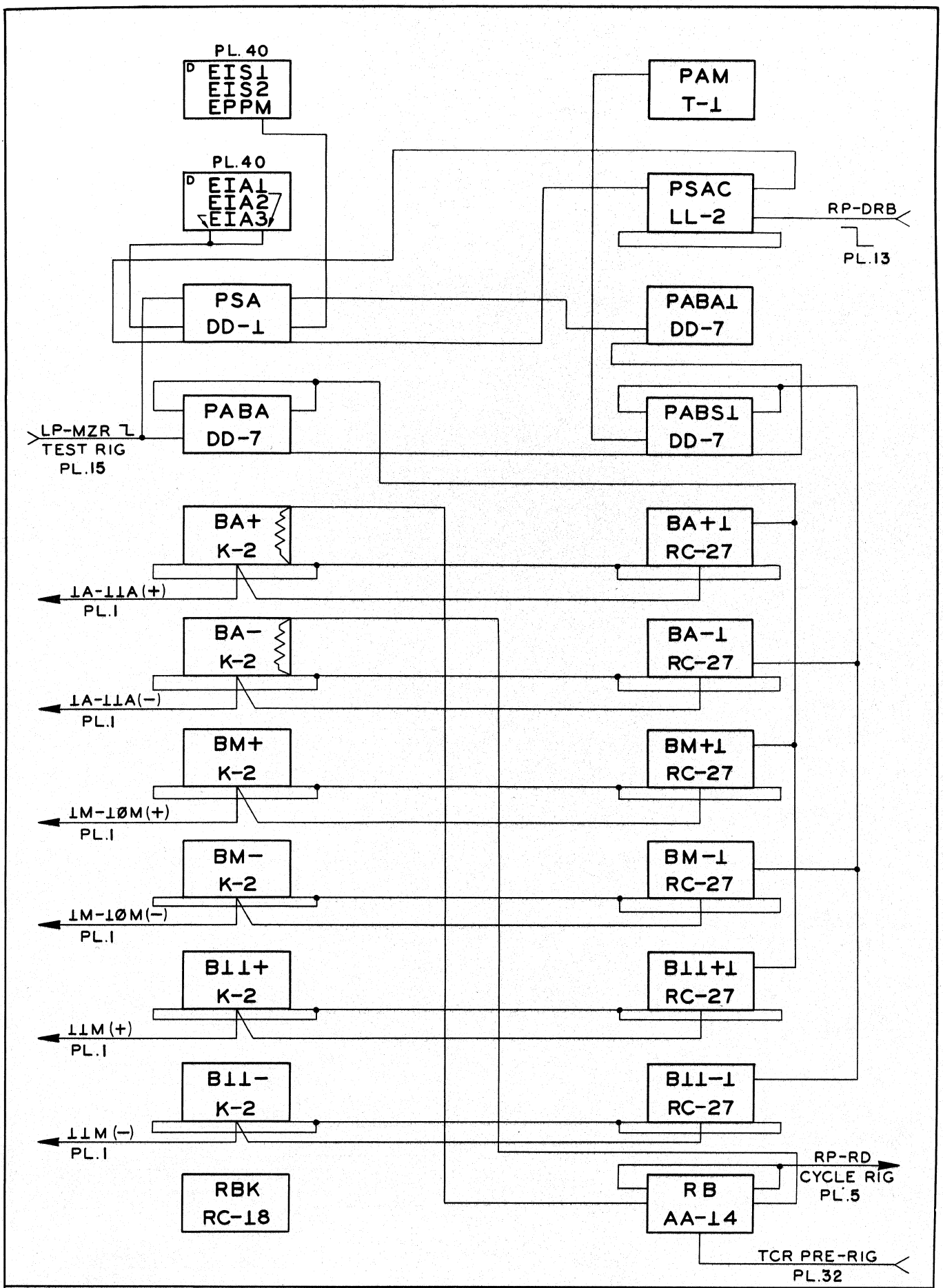


CONDITIONING CCT FOR SHIFTS | PLATE 41C

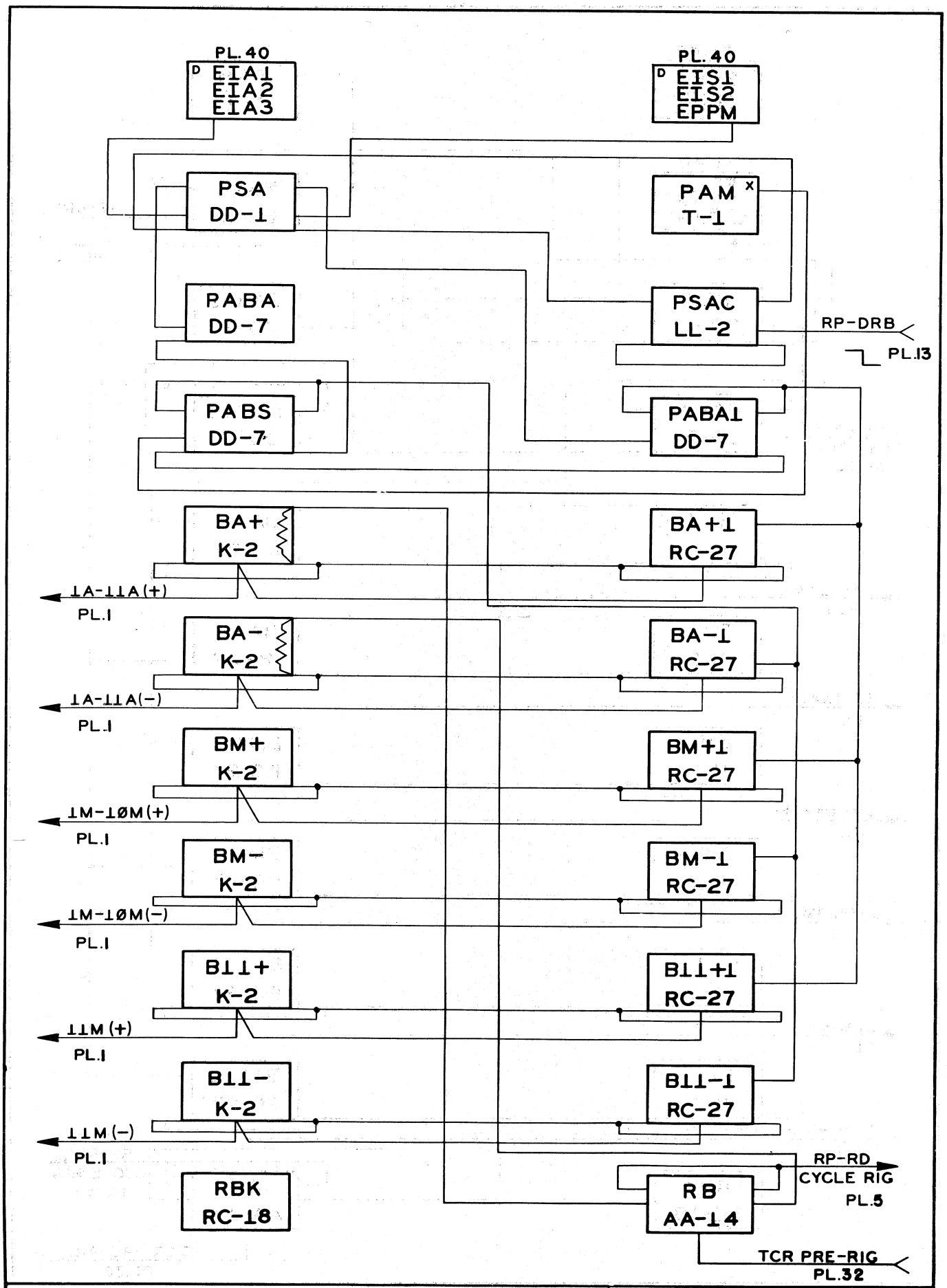


SIGN BIAS

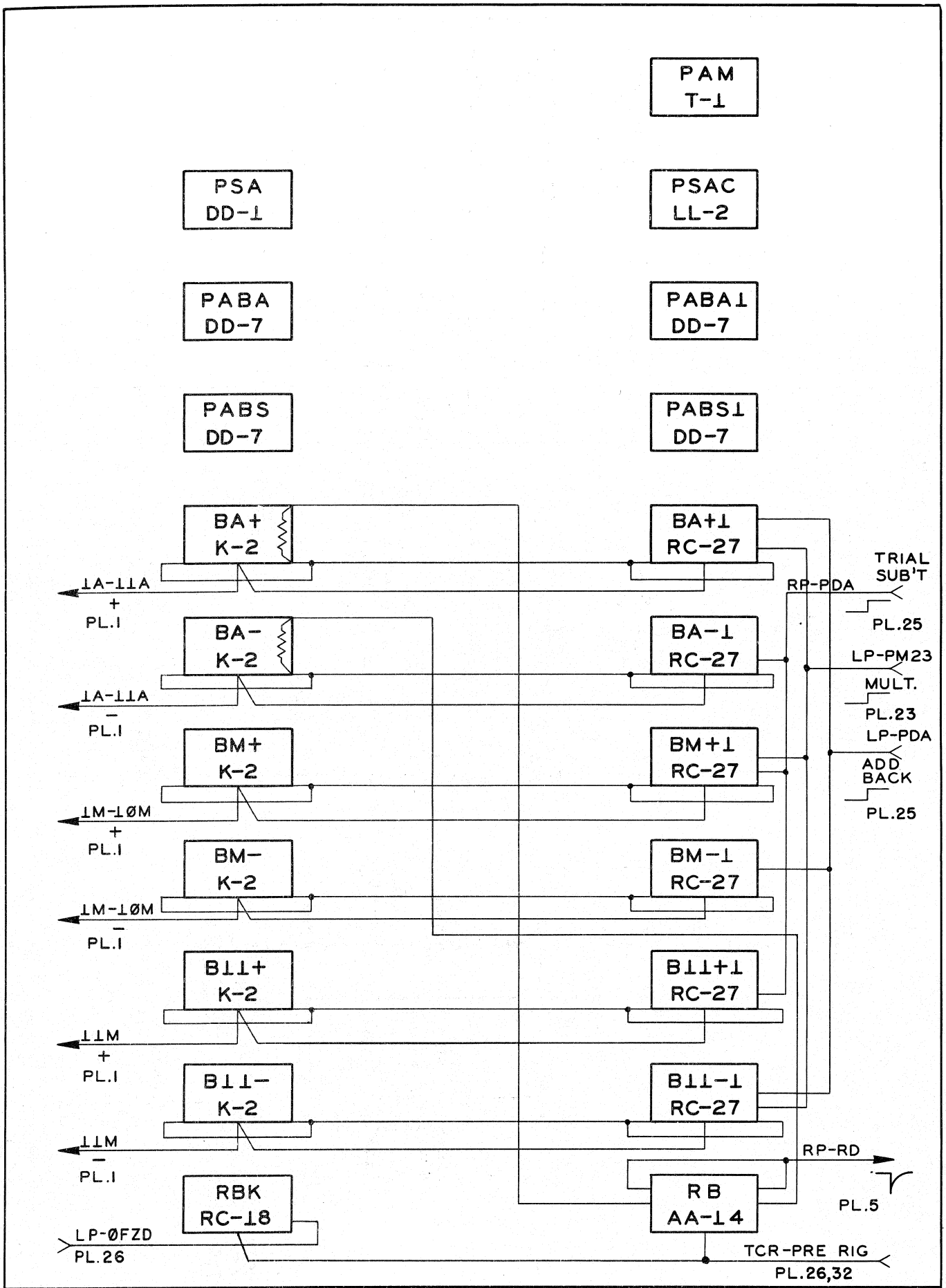
PLATE 42 C



SIGN BIAS - ADDITION & SUBTRACTION | PLATE 43 C



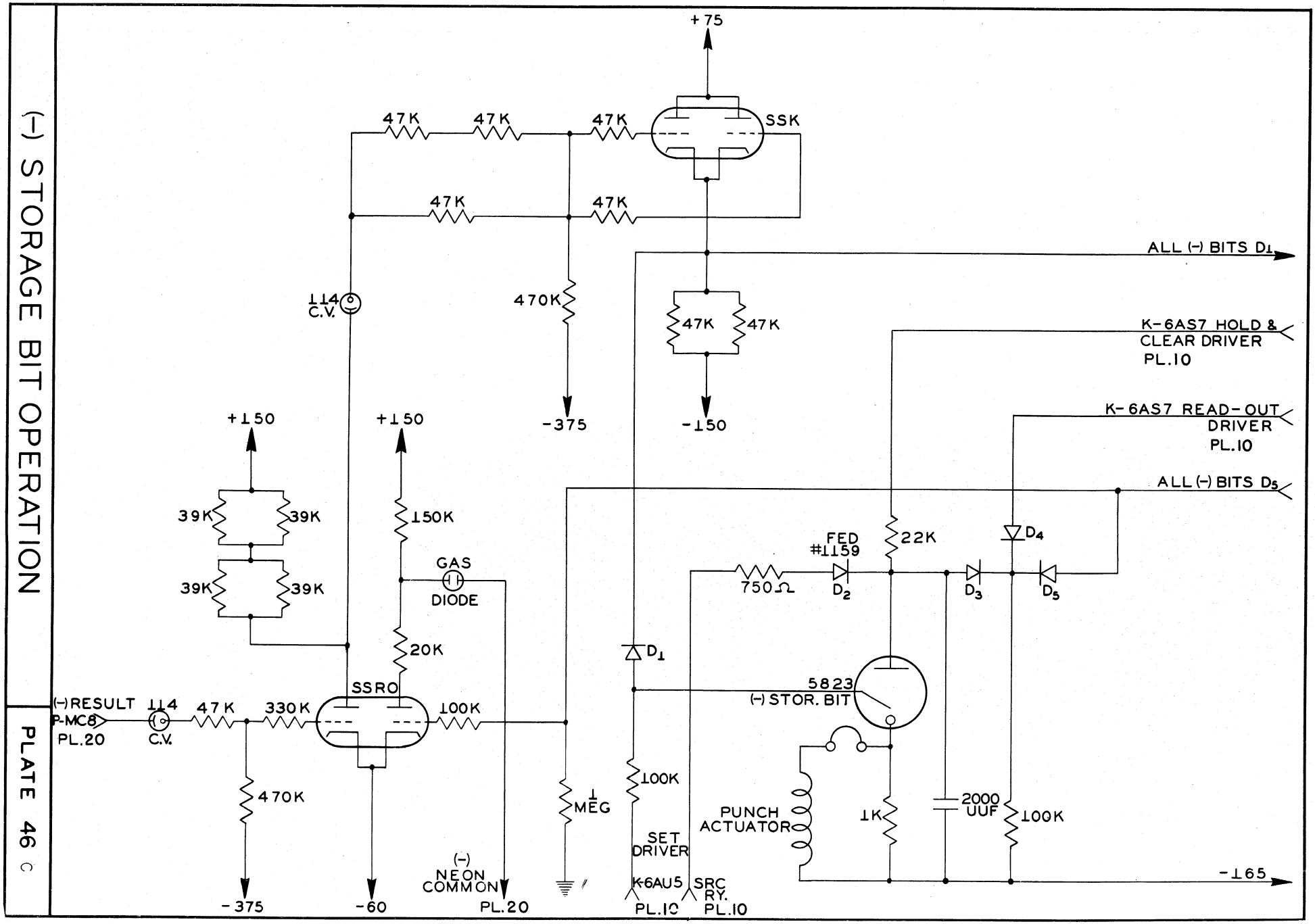
MINUS FACTOR-ADDITION & SUBTRACTION | PLATE 44 C

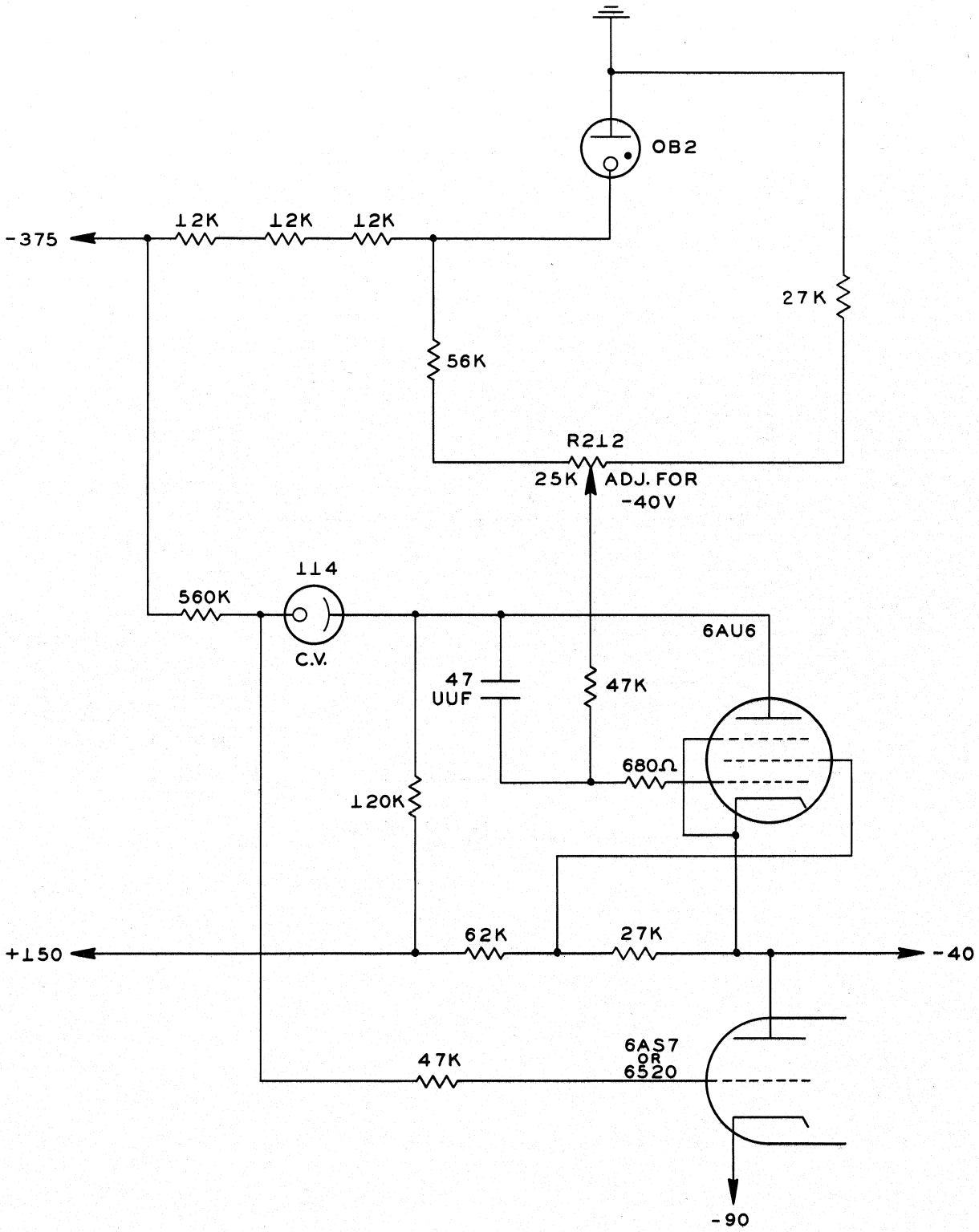


SIGN BIAS-DIVISION & MULTIPLICATION | PLATE 45 C

(-) STORAGE BIT OPERATION

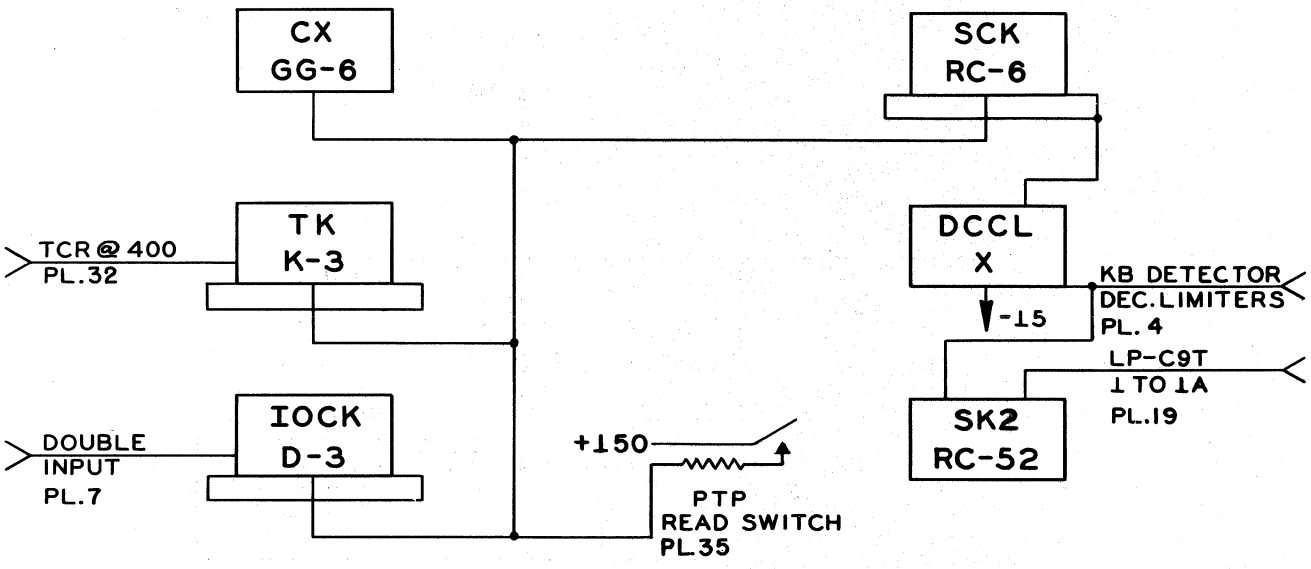
PLATE 46 C





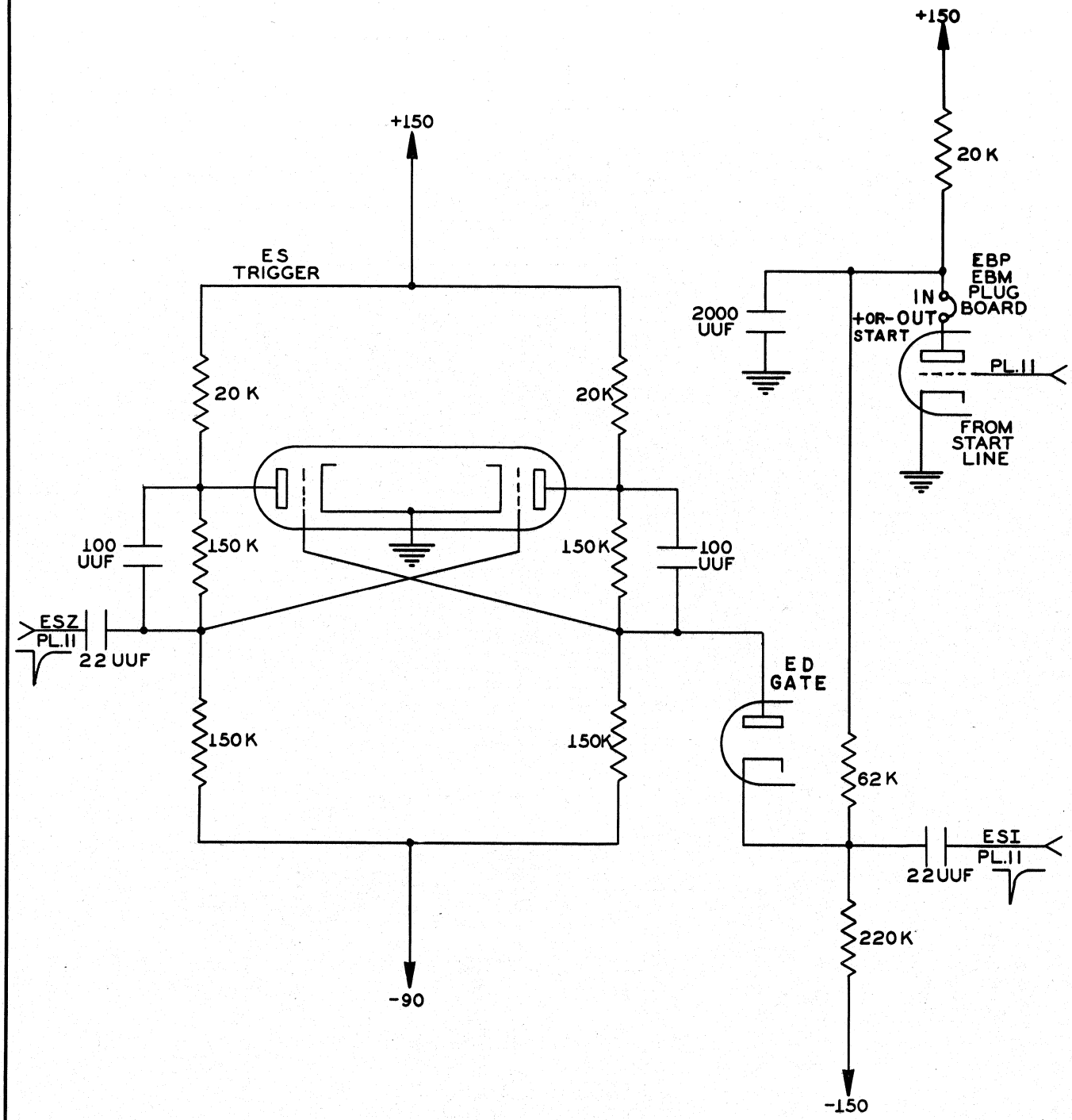
-40V REGULATED SUPPLY

PLATE 47 C



CATHODE CONTROLS ON CX

PLATE 48 C



STEP TRIGGER AND GATE | PLATE 49 C

CALCULATOR CRANK UP

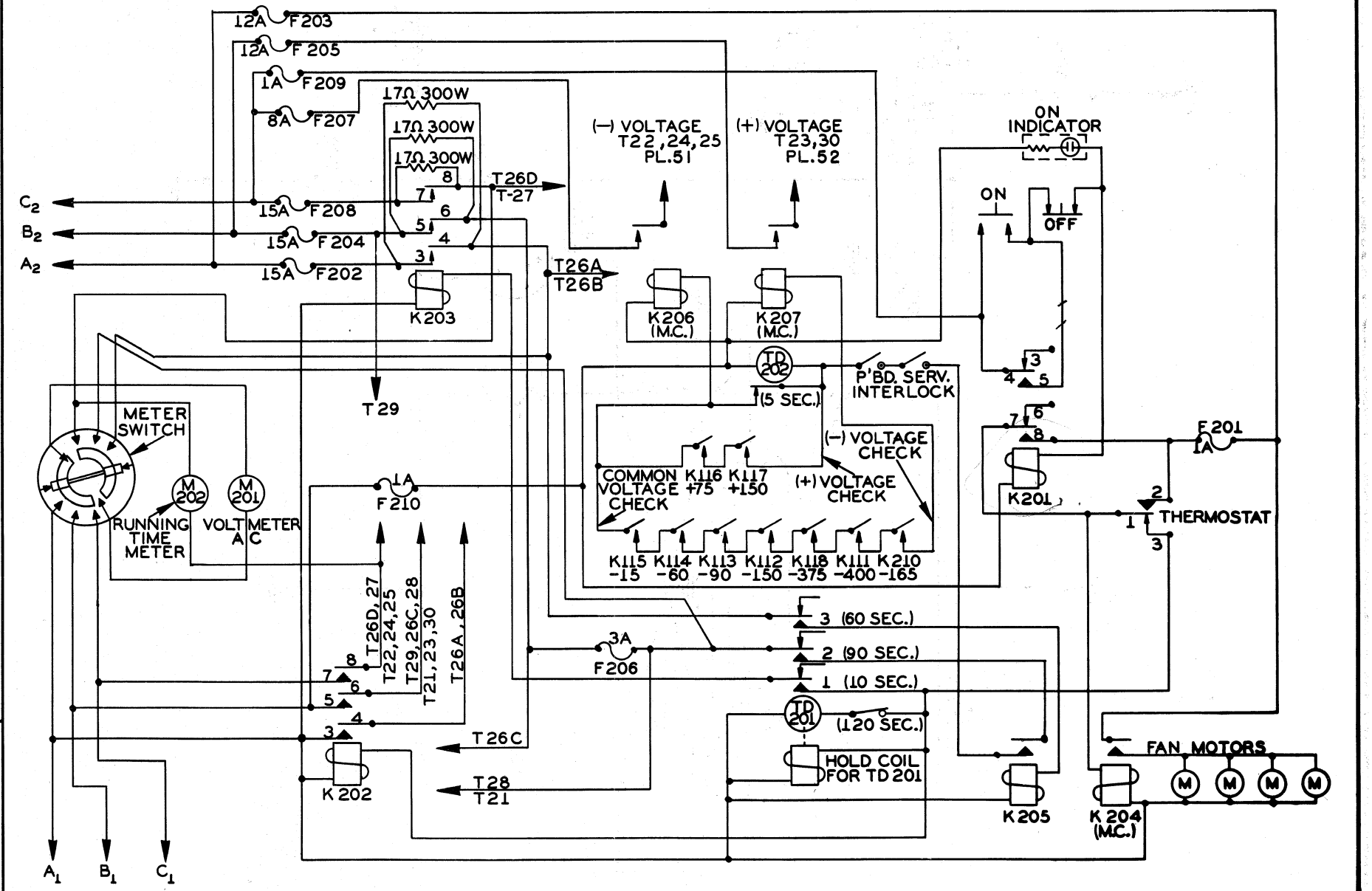
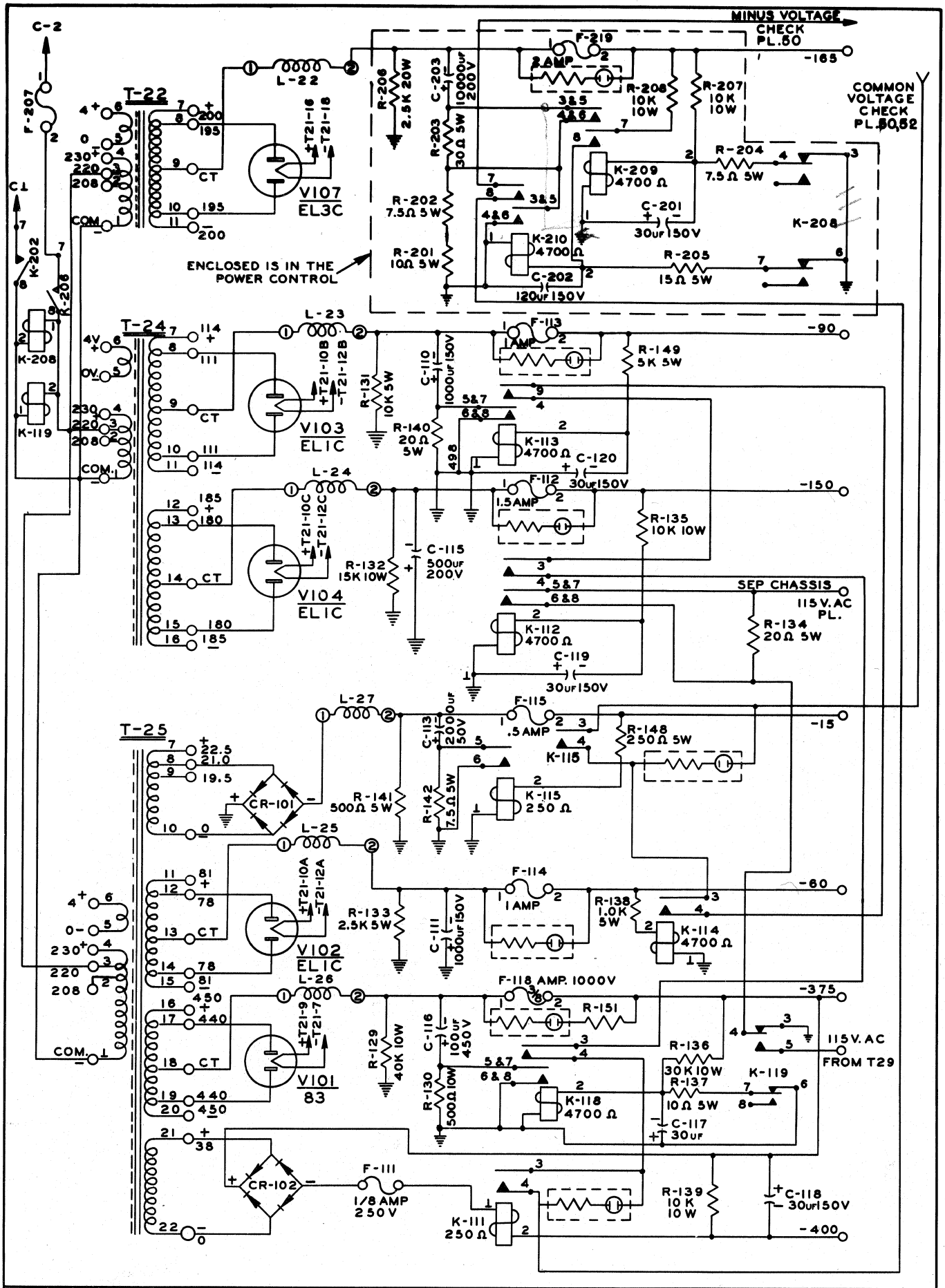


PLATE 50 C

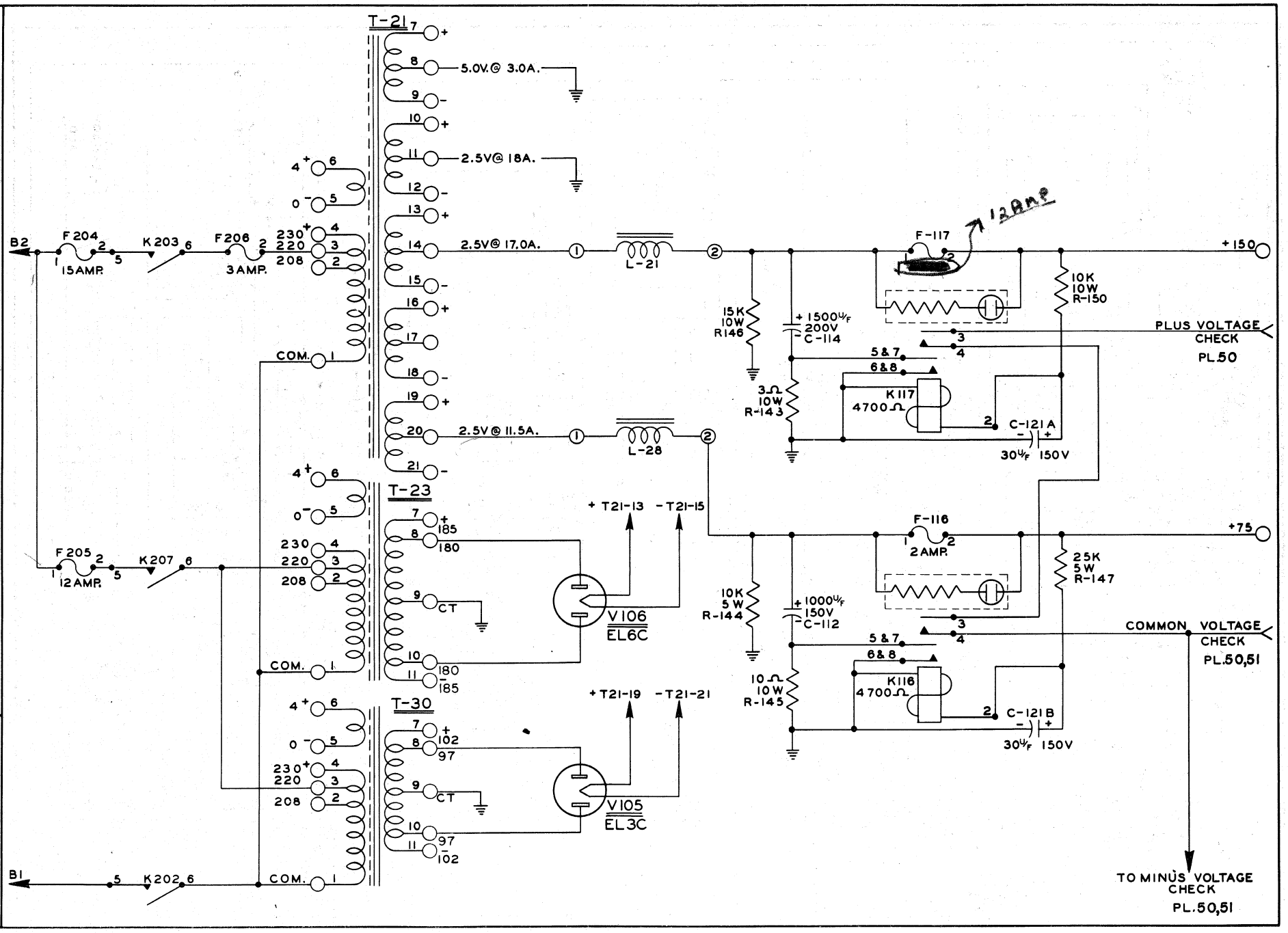


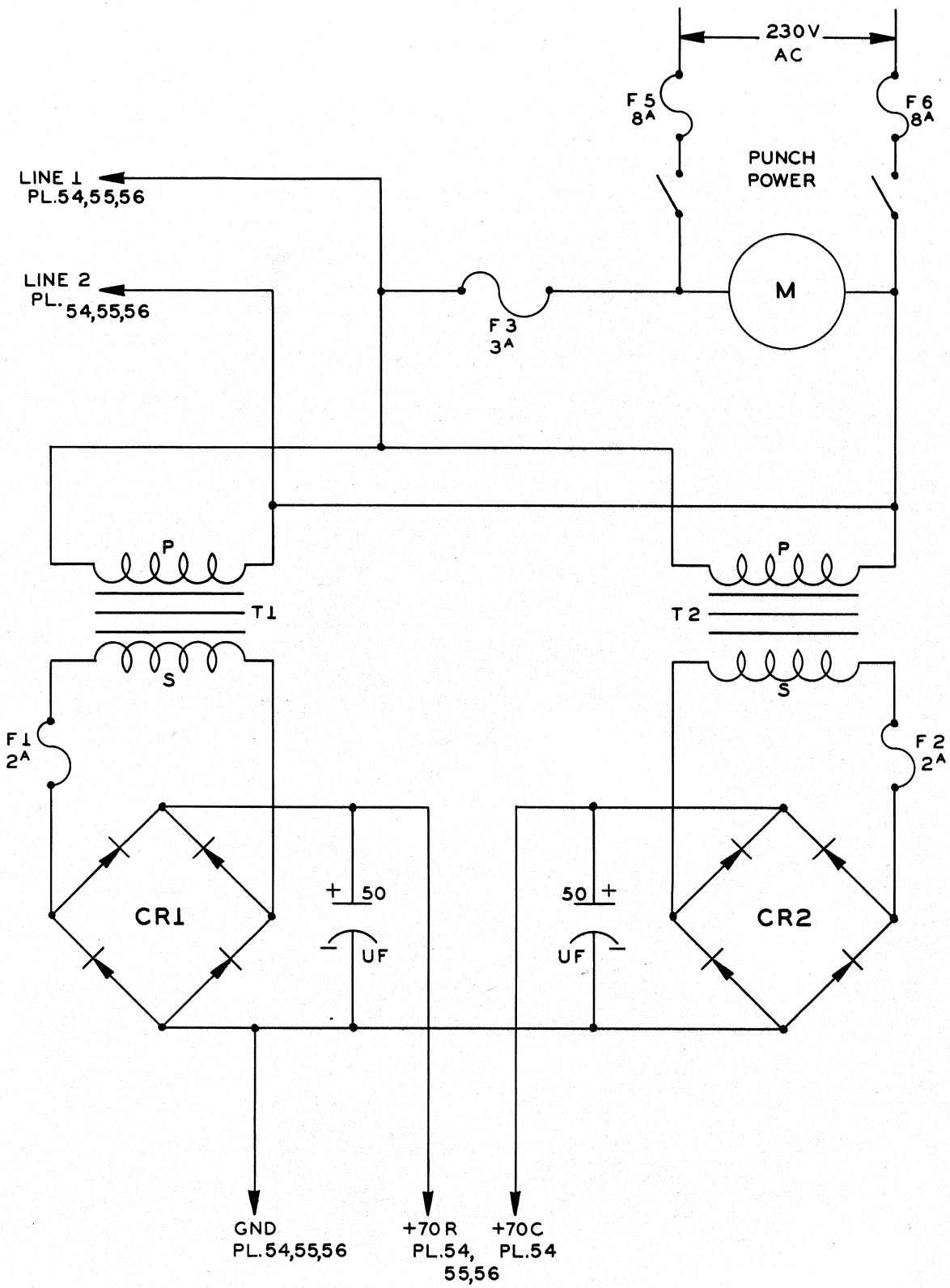
POWER SUPPLY MINUS VOLTAGES

PLATE 51 C

POWER SUPPLY PLUS VOLTAGES

PLATE 52 C





PUNCH POWER SUPPLY

PLATE 53 C

PUNCH CLUTCH & BRAKE OPERATION

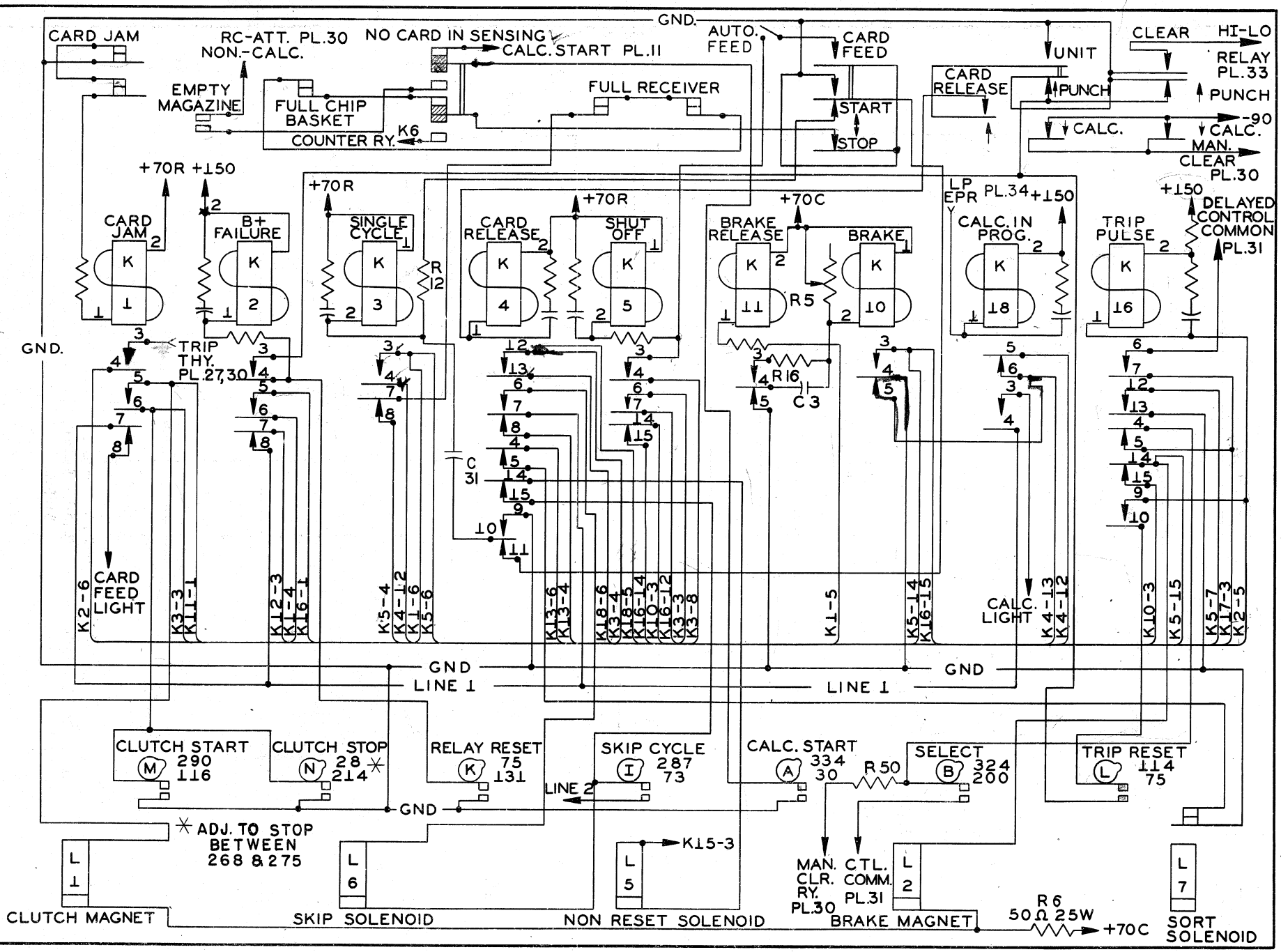
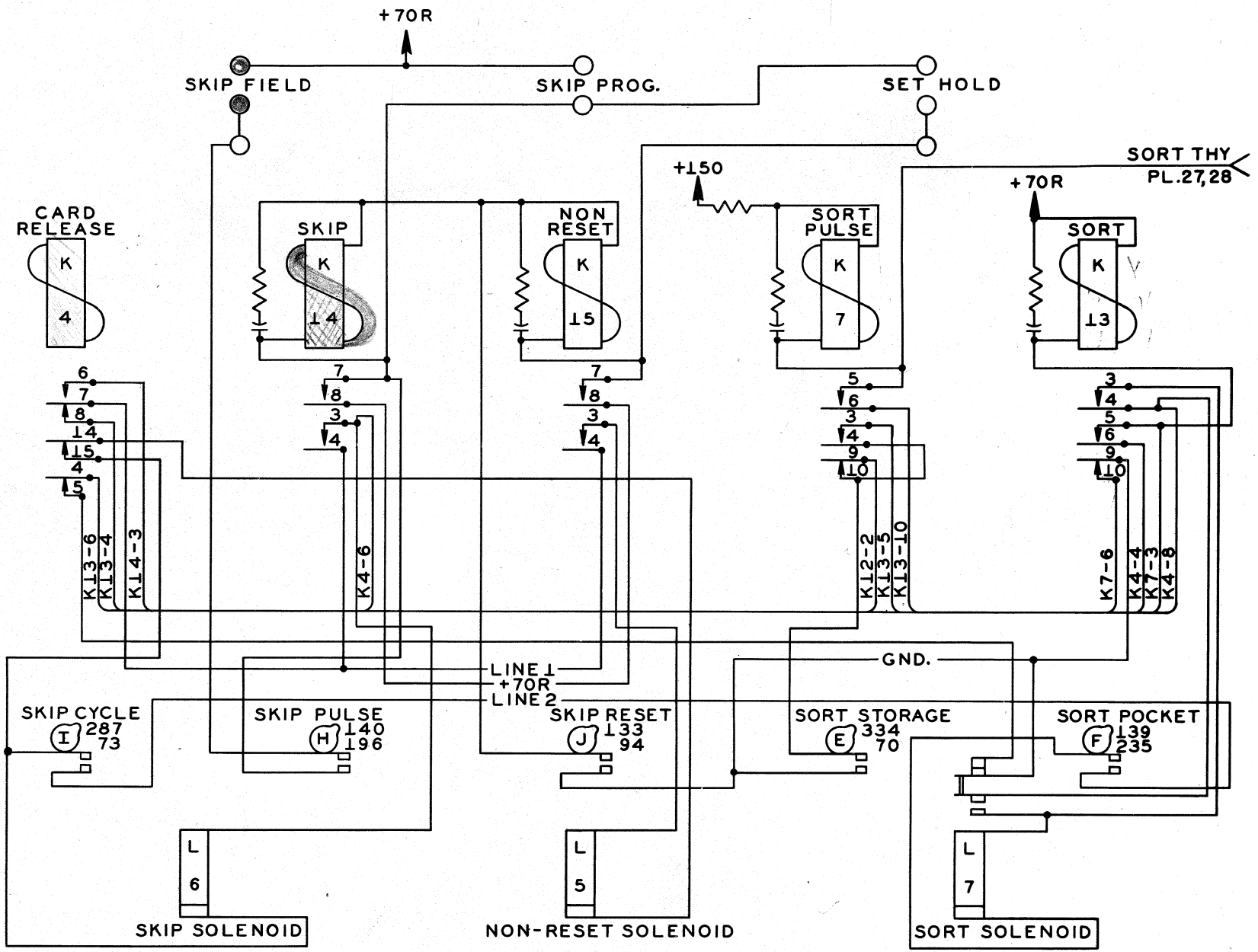


PLATE 54 C

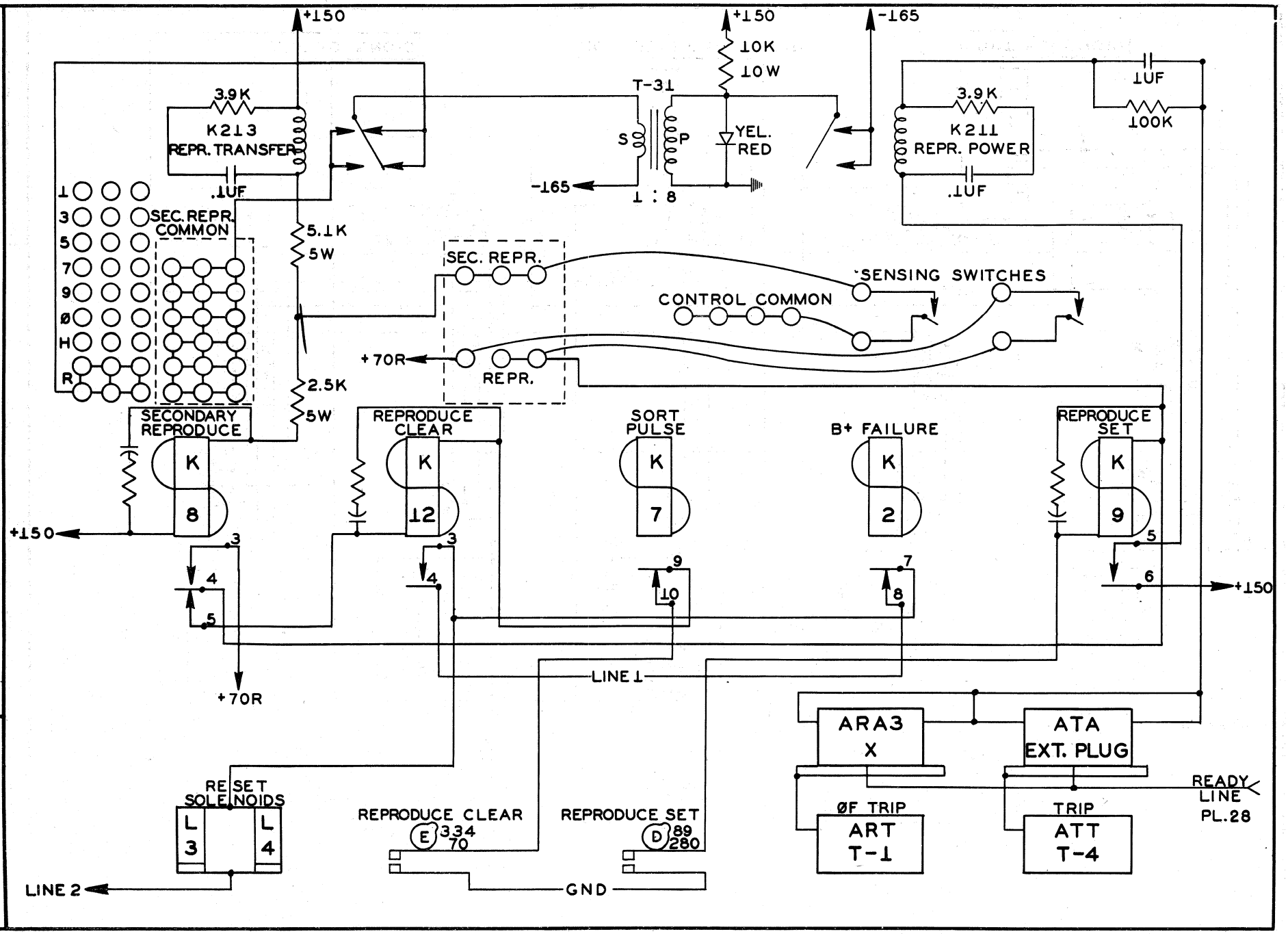
SORT, SKIP & SET HOLD

PLATE 55c



REPRODUCE & SECONDARY REPRODUCE.

PLATE 56 C



CALCULATOR-FRONT VIEW

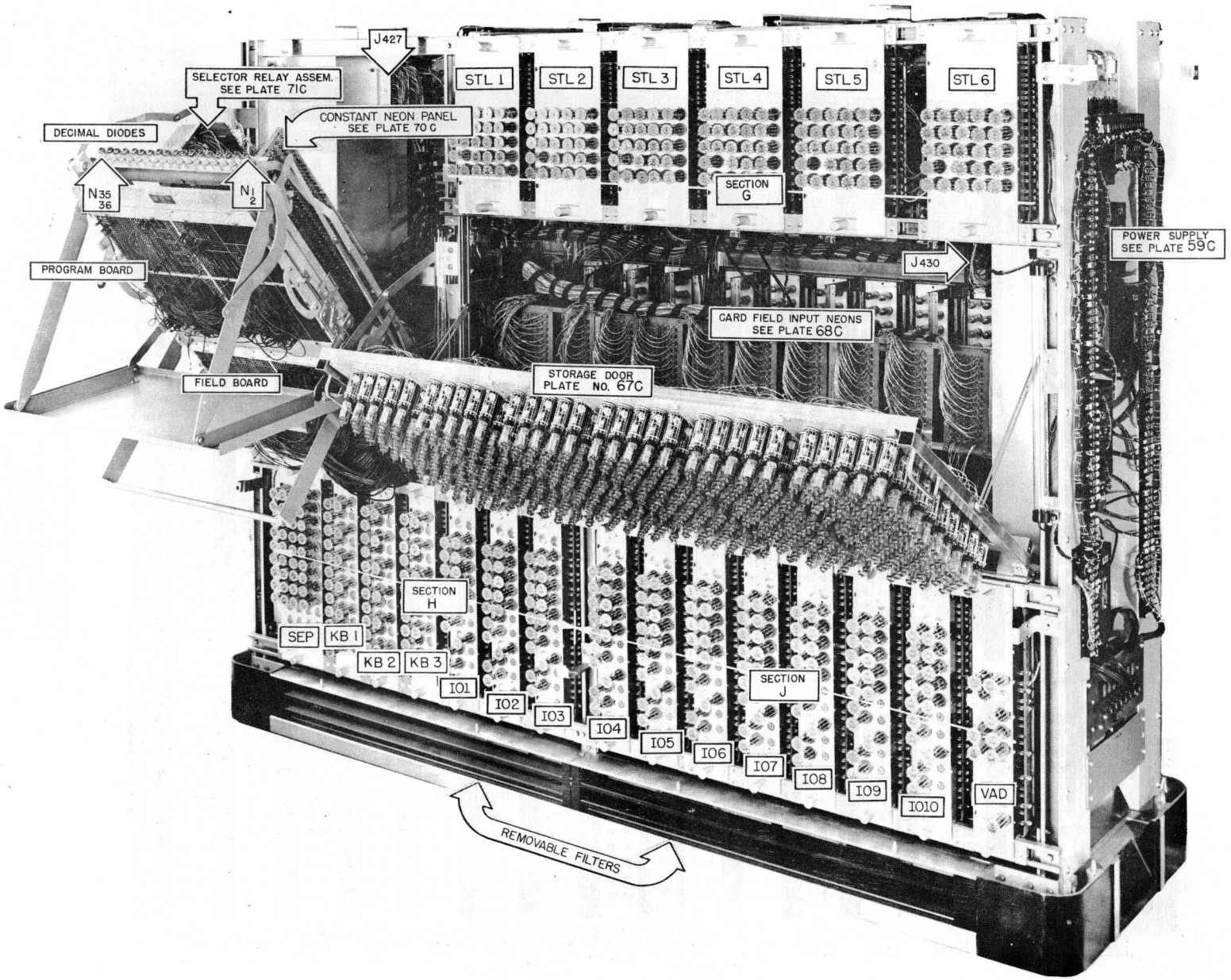
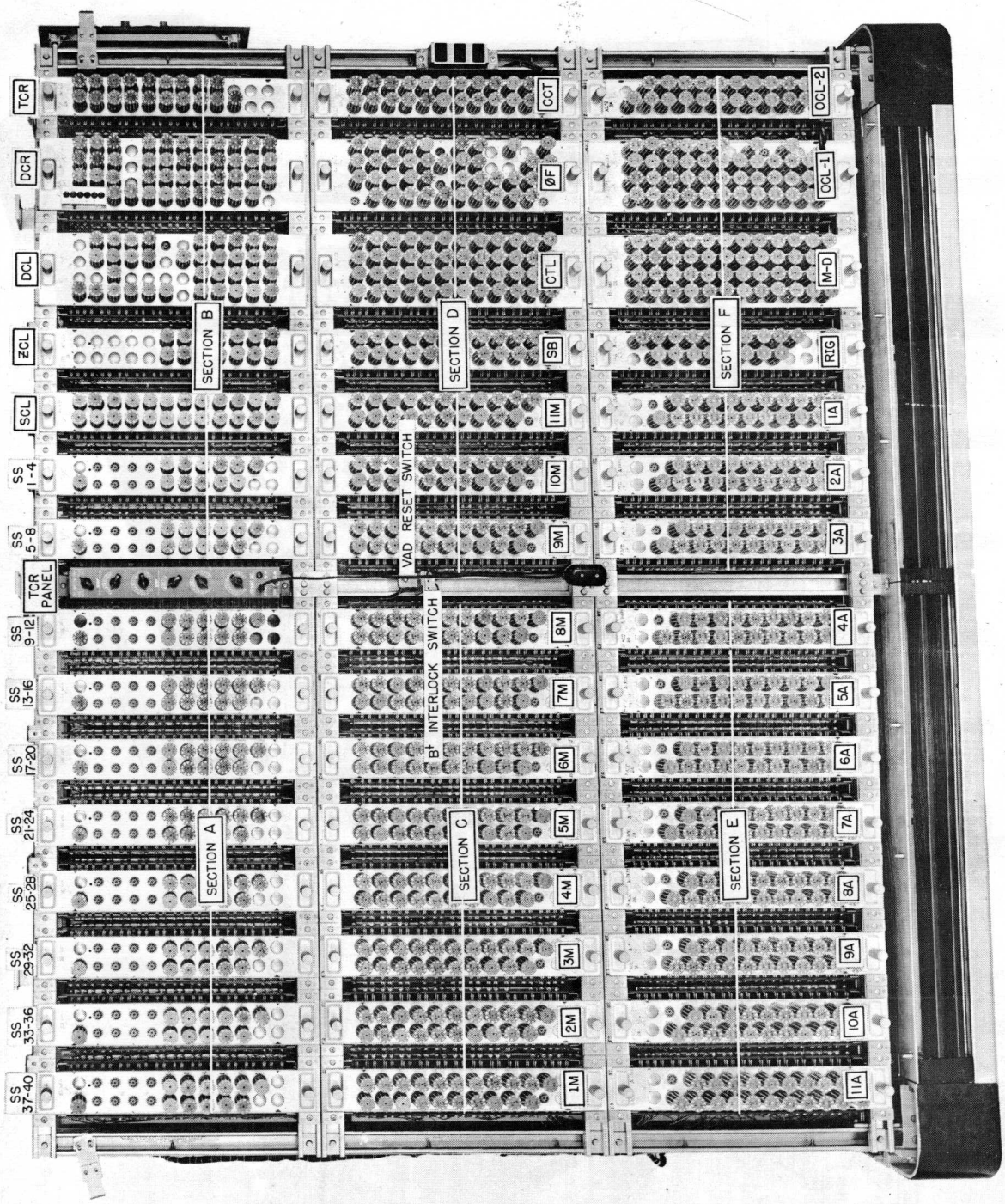


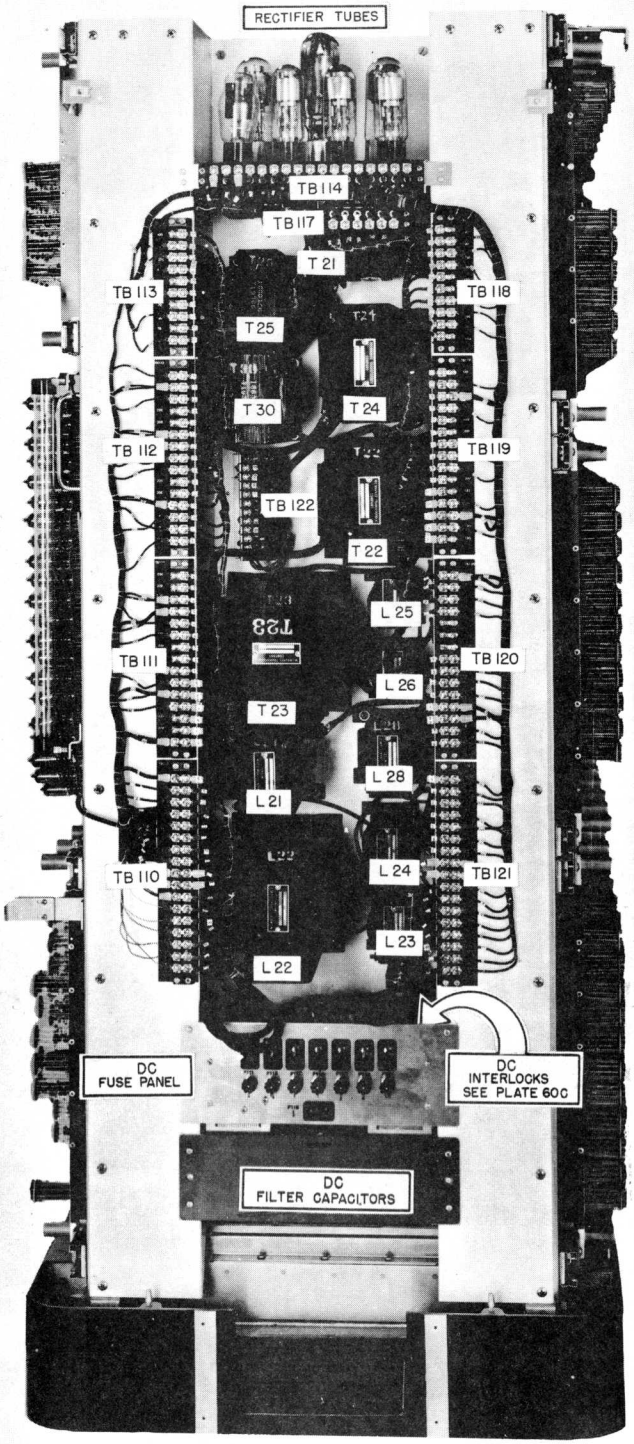
PLATE 57C



NOTE -
SECTION LOCATIONS REFER TO
WIRING DISTRIBUTION
AS SHOWN ON PLATE 65 C

CALCULATOR - REAR VIEW

PLATE 58 C



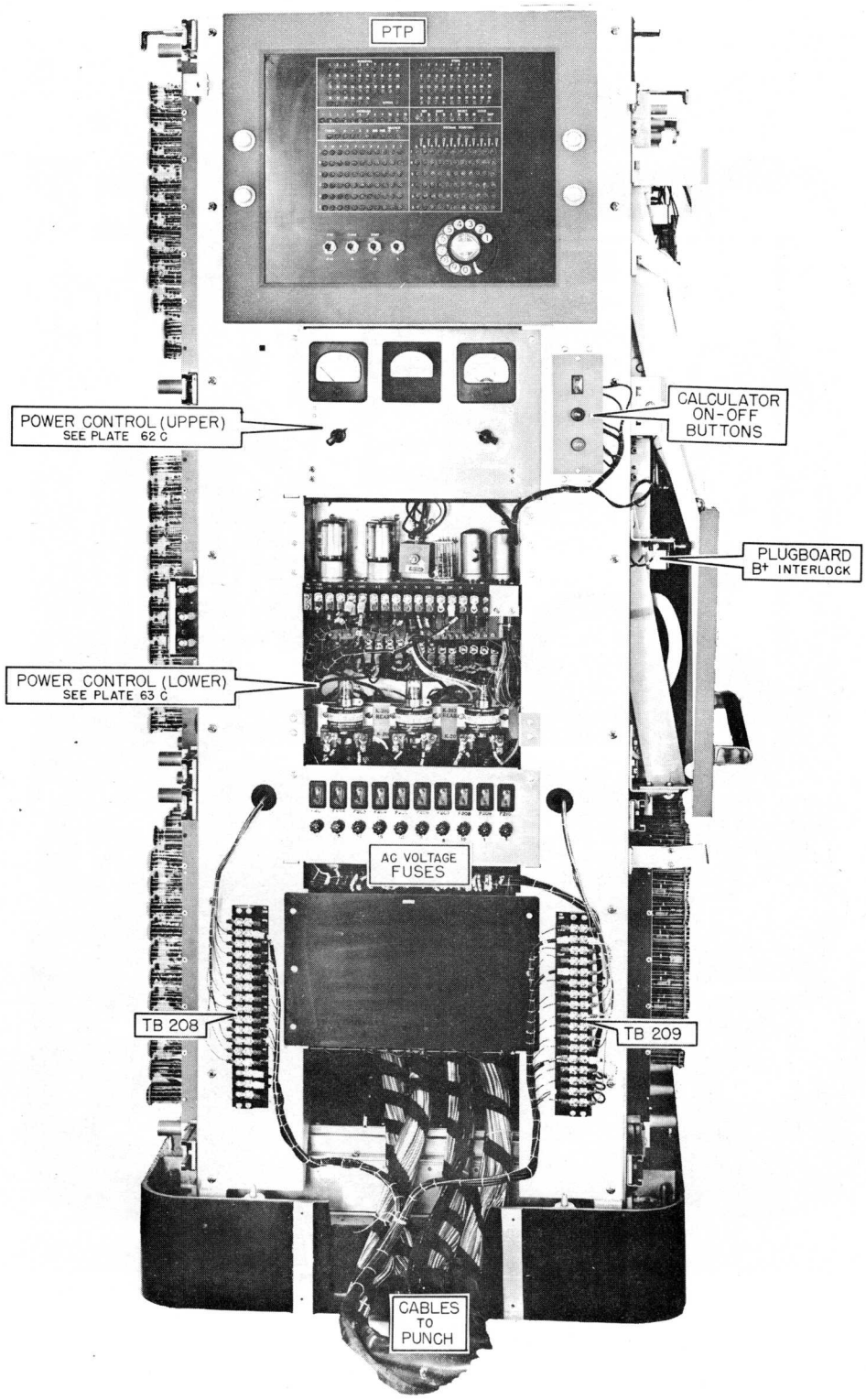
NOTE :-
CR 101 (-15) & CR 102 (-25)
ARE LOCATED BEHIND TB 122

POWER SUPPLY

PLATE 59 C

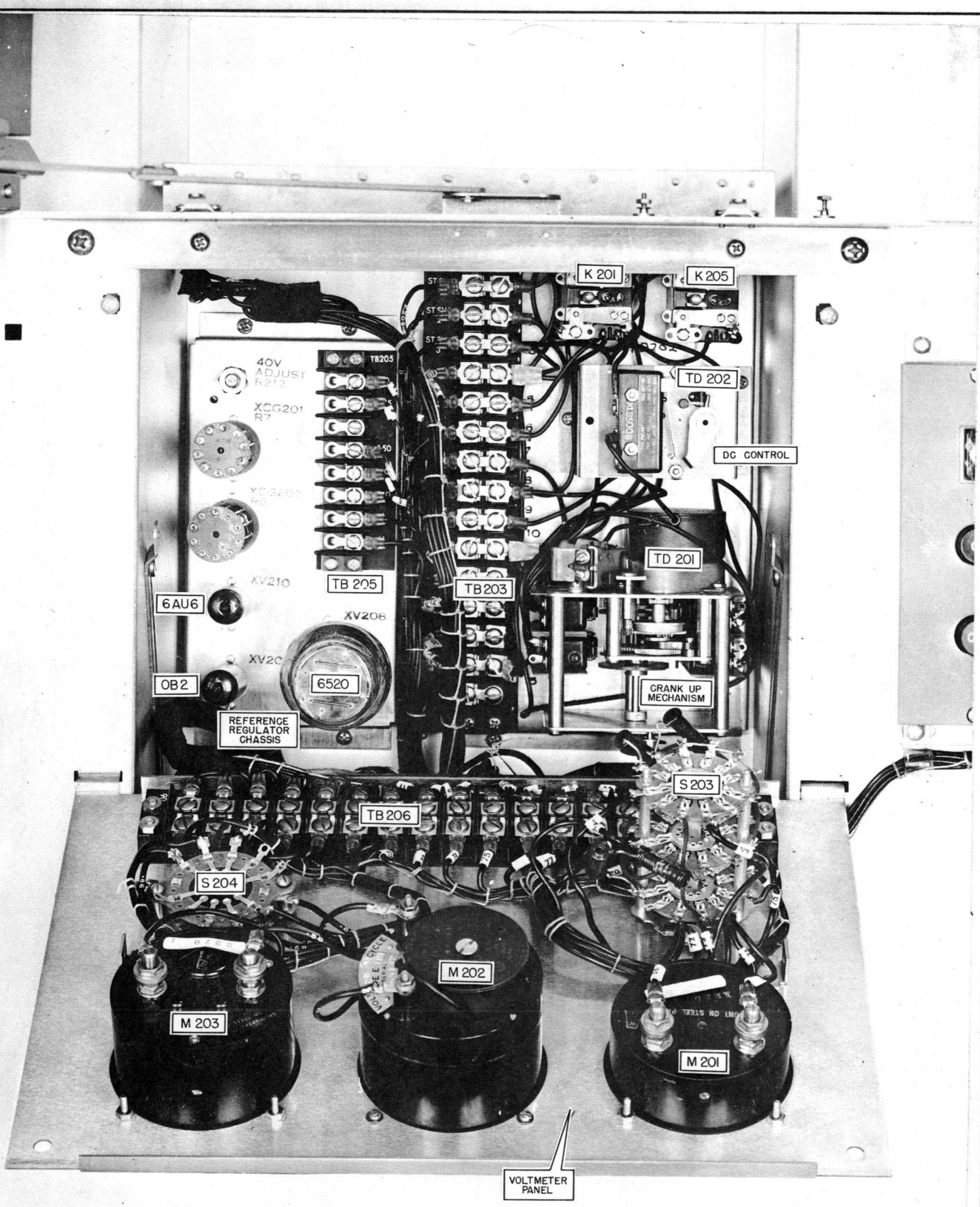
DC INTERLOCK RELAY ASSEMBLY

PLATE 60C



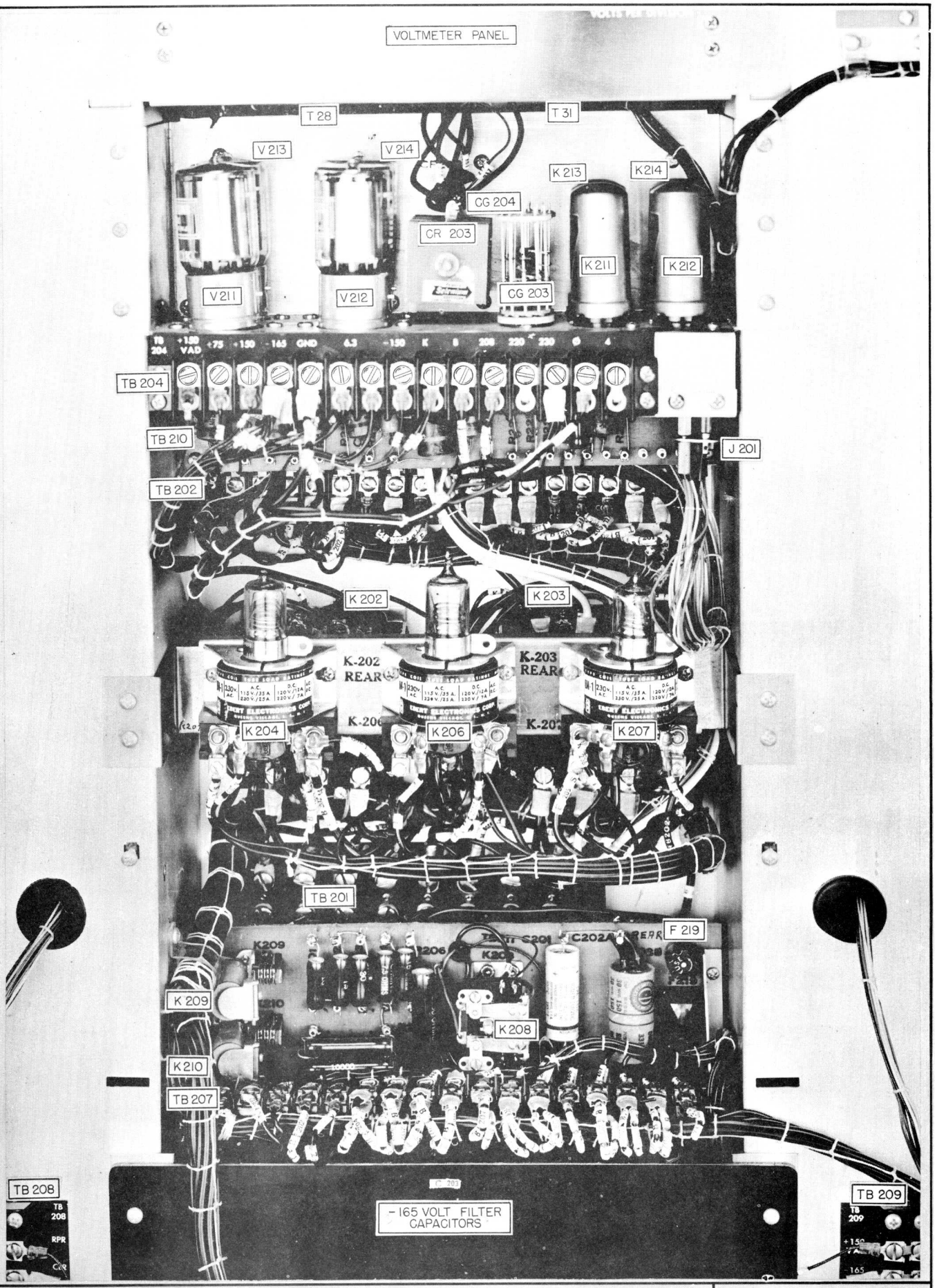
PTP & POWER CONTROL

PLATE 61 C



POWER CONTROL- UPPER

PLATE 62 C



POWER CONTROL - LOWER

PLATE 63C

FILAMENT TRANSFORMERS & FAN MOTORS

PLATE 64C

COMPUTER WIRING DISTRIBUTION

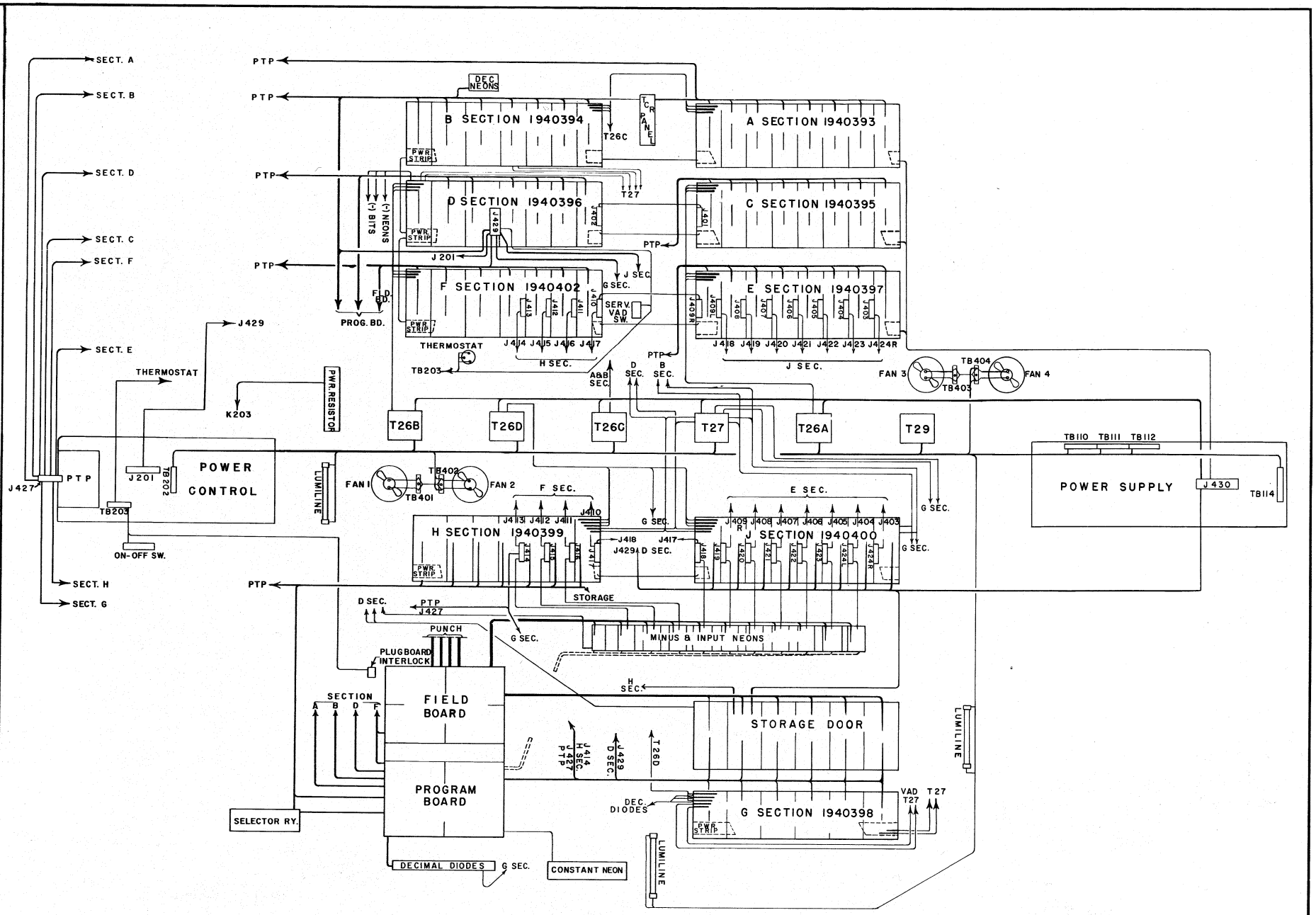


PLATE 65 C

STA CHASSIS

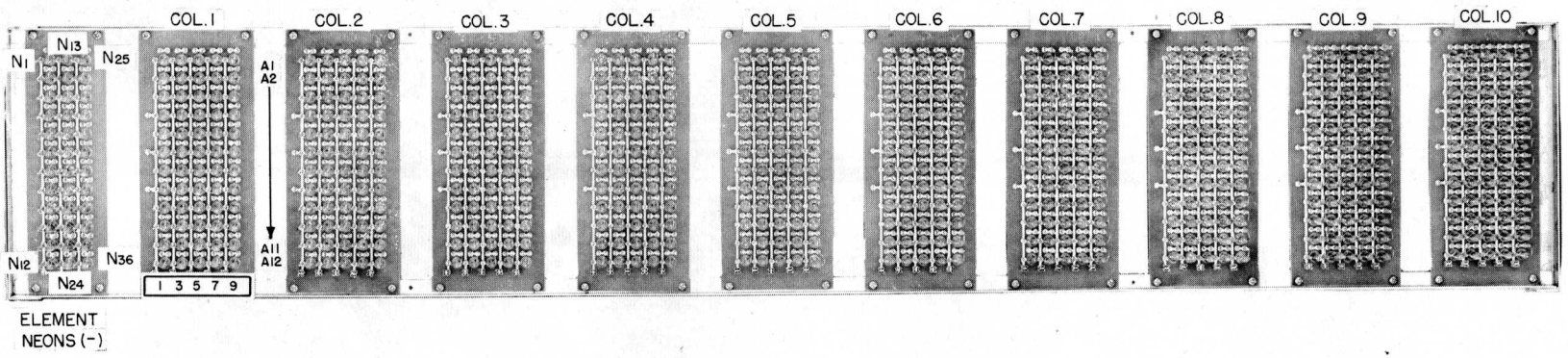
PLATE 66 C

STORAGE DOOR

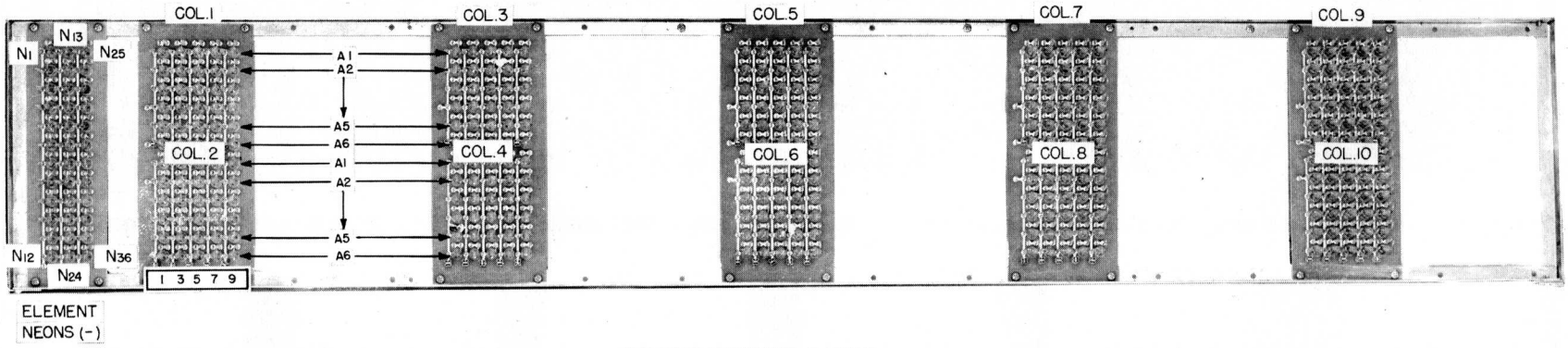
PLATE 67 C

60 & 120 FIELD INPUT NEONS

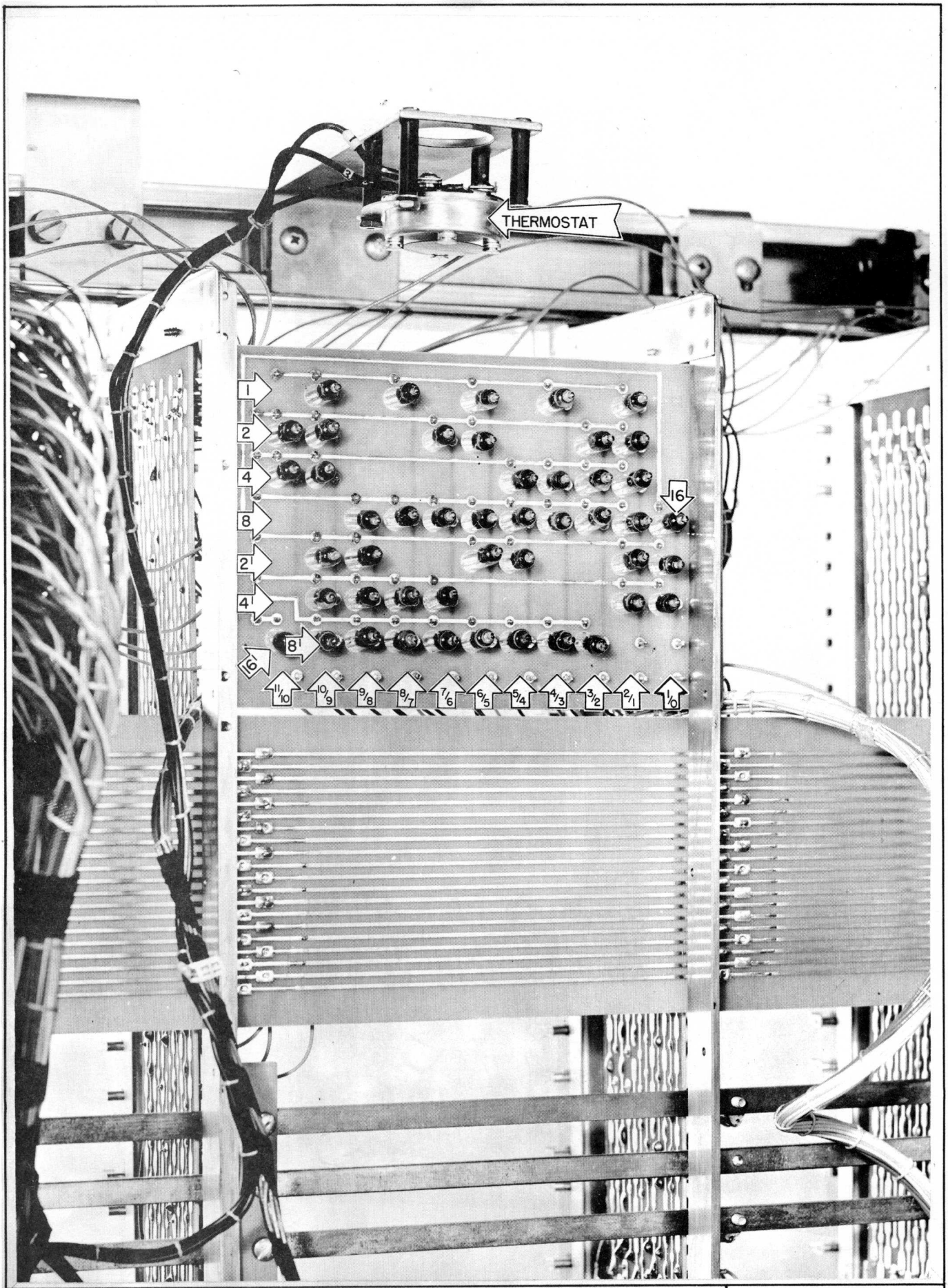
PLATE 68C



UNIVAC 120
12 INPUT FIELDS



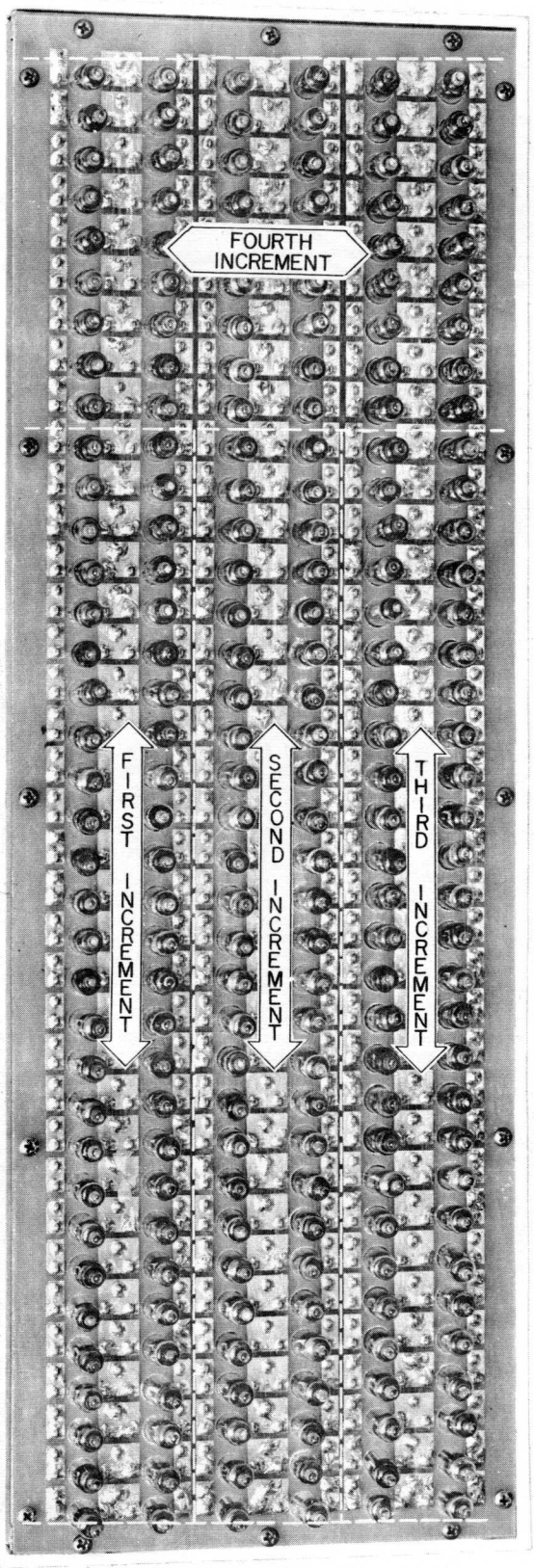
UNIVAC 60
6 INPUT FIELDS



DECIMAL NEON MIXER BOARD

PLATE 69 C

TOP



CONSTANT NEON PANEL

PLATE 70 C

SELECTOR RELAY ASSEMBLY

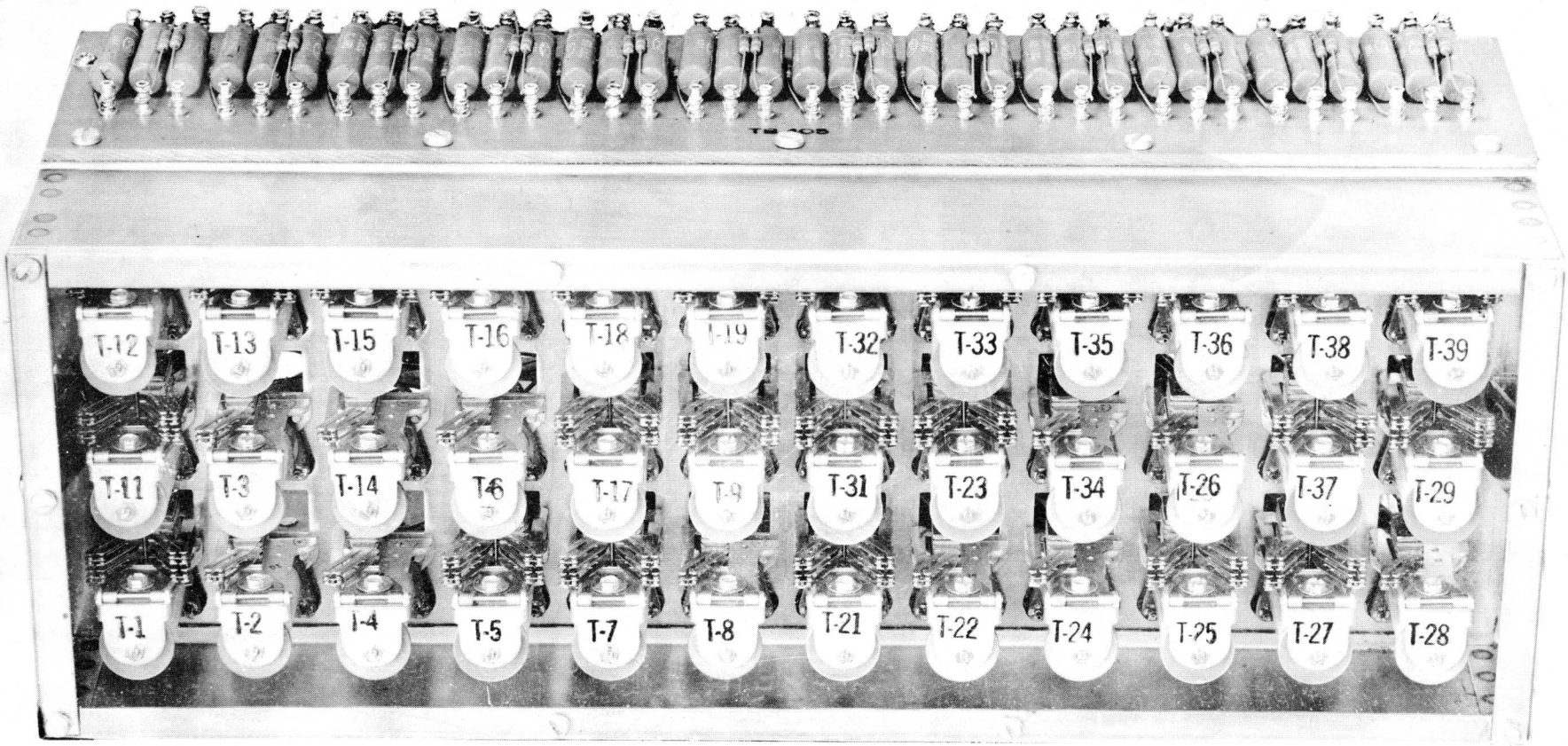
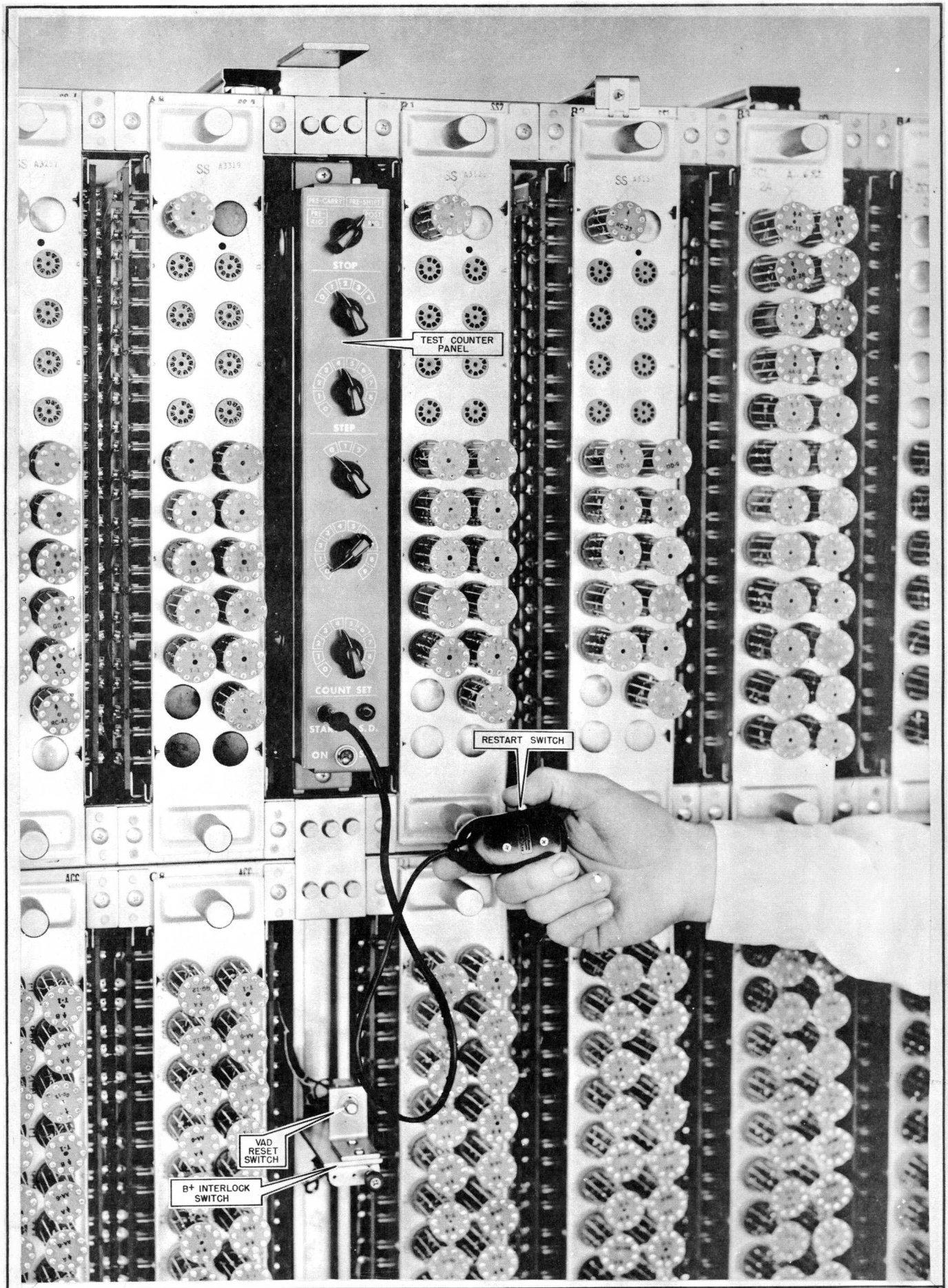
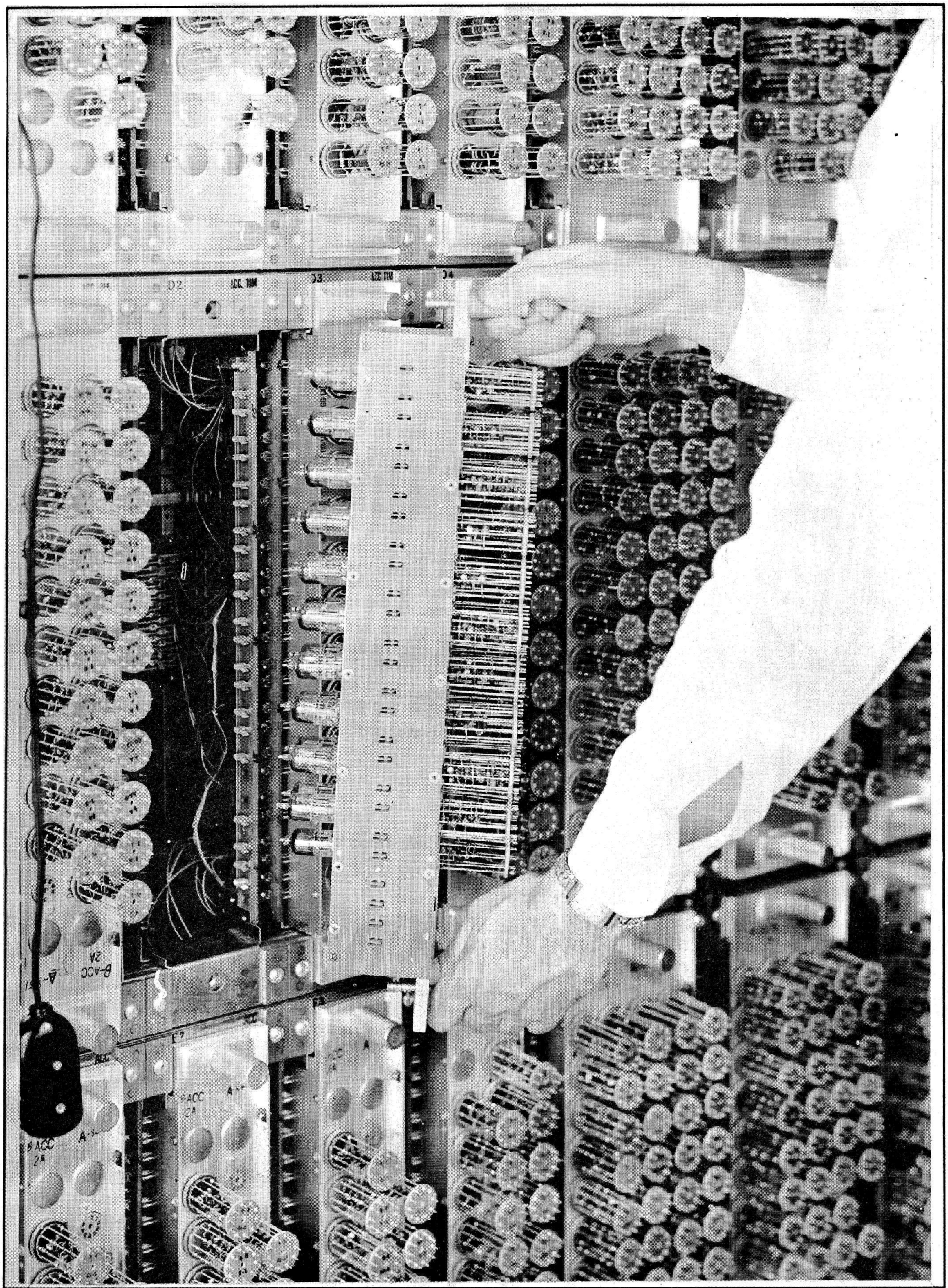


PLATE 71C



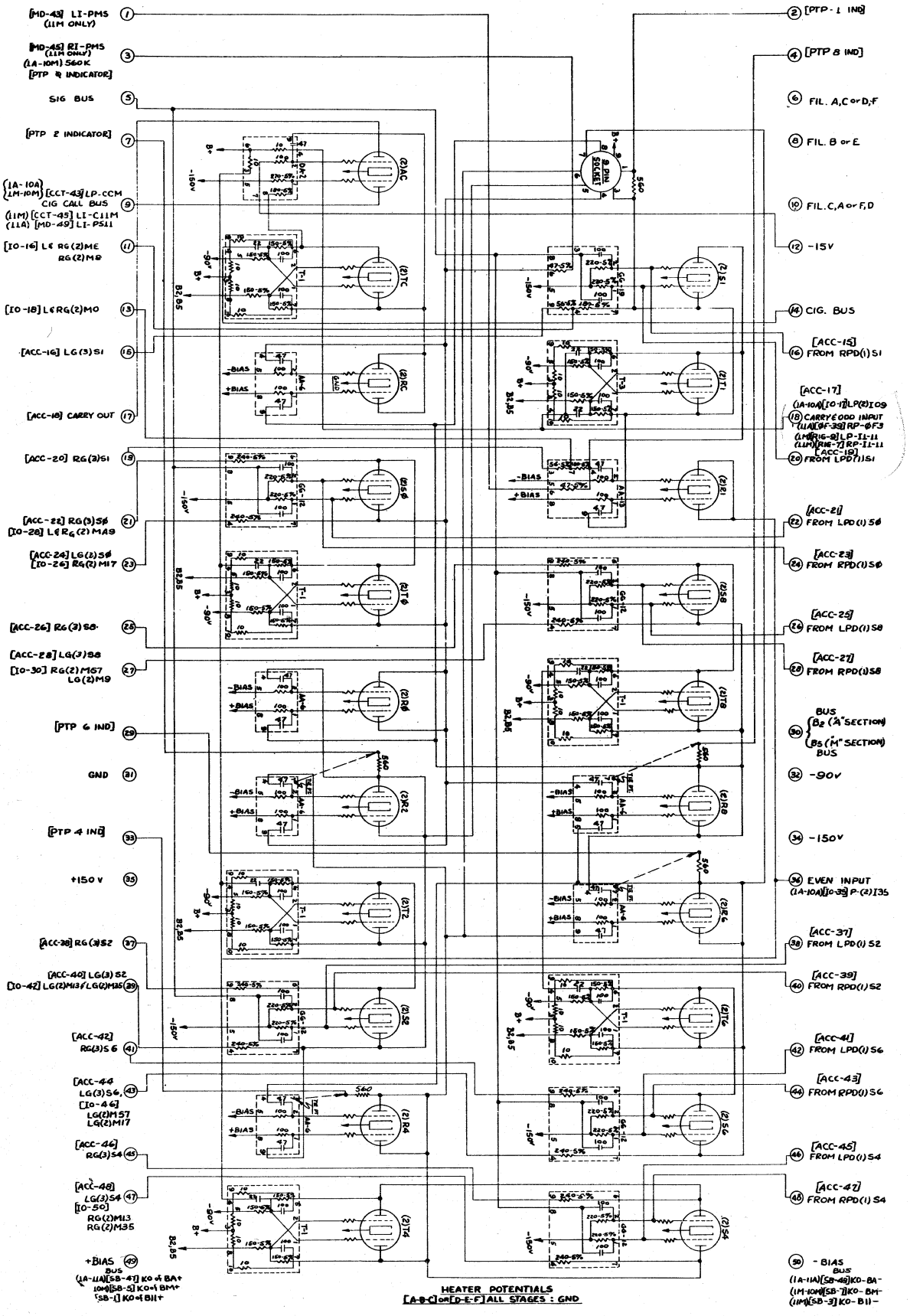
RESTART SWITCH & TCR PANEL

PLATE 72C



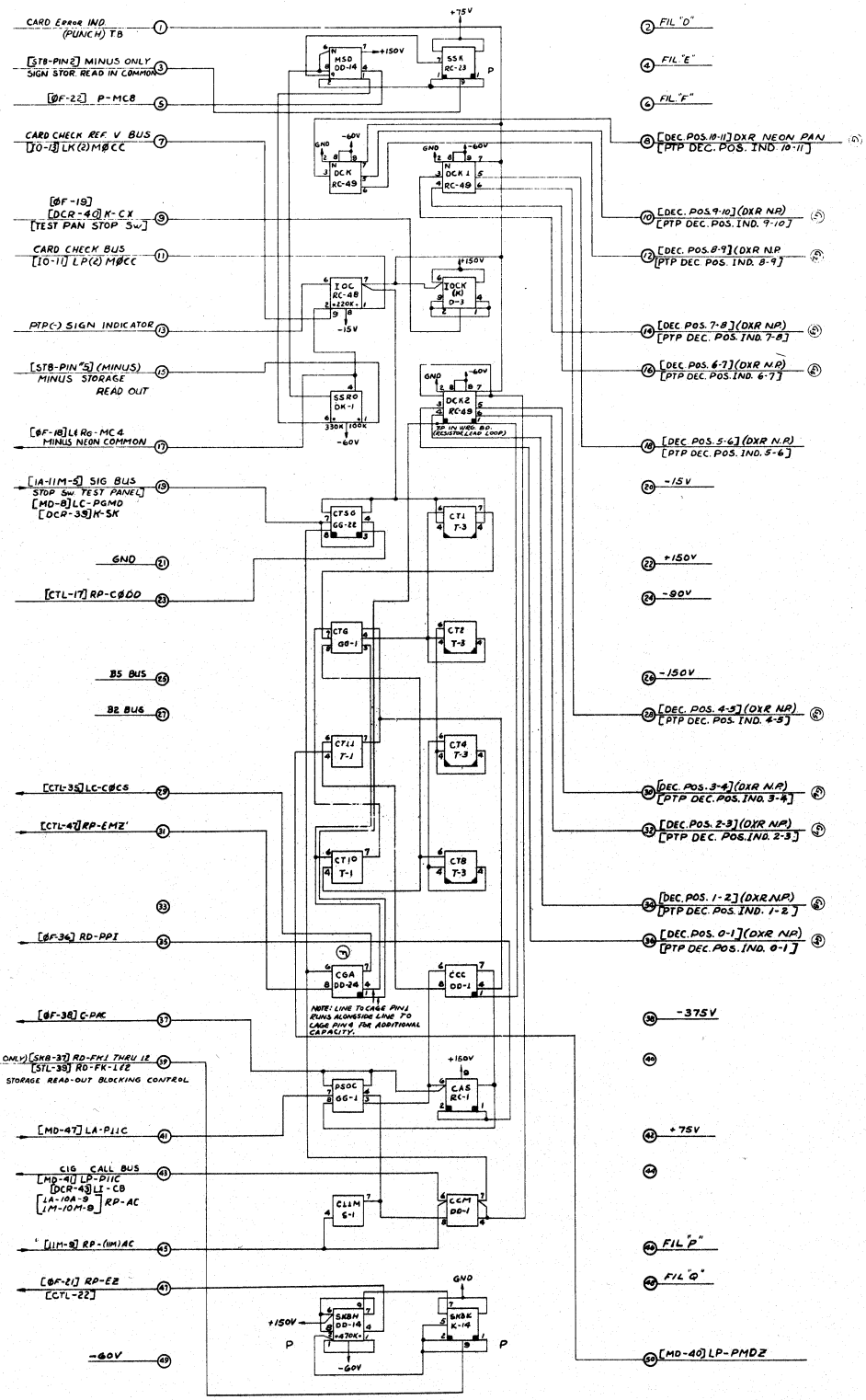
CHASSIS REMOVAL

PLATE 73C



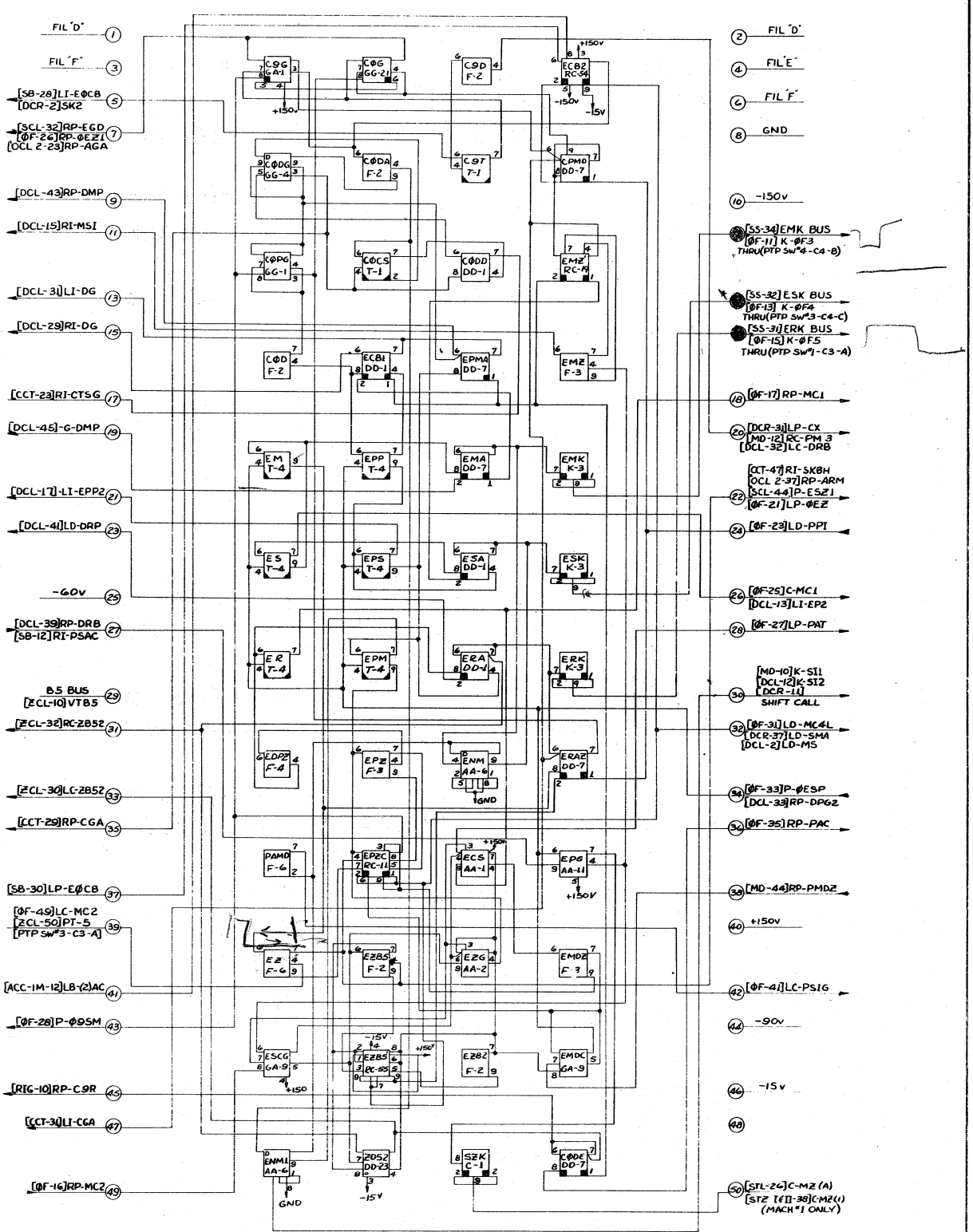
ACCUMULATOR (ACC)

PLATE 74 C



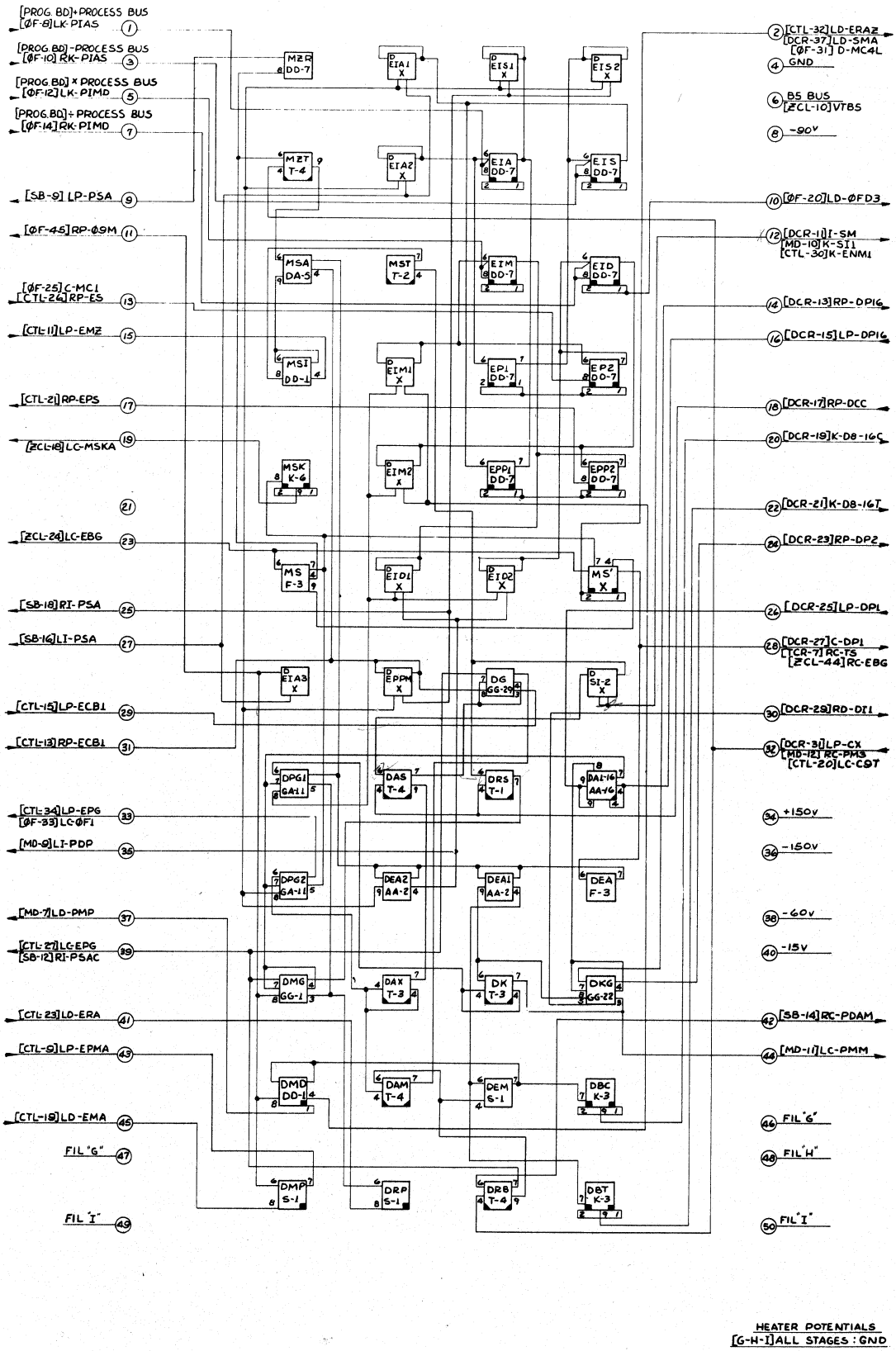
CHECK COUNTER (CCT)

PLATE 75 C



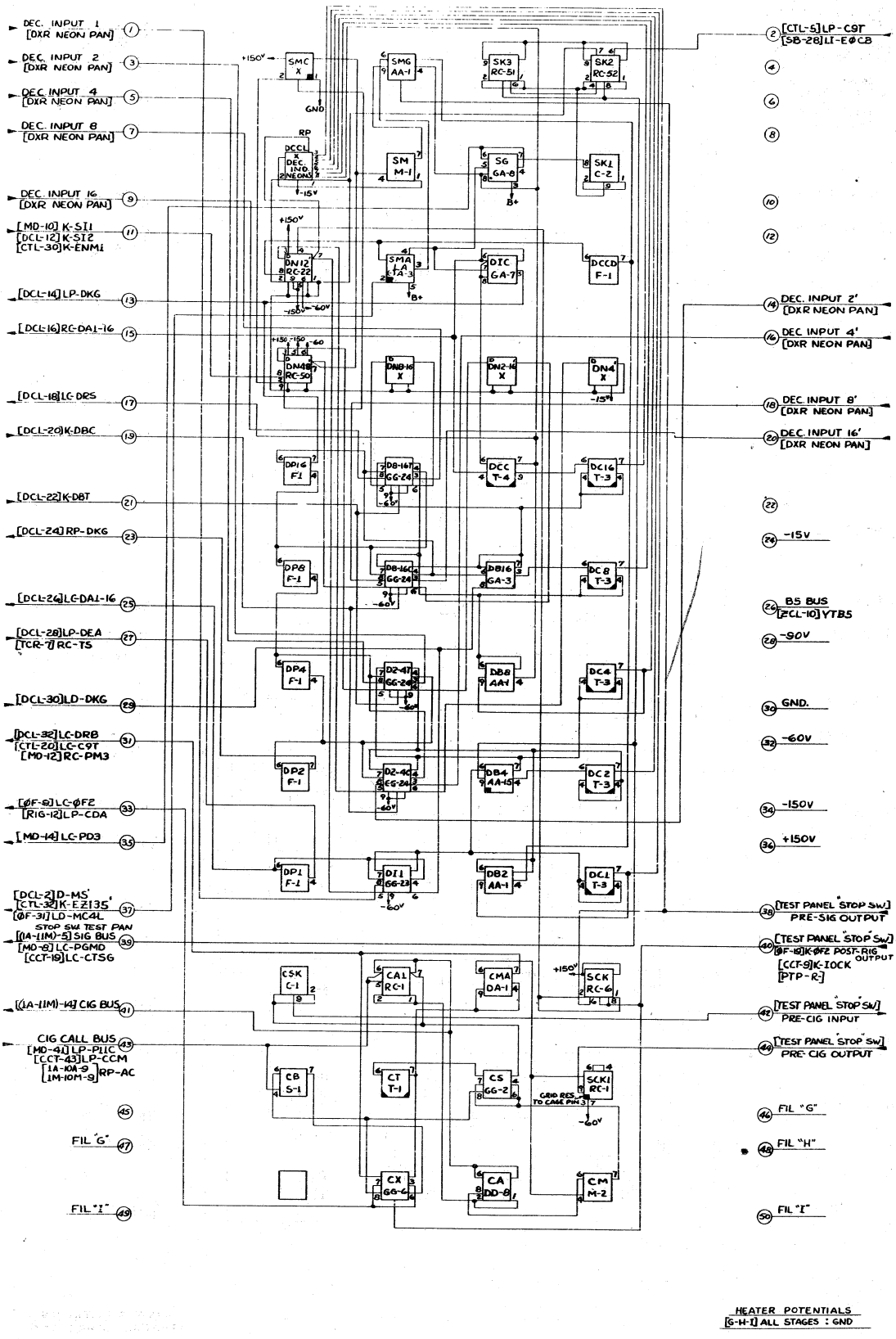
CONTROL (CTL)

PLATE 76C



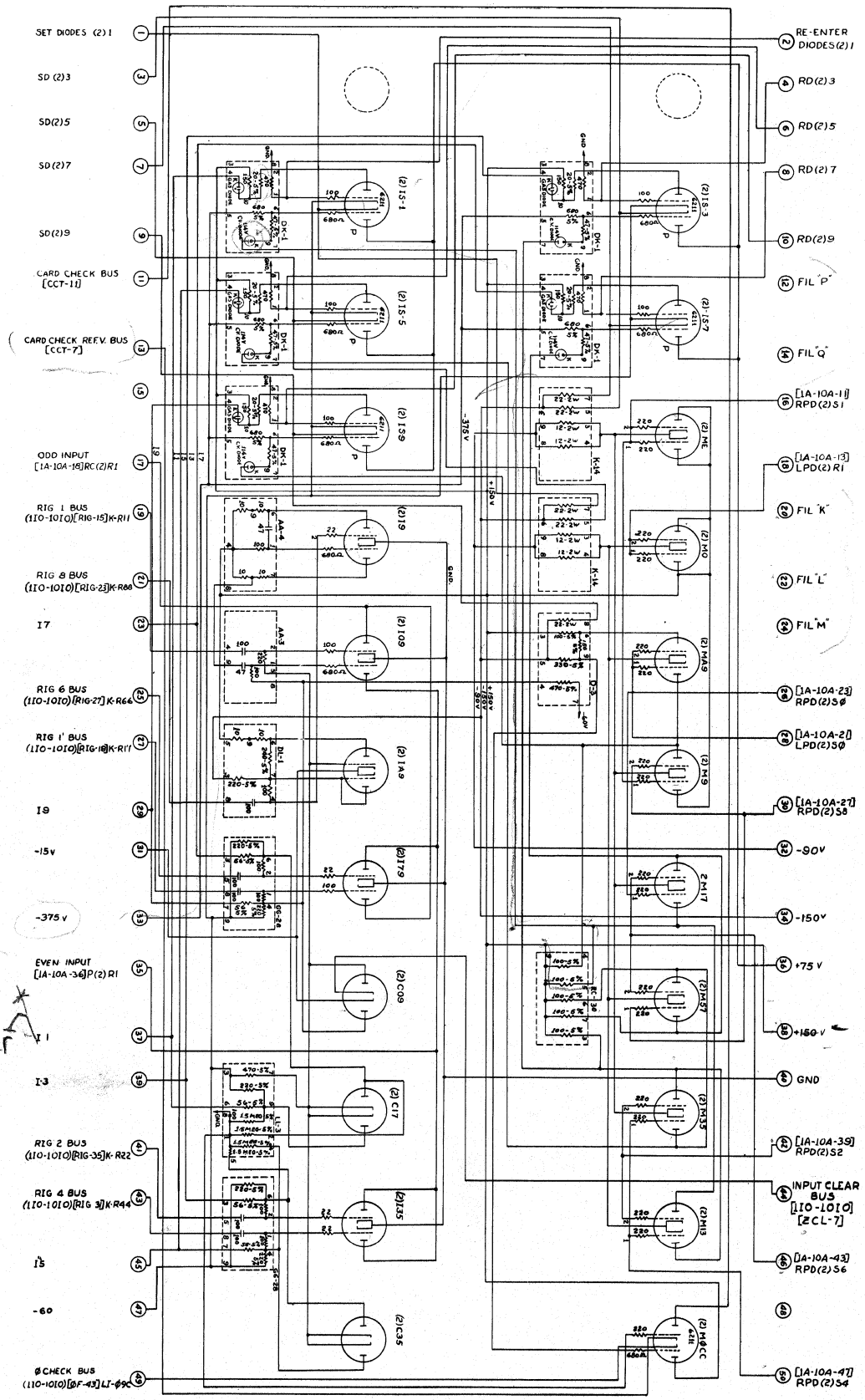
DECIMAL CONTROL (DCL)

PLATE 77 C



DECIMAL COUNTER (DCR)

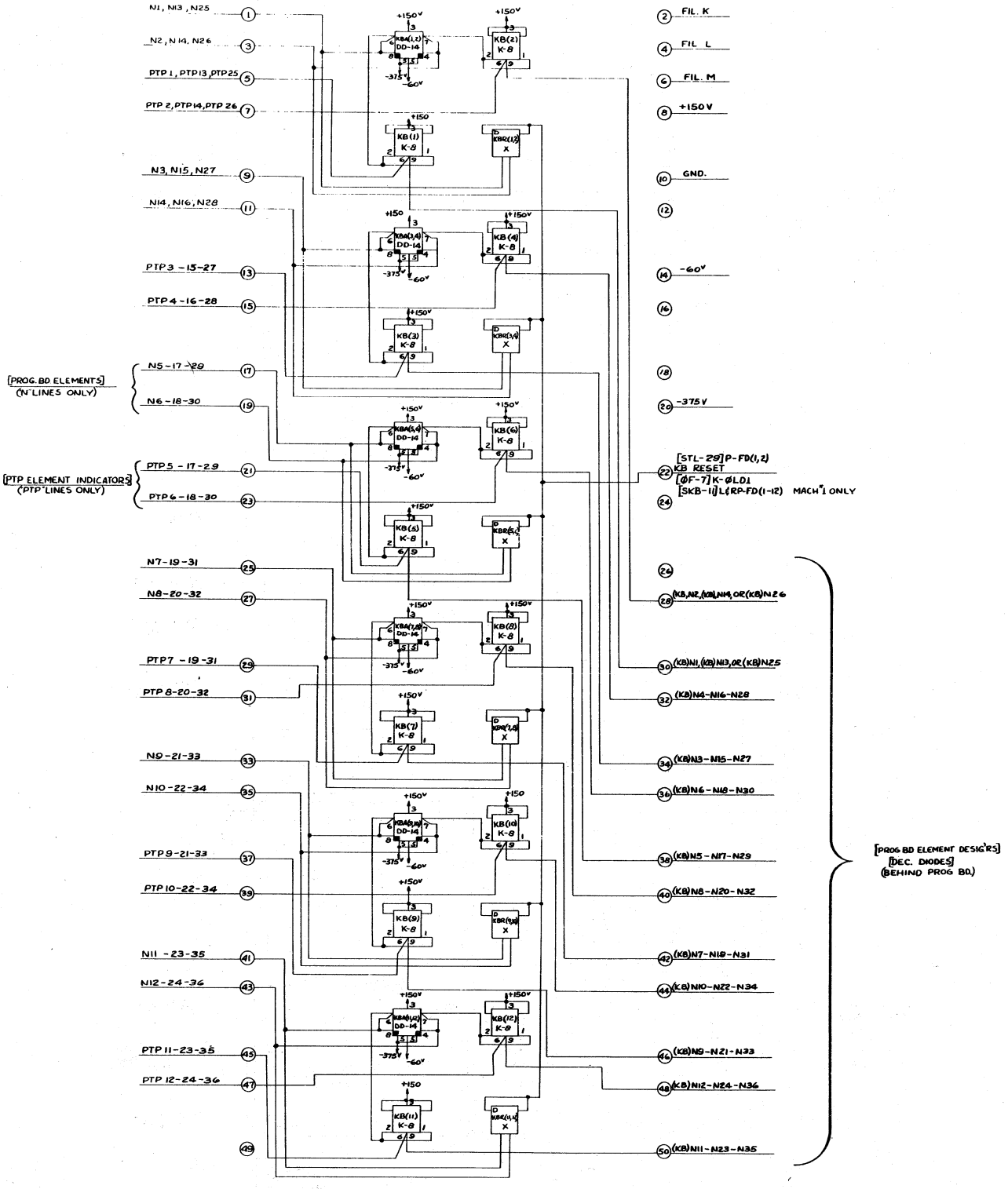
PLATE 78 C



NOTES:
1. RESISTOR VALUES IN K Ω, ½ W ±10% UNLESS OTHERWISE NOTED
2. CAPACITOR " " MMF, " ±10% " " "

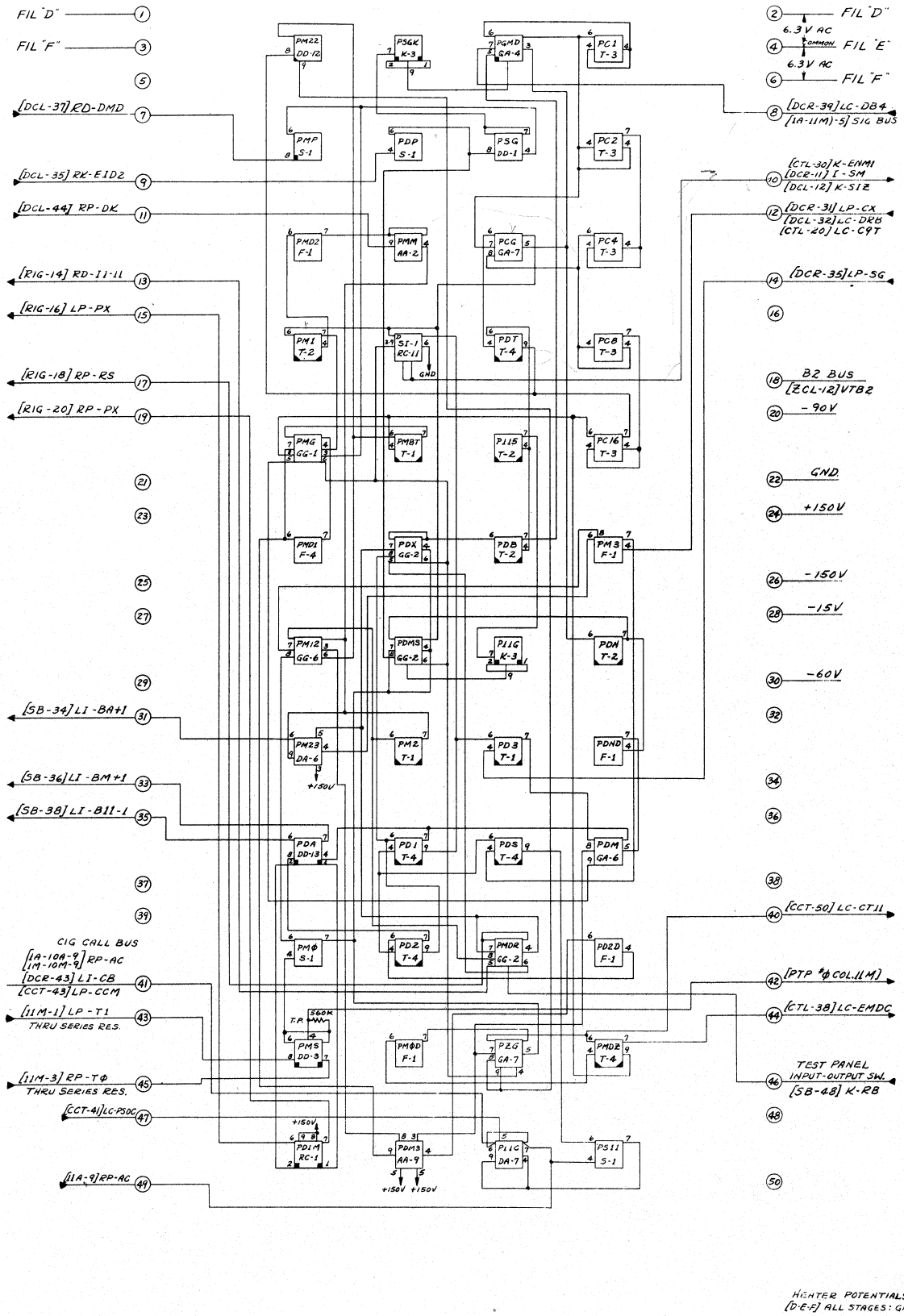
INPUT - OUTPUT (I-O)

PLATE 79 C



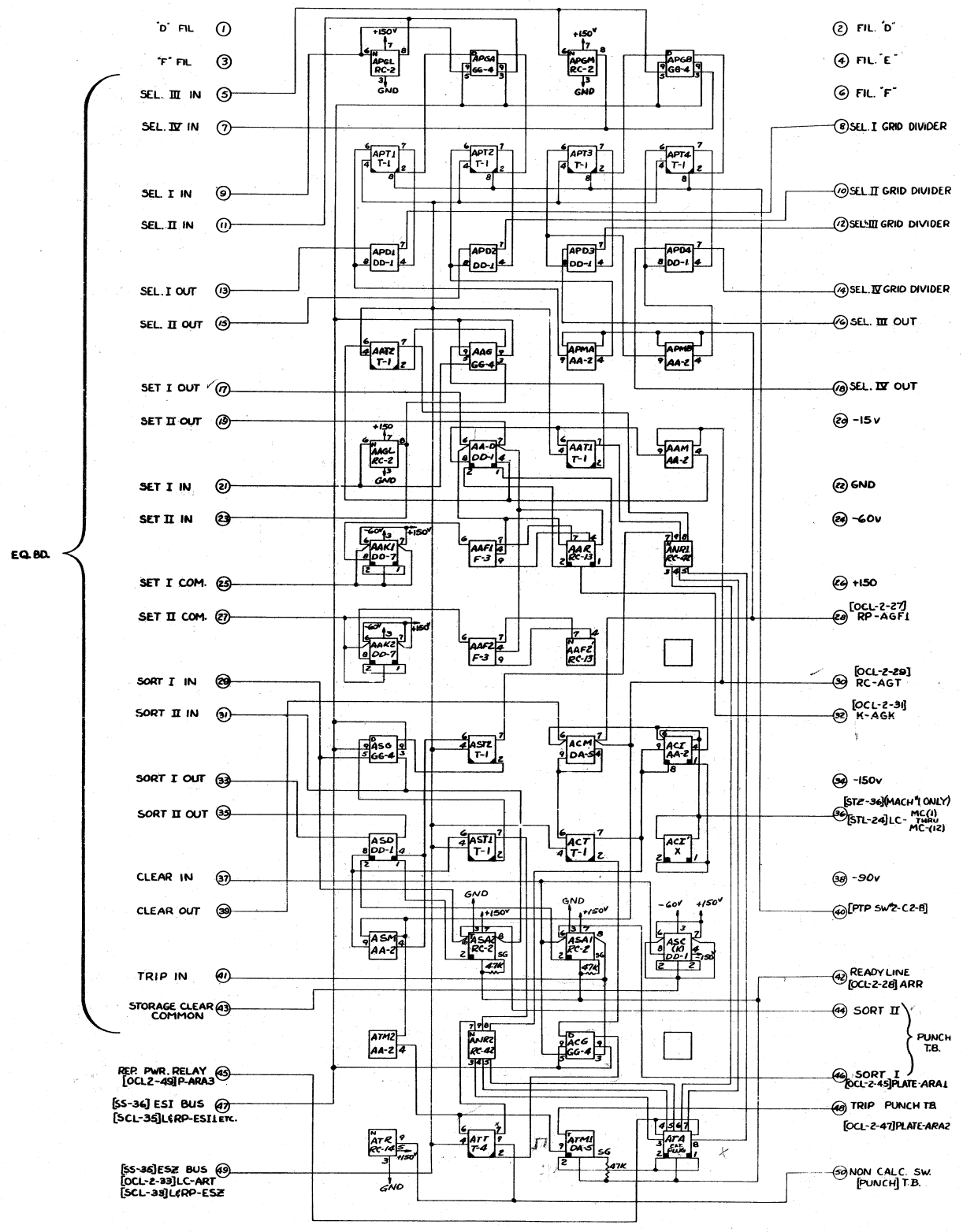
KEYBOARD BIAS (KB)

PLATE 80 C



MULTIPLICATION - DIVISION (M·D)

PLATE 81 C

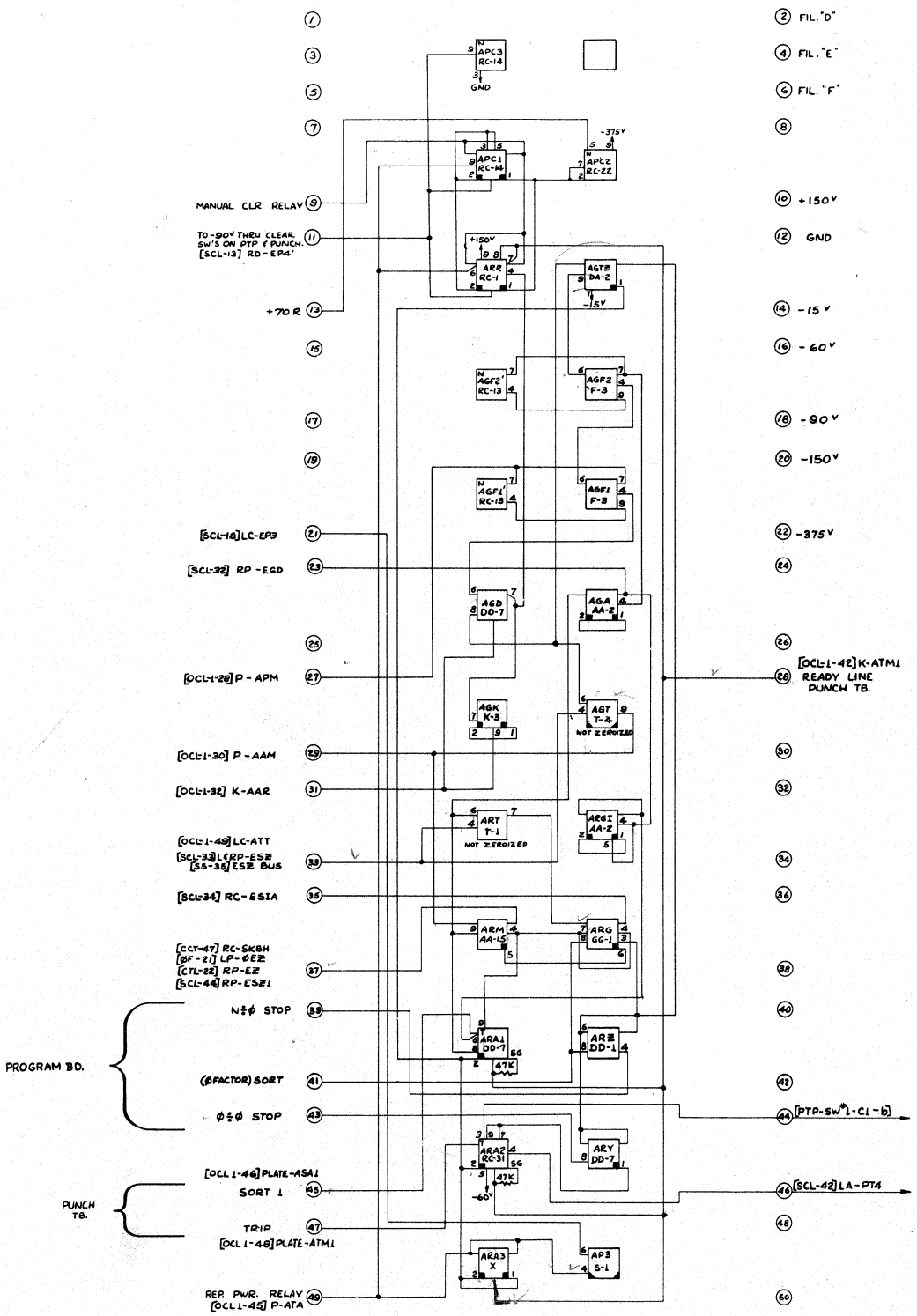


NOTE: ALL TRIGGERS NOT ZEROIZED

HEATER POTENTIALS
[D-E-F] ALL STAGES: GND

OUTPUT CONTROL-1 (OCL-1)

PLATE 82 C

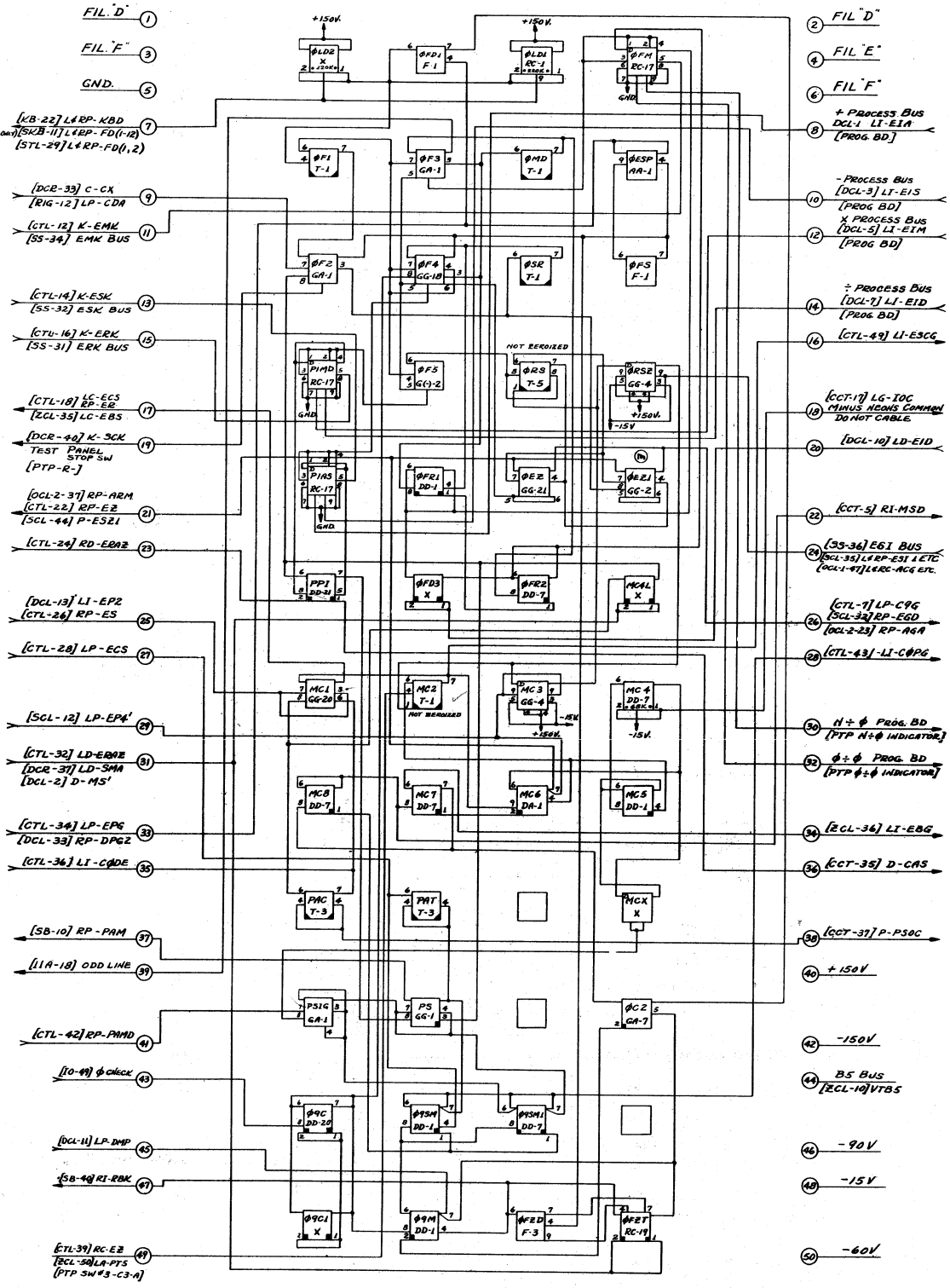


NOTE:- TRIGGERS ART & AGT ARE NOT ZEROIZED

HEATER POTENTIALS
[D-E-F] ALL STAGES : GND

OUTPUT CONTROL-2 (OCL-2)

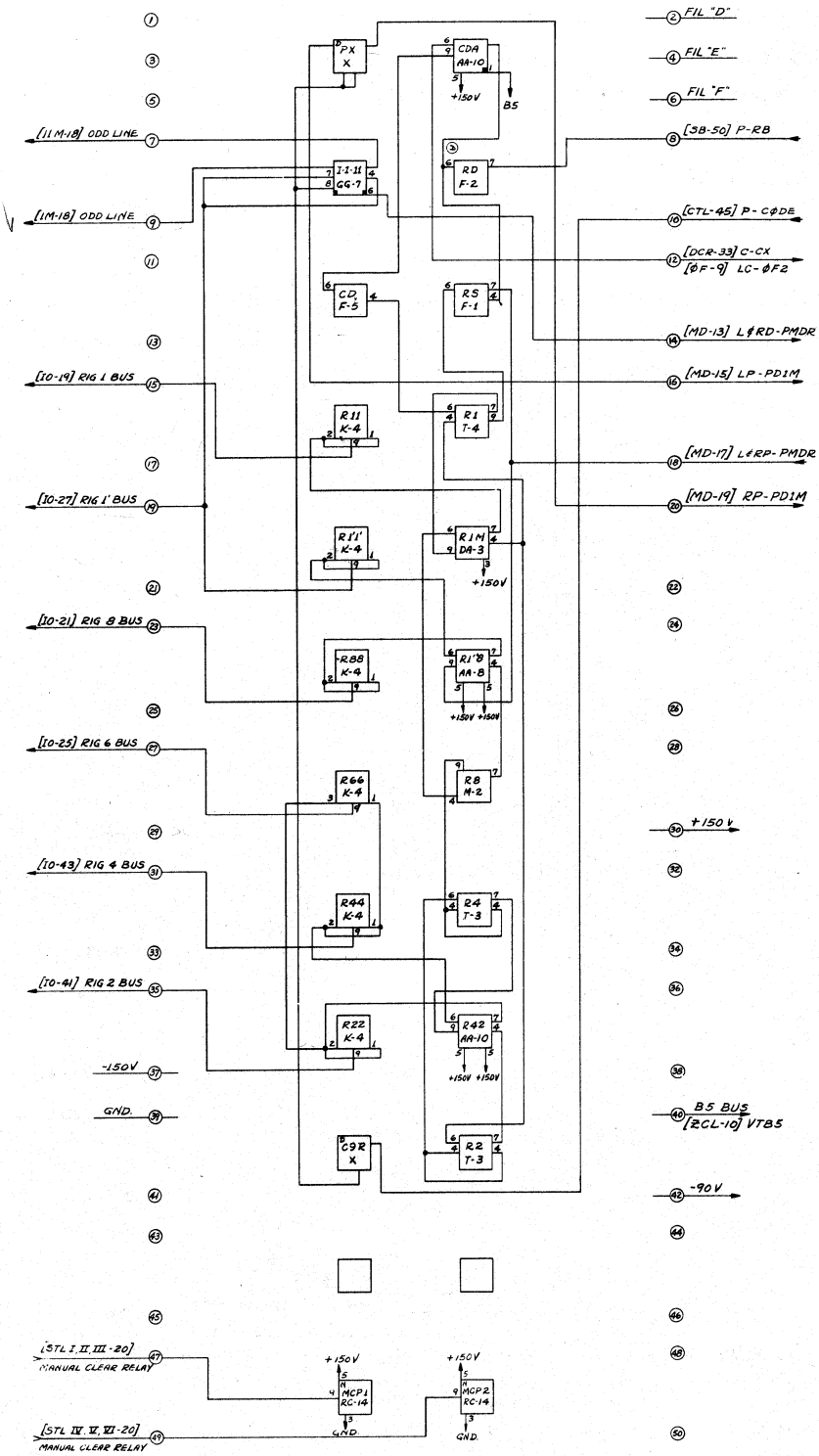
PLATE 83 C



HEATER POTENTIALS
[D-E-F] ALL STAGES GND.

ZERO FACTOR (ØF)

PLATE 84C

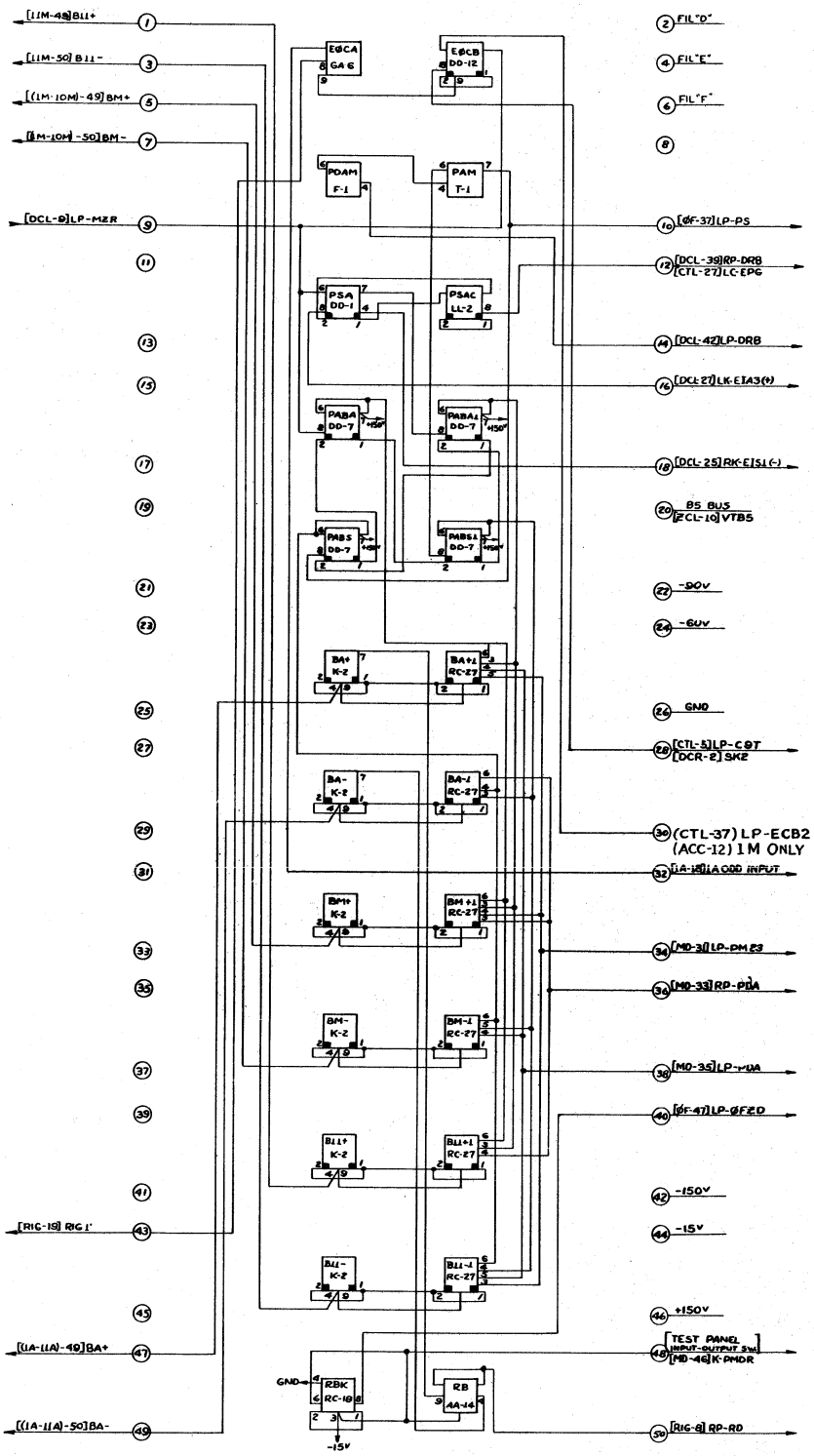


NOTE:
(1) ALL TRIGGERS ZEROIZED BY B5

HEATER POTENTIALS
[D-E-F] ALL STAGES: GND

REGISTRATION INPUT GENERATOR (RIG)

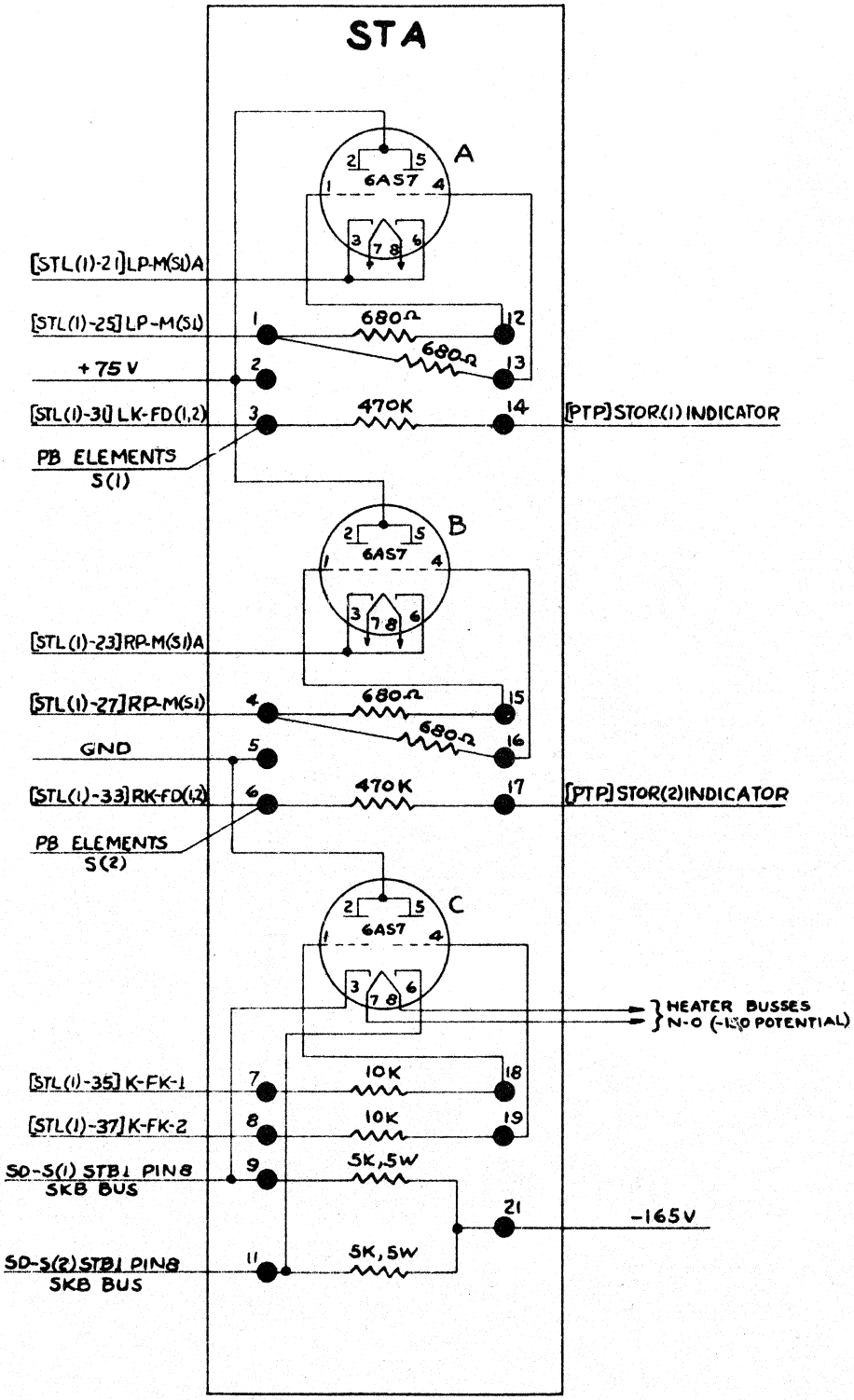
PLATE 85 C



HEATER POTENTIALS
[D-E-F] ALL STAGES : GND.

SIGN BIAS (SB)

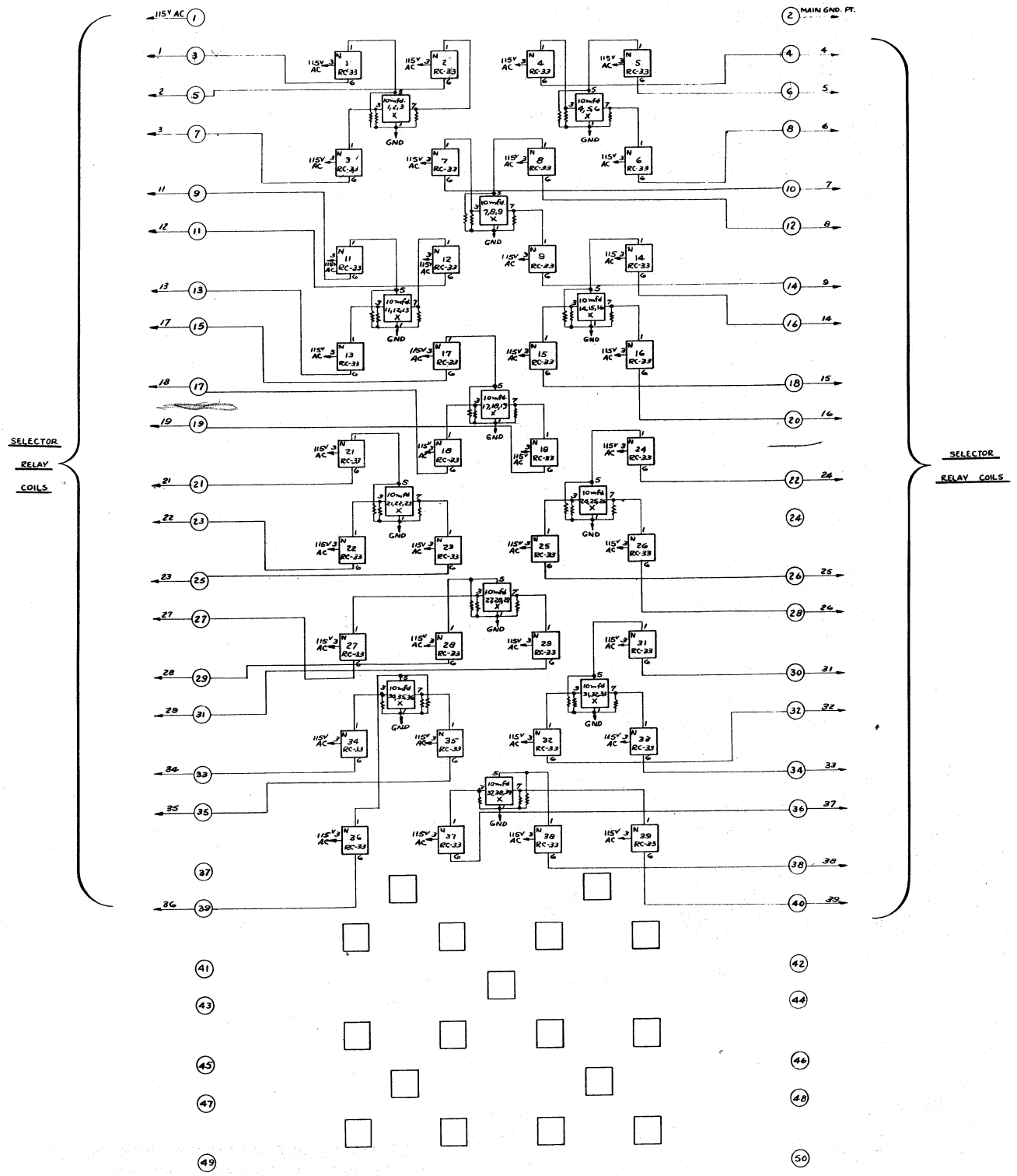
PLATE 86 C



NOTE:
1. RESISTORS ARE ½ W, AND ±10% EXCEPT WHERE NOTED.
2. THIS CHASSIS CONTAINS "MEMORY CLEAR" AND "READ-OUT FOLLOWER" CIRCUITS.

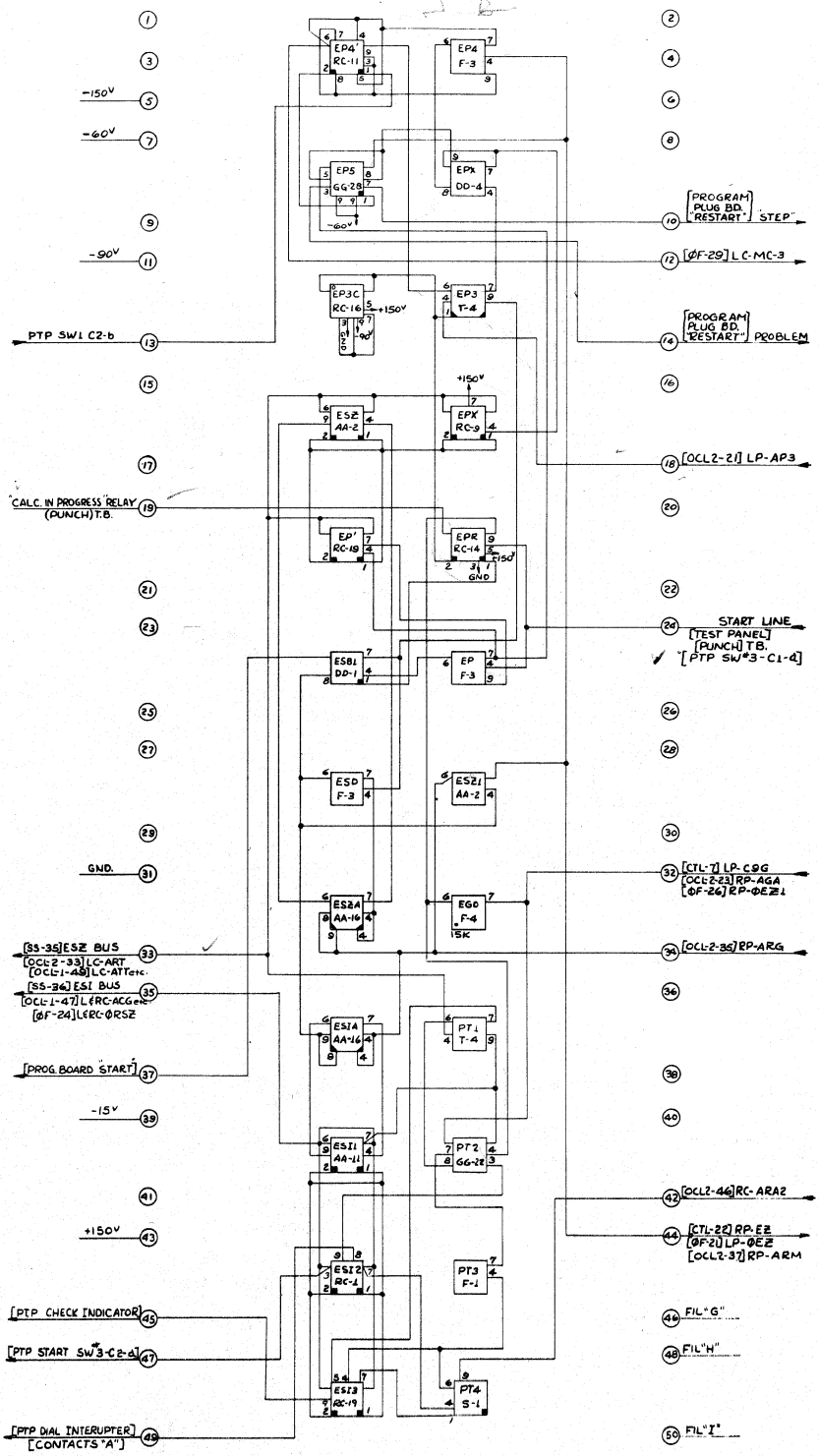
STA	PLATE 87 C

NOTE:
VALUE OF EACH OF THE RESISTORS IN PARALLEL WITH THE 10 MFD CONDENSERS IS 470 K, ½ W, ±10%.



SELECTOR POWER (SEP)

PLATE 88 C

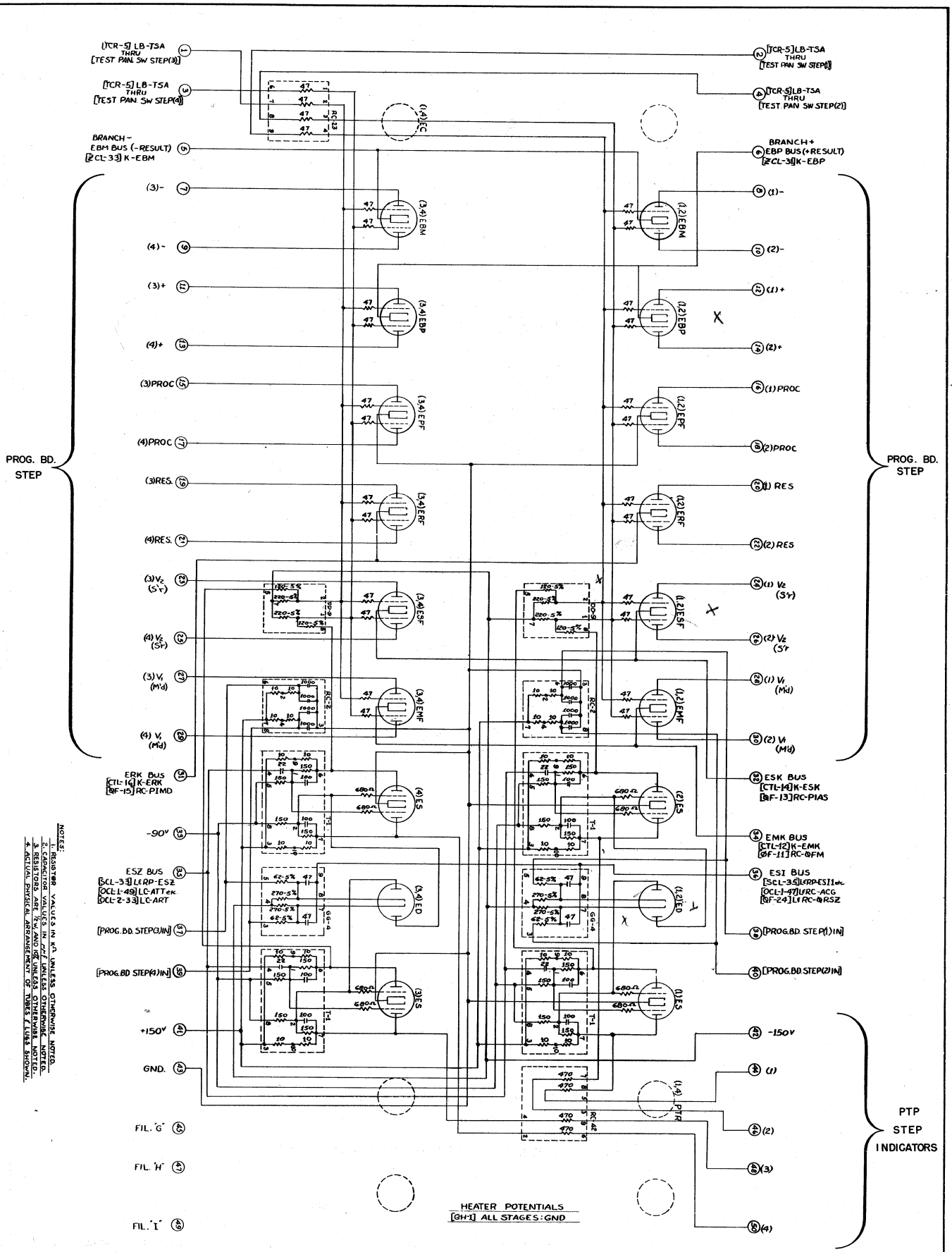


Note ~ TRIGGERS EP3 & PT1 ARE NOT ZEROIZED BY B2 OR B5

HEATER POTENTIALS
[G-H-I] ALL STAGES : GND

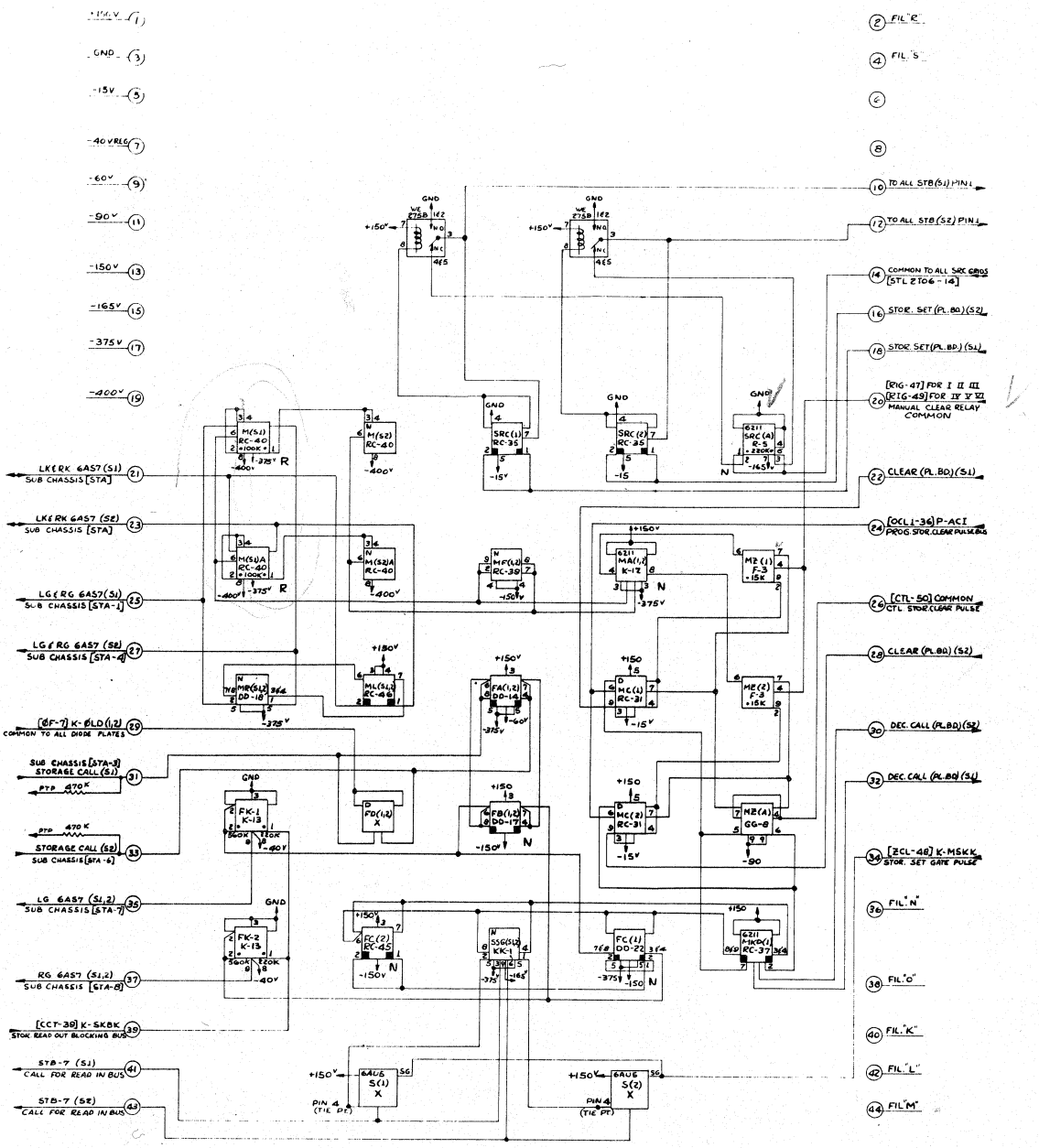
STEP CONTROL (SCL)

PLATE 89 C



STEP SEQUENCE (SS)

PLATE 90 C



HEATER POTENTIALS

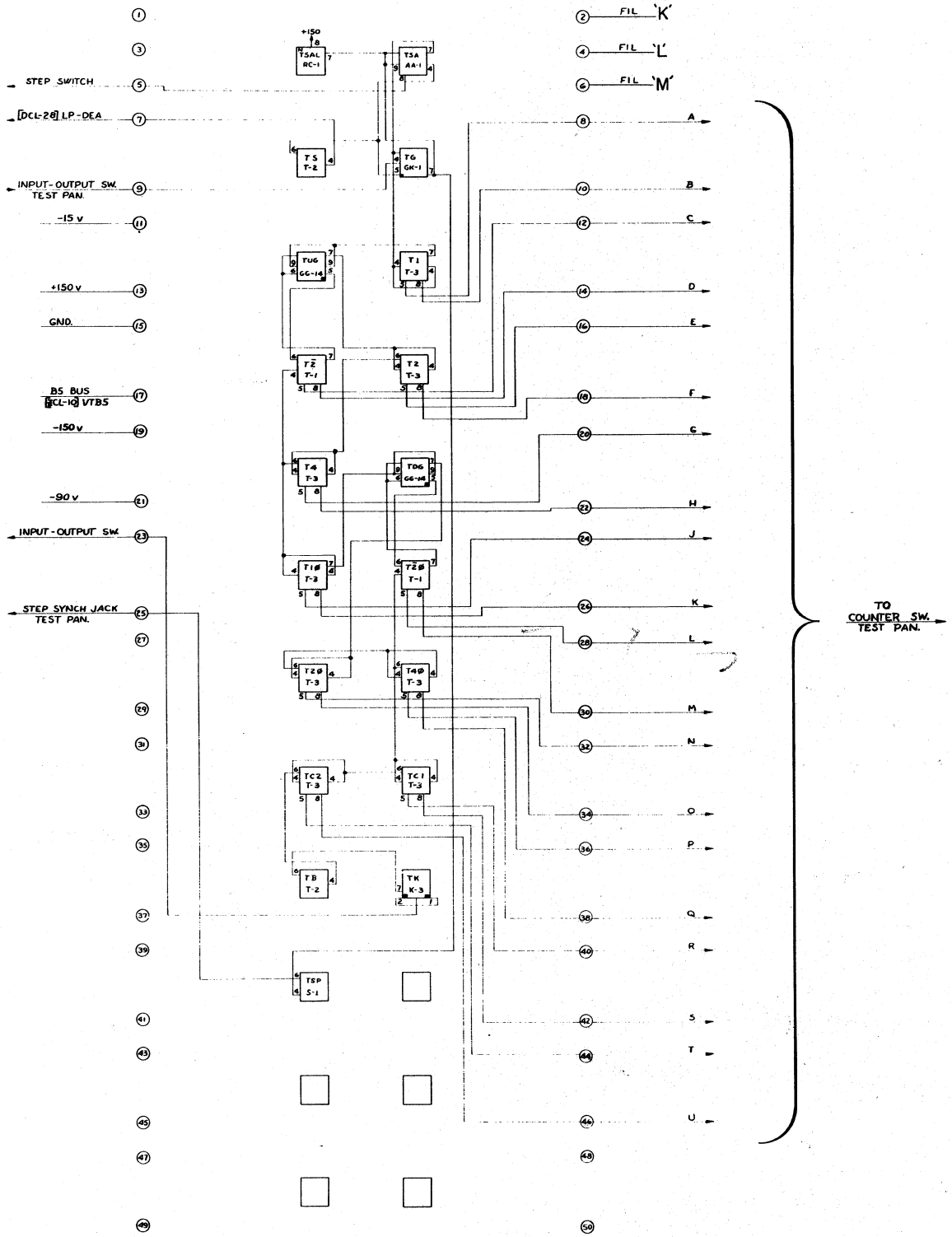
[N-O] STAGES INDICATED BY LTR "N" : -150V

[R-S] " " " " "R" : -375V

[K-L-M] " NOT INDICATED : GND

STORAGE CONTROL (STL)

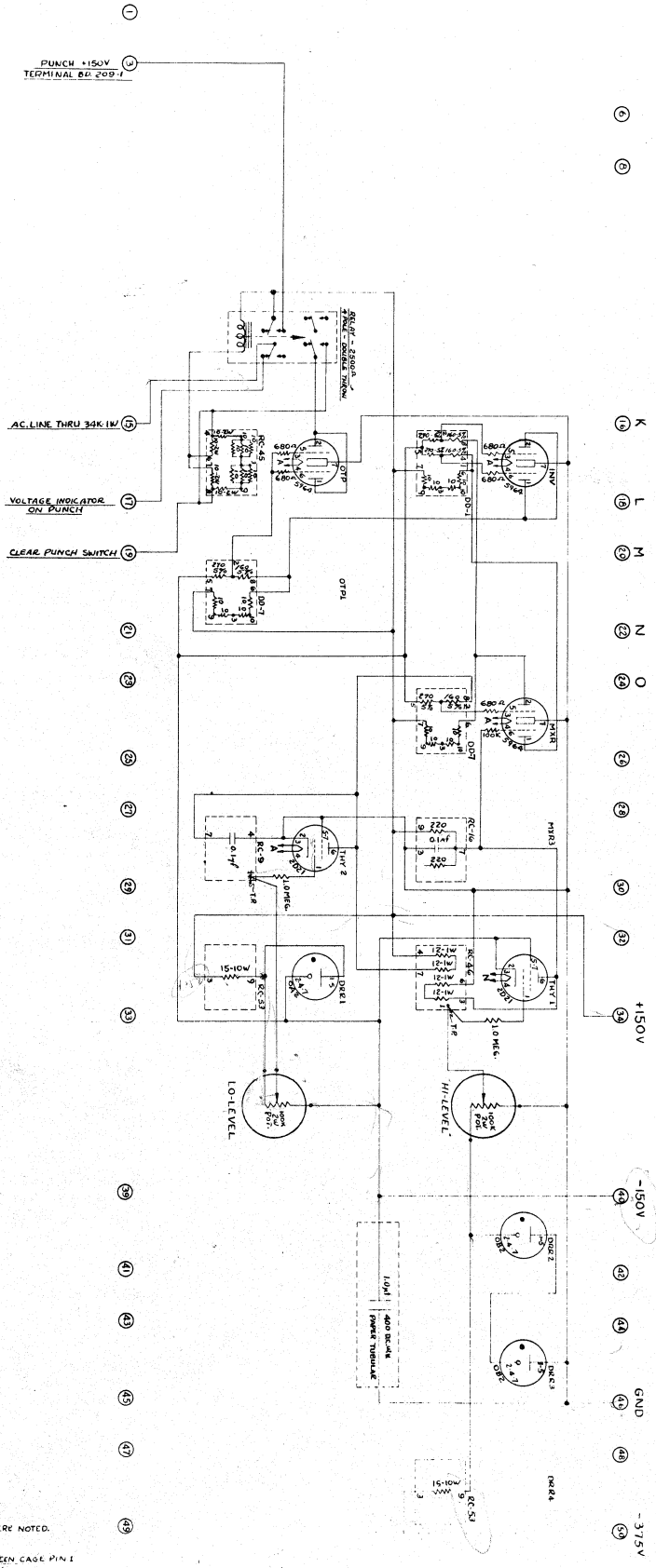
PLATE 91 C



HEATER POTENTIALS
[K-L-M] ALL STAGES : GND

TEST COUNTER (TCR)

PLATE 92 C

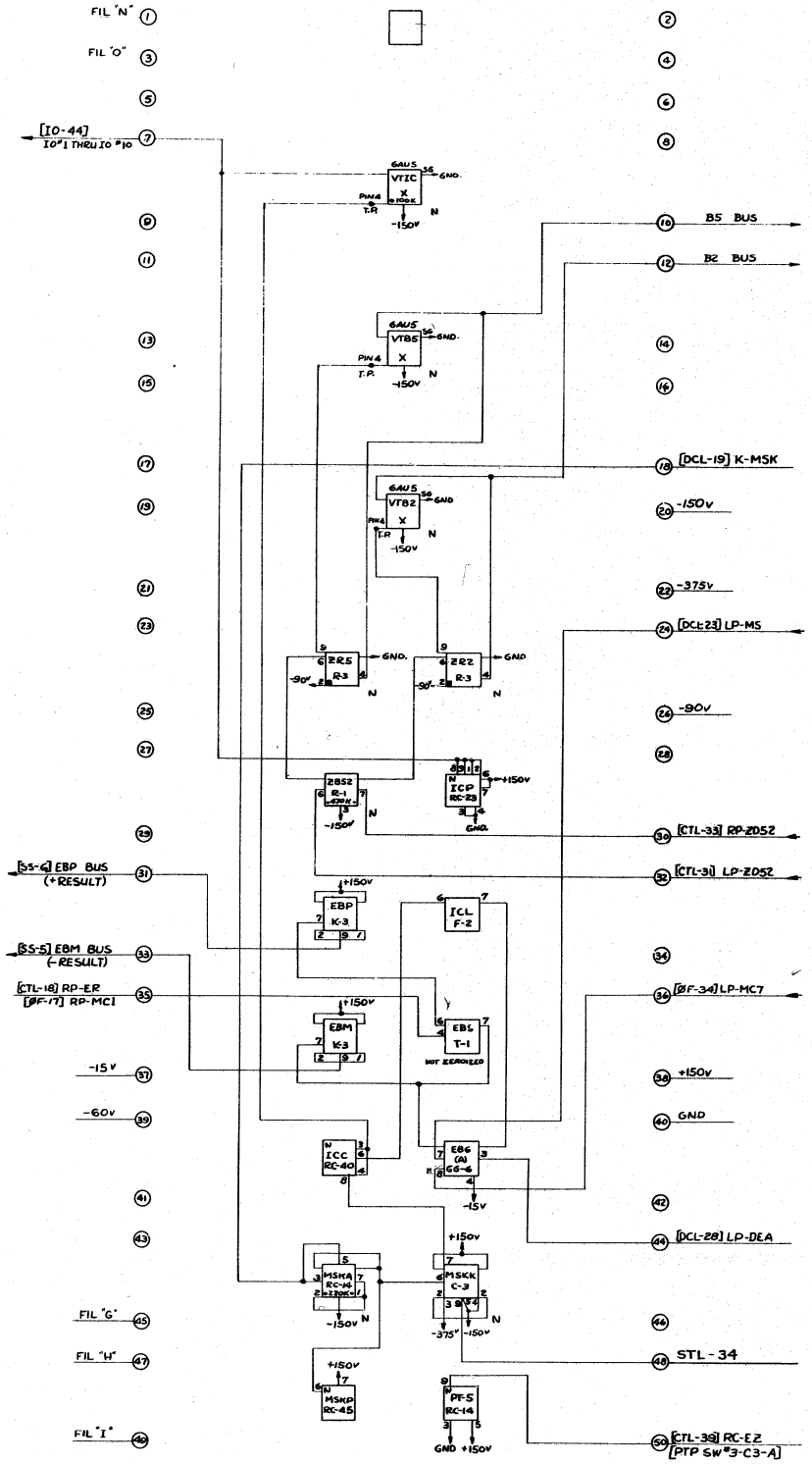


NOTE:

1. RESISTOR VALUES ARE 1/2W AND ±10% EXCEPT WHERE NOTED.
2. 'T.P.' INDICATES TIE POINT.
3. FOR 'HI-LEVEL' ADJUSTMENT CONNECT V.T.V.M. BETWEEN CAGE PIN 1 OF RC-46 CAGE & GND; THEN ADJUST FOR -162V.
4. FOR 'LO-LEVEL' ADJUSTMENT CONNECT V.T.V.M. BETWEEN CAGE PIN 1 OF RC-9 CAGE & GND; THEN ADJUST FOR -12V IF THE -150V IS AT ITS NOMINAL VALUE. IF THE -150V IS NOT NOMINAL ADJUST FOR THE ALGEBRAIC SUM OF IT & +138V.

VOLTAGE ABNORMALITY DETECTOR (VAD)

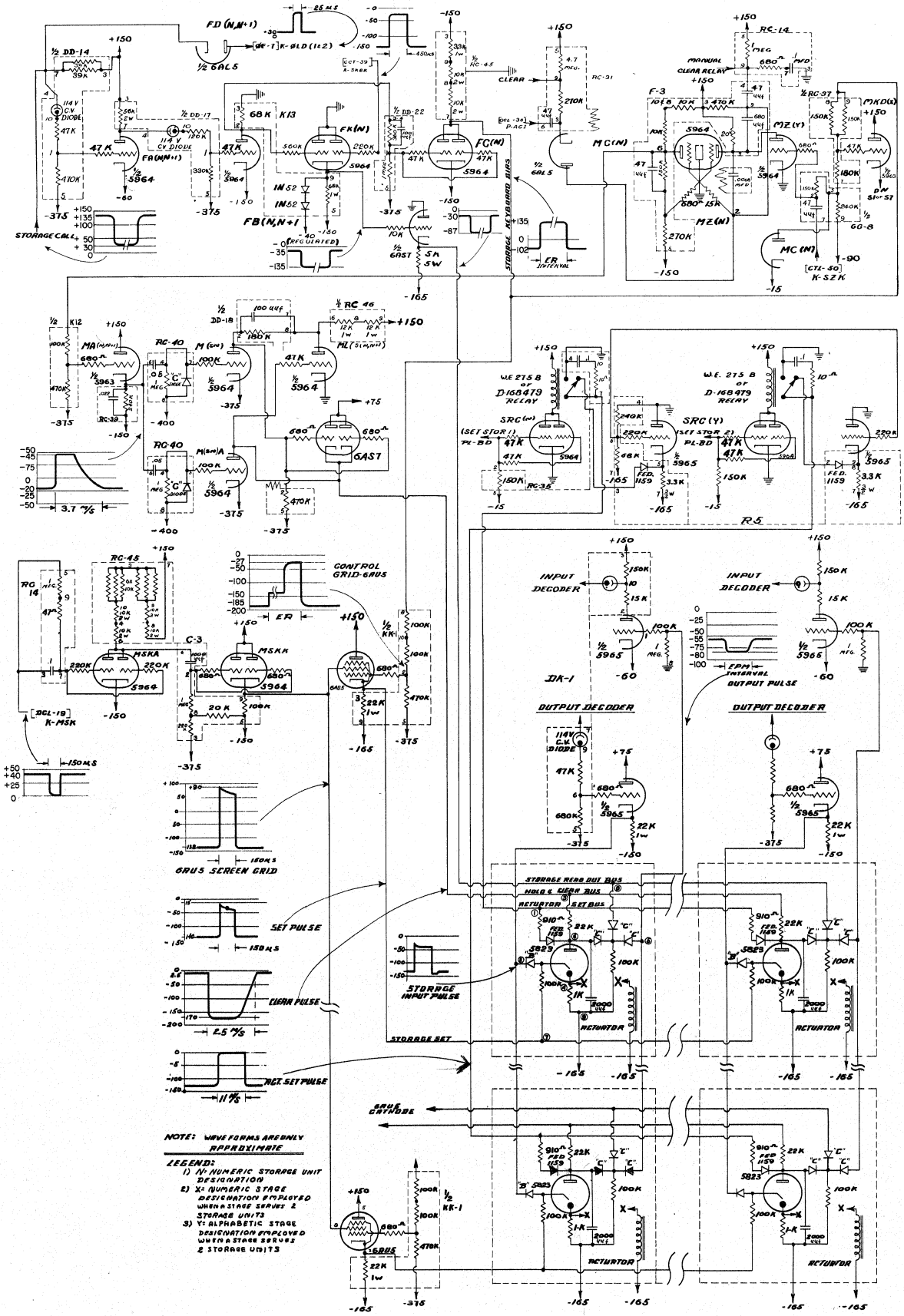
PLATE 93 C



HEATER POTENTIALS
[N-O] STAGES INDICATED BY LTR "N" : -150V
[G"H-I] " NOT INDICATED : GND

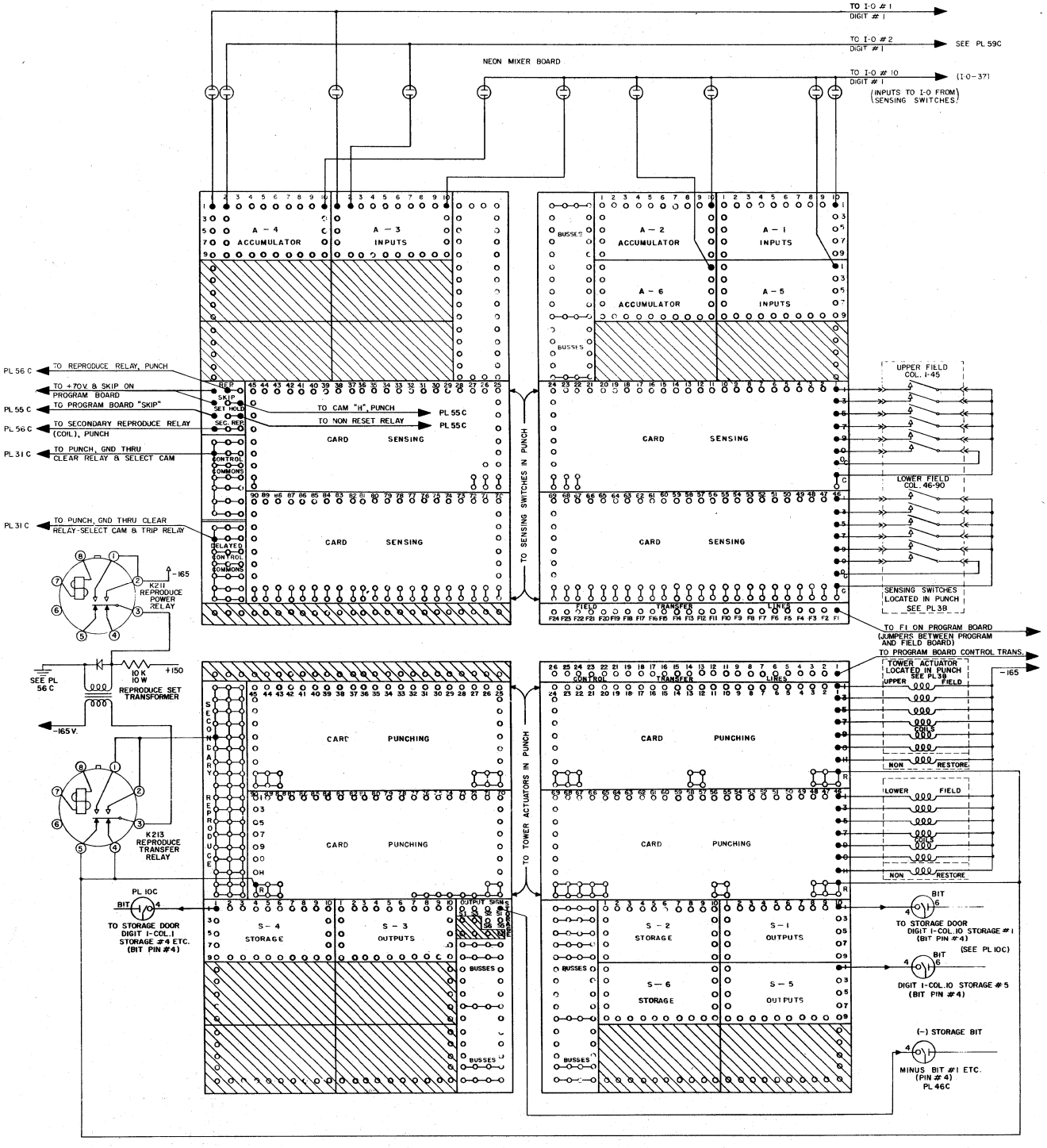
ZEROIZE CONTROL(ZCL)

PLATE 94 C



SCHEMATIC DIAGRAM - STORAGE & CONTROL

PLATE 95 C

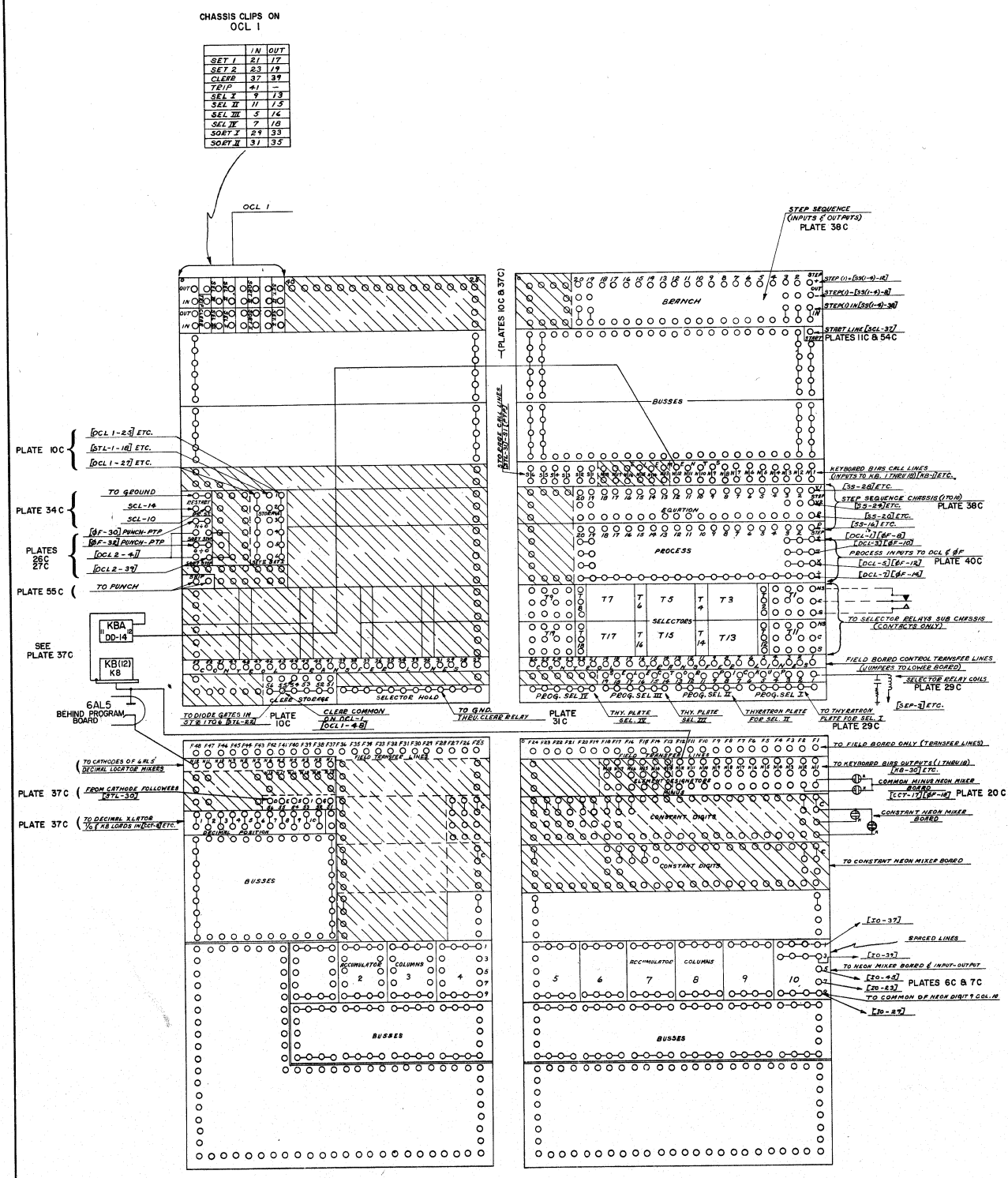


NOTE: CROSS-HATCH AREAS OMITTED FOR MODEL 409-60

REAR VIEW
FIELD BOARD

FIELD BOARD - EXPLANATORY DRAWING

PLATE 96 C



NOTE: CROSS-HATCH AREAS INDICATE SECTIONS NOT USED IN SOME MACHINES.

REAR VIEW
PROGRAM BOARD

PROGRAM BOARD - EXPLANATORY DRAWING

PLATE 97C

ADJUSTMENTS
of the
ELECTRONIC COMPUTER
UNIVAC 60 & 120

SECTION D

Remington Rand
DIVISION OF SPERRY RAND CORPORATION
315 FOURTH AVENUE
NEW YORK, N. Y.

ELECTRONIC COMPUTER
UNIVAC 60 & 120

Section -D-

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Printed In U. S. A.

ADJUSTMENTS

THROAT BLOCK

Fig. 1A

The Throat Knife should have .010 to .020 inch overlap with the Throat Block. Be sure the Throat Block and Throat Knife are parallel.

THROAT KNIFE

Fig. 1A

The Throat Knife is adjusted to obtain .008 inch clearance between the Throat Knife and Throat Block. This clearance is obtained as follows:

1. Loosen set screw on the right side of the Throat Knife Assembly.
2. Turn Throat Knife Adjustment Screw on top of Throat Knife Assembly until .008 inch is obtained.
3. Tighten set screw on side of Throat Knife Assembly.

PICKER KNIFE

Fig. 1B

The Picker Knife is adjusted to obtain a .005 inch bite on the trailing edge of the card.

1. Turn machine until the Card Feed Slide is in full feed position.
2. Through access slots in Card Feed Slide Guard, loosen the 3 Picker Knife set screws.
3. Loosen the 2 Picker Knife Adjustment Screw Lock Nuts.
4. Adjust Picker Knife for .005 inch height by turning the 2 adjustment screws. The heads of the adjustment screws must contact the top of the slot in the Picker Knife. Check for .005 inch height across the width of the Picker Knife.

NOTE: The Picker Knife has two useable edges and can be inverted when one edge becomes worn.

CARD FEED SLIDE

Fig. 1B

This adjustment is obtained with the Card Feed Slide Eccentric which is located under the Card Feed Slide.

1. Position the Card Feed Slide in full restored position.

2. Place a card in the Feed Magazine and position the card so its trailing edge is contacting the rear Card Stacking Guides.

3. Adjust the Card Feed Slide Eccentric to obtain .031 inch Picker Knife overthrow behind trailing edge of the card.

4. Position the Card Feed Slide in full feed position. Place a card in the Feed Magazine to just contact the Feed Rolls. The Picker Knife must overthrow the trailing edge of the card with a minimum of .062 inch to insure a positive feed.

CARD FEED SLIDE SIDE PLAY

Fig. 1C

The Card Feed Slide Side Play is controlled by an adjustable Gib.

1. Loosen 3 set screws under left side of the Feed Magazine. (Magazine removed from machine).

2. Adjust 3 screws on left side of Feed Magazine for a minimum Card Feed Slide Side Play condition.

3. Check for minimum side play with Card Feed Slide in full feed and restored positions.

4. The Card Feed Slide must be free to fall by its own weight when the Feed Magazine is tilted.

5. Secure adjustment by tightening 3 set screws under left side of Feed Magazine.

FEED MAGAZINE ALIGNMENT

Fig. 1

The Feed Magazine is aligned so that cards feeding into the Sensing Section are sensed in the center of the punched hole.

1. Punch a card with alternate 7 and 9 positions punched in the Lower Field.

2. Feed the card into the Sensing Section until the pins in the Lower Sensing Pin Box indicate sensing of the card has begun.

3. Gently tap the non-selected pins of the Lower Sensing Pin Box.

NOTE: Too heavy a blow on the pins could puncture the card and cause a card jam.

4. Remove the card, check the pimpled card for proper alignment.

5. In case the alignment is not correct, the magazine is to be moved in a direction determined by the hole nearest the pimpled mark. For example: if the pimpled mark is nearest the hole on its left, move the Feed Magazine to the

left. The Feed Magazine is moved, after loosening the 4 Magazine Mounting Screws, by adjusting the screw and lock nut which extends through the base casting to the left of the Feed Magazine.

DUMMY CAM

Fig. 2A

1. No cards in the machine.
2. Lower Sensing Pin Box bottom dead center.
3. Holding the Pin Lock Mechanism unlatched, cycle the machine manually until the first sign of pin movement in the Upper Sensing Pin Box is observed; CAUTION: All Sensing Pins are in a locked position.
4. Gently tap the pins in the Lower Sensing Pin Box while backing off the Machine until all movement just disappears from the pins in the Upper Sensing Pin Box.
5. Adjust height of Dummy Cam to leave .001 inch clearance between cam surface and Follower Roll. NOTE: Manually latch the Pin Lock Mechanism to prevent locking all 540 Upper Set Up Pins.

PIN LOCK TORSION SPRINGS

Fig. 2A

The Pin Lock Torsion Springs are adjusted with approximately 1½ turns for tension. Be sure spring is free.

PIN LOCK ECCENTRIC

1. Lower Sensing Pin Box at bottom dead center.
2. Adjust Pin Lock Eccentric to obtain a minimum passing clearance with the Pin Lock Mechanism Locking Extension, as shown in 2B.
3. The Lower Sensing Pins should remain free, unlatched, when the Lower Pin Box is raised and no card is sensed, as shown in 2C.

SENSING SWITCH BOX

Fig. 3C

A selected Upper Sensing Pin must just contact its corresponding Sensing Switch Box Intermediate Sensing Pin at 301°. This timing is obtained by shimming the Sensing Switch Box using Laminated Shims #1100101 & #1100102.

1. Feed a card with "0" positions punched Upper Field columns 1 through 45 and "9" positions punched Lower Field columns 46 through 90, manually into the machine.

2. Observe when the selected Upper Sensing Pins just contact their corresponding Sensing Switch Box Intermediate Sensing Pins. The machine timing dial must read 301°

3. To obtain condition described in Paragraph 2 above, raise or lower the Sensing Switch Box by removing or inserting shims under the Switch Box Mounting Rails.

   NOTE: Check all 4 corners of the Sensing Switch Box, Columns 1, 45, 46 and 90.

TOWER RETRACT BAIL AND ECCENTRIC

Fig. 3

1. Machine on low part of Tower Retract Cam.

2. Adjust clamp on Retract Bail Shaft so bail just contacts all Actuator Retract Links, as shown in 3A.

3. Adjust Tower Retract Link Eccentric to give approximately .030 inch overthrow on Non-Reset Latch as shown in 3B.

4. Turn machine to high part of Retract Cam as shown in Figure 4. Check to see that the Actuator Interposer Assembly does not limit motion of the Actuator Retract Links as shown in 4A. If limit occurs, increase the gap on the Non-Reset Latch.

5. Check to be sure the Interposer Assembly relatches with overthrow.

NON-RESTORE BAIL

Fig. 4

1. Manually release several Non-Restore Actuator Interposer Assemblies.

2. With Reset Solenoids normal adjust Non-Restore Bail Clamp for .030 inch clearance above Non-Restore Actuator Interposer Assembly as shown in 4B.

3. Check that the Non-Restore Actuator Interposer Assembly does not limit when Reset Solenoid is fully operative.

SET BAR RETRACT ECCENTRIC

Fig. 5A

1. Turn machine to the high part of the Set Bar Section Retract Cam.

2. Adjust Eccentric to Retract the Lock Slides in the Set Bar Section within .005 inch of a limit.

SKIP INTERPOSER ECCENTRIC

Fig. 5B

1. Hold the Skip Interposer in an operative condition while the machine is on the high part of the Set Bar Section Retract Cam.

2. Adjust Eccentric on Skip Interposer so there is .005 inch clearance between Stud and Skip Interposer.

DIE SECTION CARD STOP

Fig. 5C

1. Turn machine to the high part of the Die Section Card Stop Cam.

2. Position and secure the 2 Card Stop Operating Arms on the Card Stop Operating Shaft to open the Card Stops .025 inch below the Punching Chamber.

3. Check to be sure Card Stops close evenly when turning machine to low part of Die Section Card Stop Cam.

FRONT CARD RECEIVER SHUTTER FINGERS

Fig. 6A & 6B

1. Hold Shutter Finger Shaft in a fully operated position.

2. Tip of Shutter Fingers should be set .750 inch above plane of card travel.

3. Set Limit Eccentric so that Shutter Fingers close slightly below plane of card travel

SORT MICRO SWITCH

Fig. 6

The Micro Switch should be fully operated when the Front Receiver Shutter Fingers are fully opened.

CARD JAM MICRO SWITCH

Fig. 6

A card under either Card Jam Micro Switch Plunger, when the Set Bar Section is at its low limit, should fully operate the Micro Switch.

FULL CHIP PAN MICRO SWITCH

3/4 Full Chip Pan should fully operate Full Chip Pan Micro Switch. (Switch is

located under Chip Pan).

FULL RECEIVER MICRO SWITCH

Full Receiver should fully operate Receiver Micro Switches. (Switch located under Card Receivers).

CAM CONTACTS

Fig. 7A

Adjust Cam Contacts for .025 inch clearance when on the low part of the Phenolic Cams.

PHENOLIC CAMS

Fig. 7

There are 14 Phenolic Cams with 7 cams on the Front Main Shaft and 7 cams on the Rear Main Shaft. The cams are not keyed but held in place by pressure exerted by the Phenolic Cam Adjustment Nut. Any of the 7 cams on the Shaft may be adjusted by loosening the Phenolic Cam Adjustment Nut and turning the Phenolic Cams by hand. The Timing Adjustments for the 14 cams are as follows:

CAM	NAME	MAKE		BREAK
A	Calc. Start	334°		30°
B	Select	324°		200°
C	Ready	134°		280°
D	Reproduce Set	89°		280°
E	Reproduce Clear and Sort Storage	334°		70°
F	Sort Pocket	139°		235°
G	Count	350°		46°
H	Skip Pulse	140°		196°
I	Skip Cycle	287°		73°
J	Skip Reset	133°		94°
K	Relay Reset	75°		131°
L	Trip Reset	114°		75°
M	Clutch Start	290°		116°
N	Clutch Stop	28°	APPROX.	214°

Cam N is adjusted to stop the Punch between 268° and 275°

SHAFTS, GEAR TRAINS AND TIMING

Fig. 7

The Clutch controls the cycling of the Punch. The shaft coupled to the Clutch is called the Line Shaft. All mechanical motion of the Punch is driven from the Line Shaft. There are two basic shafts which are called Front and Rear Main Shafts. All Punch Timing is based on the Front Main Shaft. The Rear Main Shaft Dial reads 180°

when the Front Main Shaft Dial reads 0°. The Front Main Shaft controls the Feed Magazine Feed, Lower Sensing Pin Box vertical motion, Upper Sensing Pin Box Card Stop and Retract and Tower Retraction. The Rear Main Shaft controls the Tower Rod and Set Bar Section vertical motion, Set Bar Section Retract, Stripper Plate Motion and Punching Chamber Card Stop.

The Feed Rolls, Intermediate Feed Rolls and Eject Rolls are driven directly from the Line Shaft. There is no timing involved in their operation.

CLUTCH AND BRAKE ASSEMBLY

Fig. 7

The following procedure must be used when installing a Clutch and Brake Assembly:

1. Loosen the Clutch Field Housing Mounting Screws so that the Clutch Field Housing moves freely.
2. Remove Male Coupling.
3. Mount the Assembly in the base.
4. Attach Male Coupling and Female Coupling and position assembly with .025 inch clearance between Coupling and Drive Coupling. This clearance is obtained by use of shims between Casting and Clutch Mounting Bracket.
5. Three .008 inch Shims should be equally spaced about the Clutch Field Housing.
6. The Clutch Field Housing Mounting Screws should be tightened and the .008 inch Shims removed.

SINGLE AND THREE PHASE CONNECTIONS

Fig. 8

1. Single and Three Phase Connections are as shown in Figure 8A. Section A of the Manual shows 5 systems but they must be either Single or Three Phase.

BELT TENSION AND MACHINE SPEED

Fig. 8

1. Belt Tension is obtained through adjustment of the Motor Hanger Bolt.
2. Machine Speed of either 150 CPM or 125 CPM is obtained by the proper Flywheel and Pulley.

NO CARD SENSING PLUNGER

1. No cards in machine.

2. Turn machine until Lower Sensing Pin Box is top dead center.

3. Adjust No Card Sensing Operating Arm to fully operate Micro Switch. (Switch is located on left side of Base Casting).

4. Adjust Limit Arm to rest against Upper Pin Box Casting. This Limit Arm prevents Plunger from positioning itself out of its Guide Hole in the Card Chamber.

BRAKE POTENTIOMETER

Adjust Potentiometer to operate Brake sufficiently to stop the Punch. One second should be sufficient.

FEED AND EJECT ROLL TENSION

Adjust Tension Springs on both sides of roll for an even and heavy pull on the card.

EMPTY FEED MAGAZINE MICRO SWITCH

Adjust the Micro Switch to fully operate when cards and Card Weight are placed in the Feed Magazine.

OUTPUT VOLTAGE ADJUSTMENT

Fig. 9

The Transformer Primary Windings for both filament and D. C. supplies have an auxiliary winding which permits closer adjustment of the output voltage on the secondary side. All Transformer Primaries are numbered similarly, therefore, any Transformer Adjustment, filament or D. C. can be made according to the sketch.

1. The line voltage should first be measured and then the Transformer Primaries may be connected using Figure 9 as a guide. Some corrections may be necessary to offset Transformer variations.

2. When it is not necessary to use Terminals #5 or #6, leave one end of the Jumper Wire connected to Tap #5 and #6 and the other to a Tap not being used for the line. CAUTION: Never connect the Jumper Wire from Terminal #5 to #6.

3. The filament voltages should be 6.3 volts $\pm$ .2 volts at the chassis male contacts or at the socket of the Rectifier or Thyratron Tube requiring a 6.3 volt filament supply. The Rectifier Tubes requiring a 2.5 volt filament supply should have 2.5 volts $\pm$ .01 volts at their socket.

4. No adjustment should be attempted without the use of a low scale A.C. meter of 2% accuracy or better since the usual accuracy of the field service meters is not better than 5%.

   The D.C. voltages should be adjusted within 2% except -60 V.D.C. which is allowed 10%.

-165 SURGE LIMIT CONTROL

Fig. 10

The control circuit mounted at the top of the -165 V. Capacitor Assembly is for the purpose of eliminating overloads which would otherwise be present on the EL3C Rectifier Tube, when the filter capacitor bank charges.

At the instant T-22 becomes energized, charging current flows to capacitor C203, through Resistors R201, R202 and R203. These Resistors limit the current flow to a safe value for the tube.

As the -165 V. line on the output of F219 increases its voltage in a negative direction, R207 passes current to C201, charging same. As the charge reaches the voltage required to operate K209, the relay closes, and shorts out R203. At this time, an increase current flows through R201 and R202, charging the capacitor C203 further.

The closing of K209 also starts a new charging time interval when contacts 7 and 8 close. This permits C202 to be charged through R208. K210 then operates. Contacts 3 and 5 (paralleled) and 4 and 6 (paralleled) then short out R201 and R202, allowing full current charge of capacitor bank C203.

K208 is used to discharge C201 and C202 through R204 and R205 so that full charging time is available in the following charging cycle, should it follow immediately.

These circuits are checked as follows:

1. All relay contacts should be clean and have proper wiping action. They must make very good contact.

2. Resistors R201, R202, R203, R207 and R208 should be checked.

3. Timing of K209 and K210 should be checked, and if found to be short, C201 and C202 should be changed. K209 should pull in approximately .2 seconds after T-22 is energized. K210 should pull in .9 seconds after K209 closes.

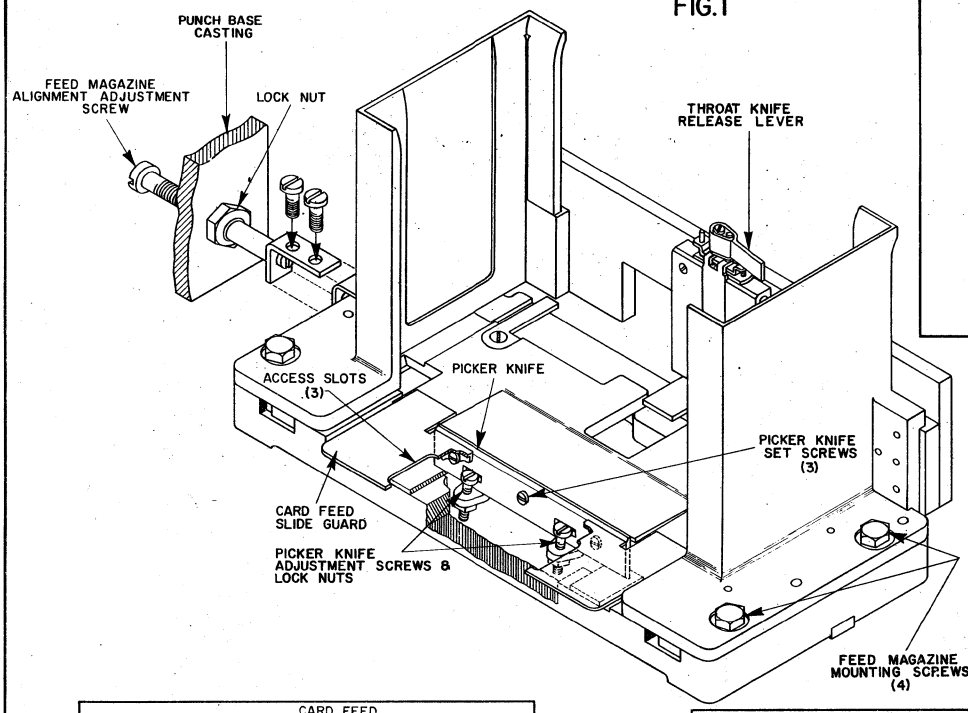


FIG. 1

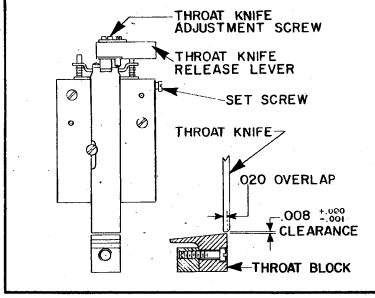


FIG. 1A

FEED MAGAZINE ADJUSTMENTS

FIG. 1

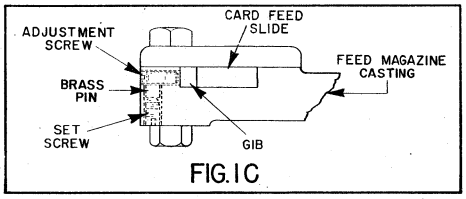
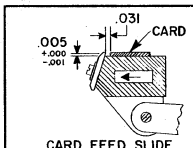


FIG. 1C



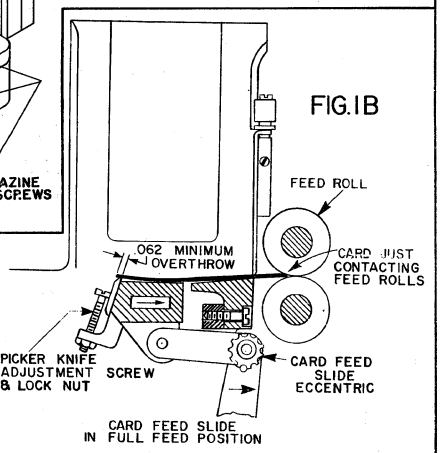
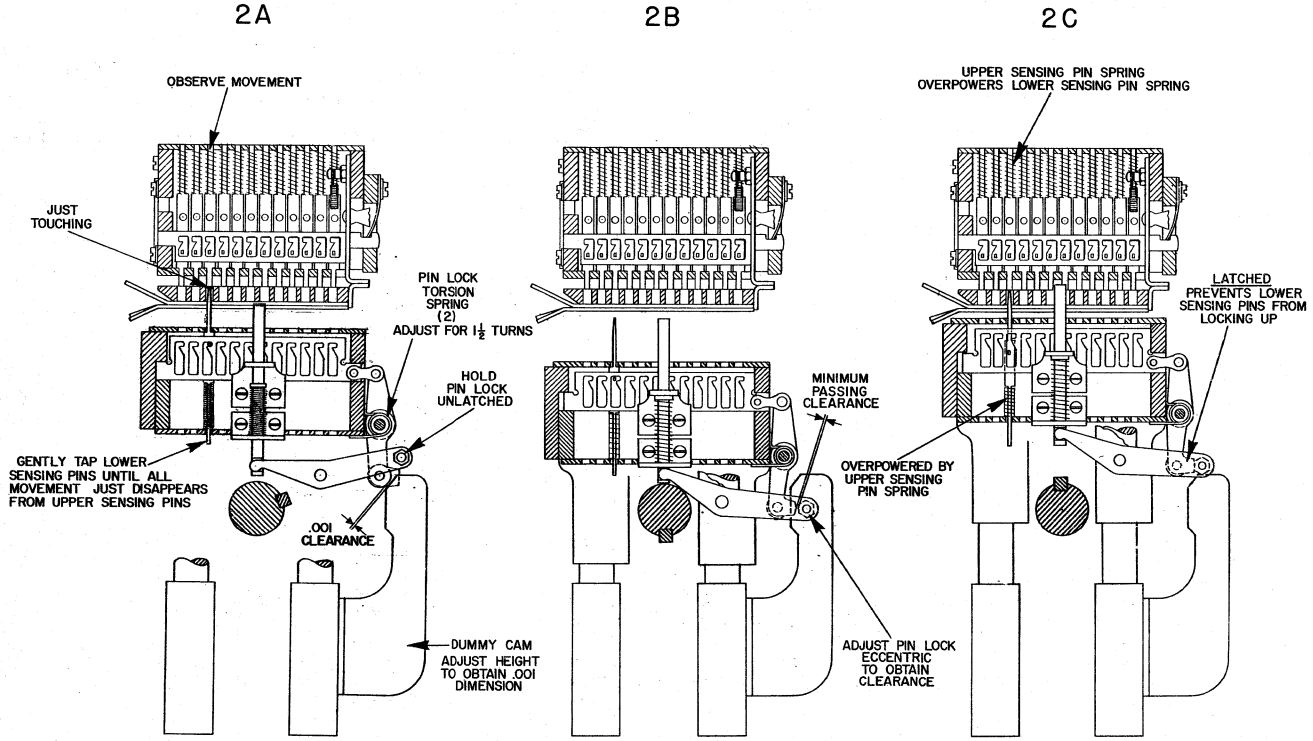
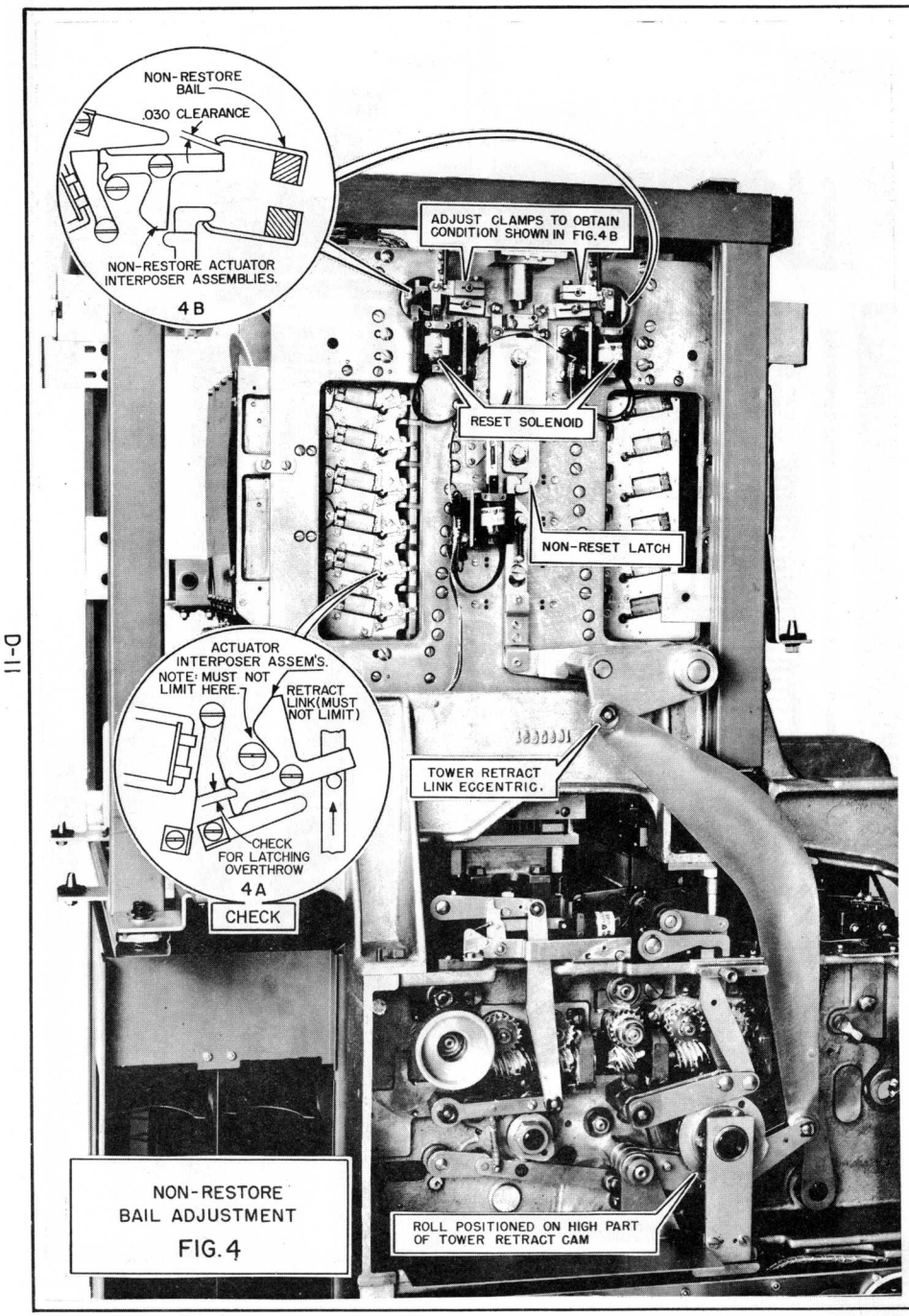


FIG. 1B



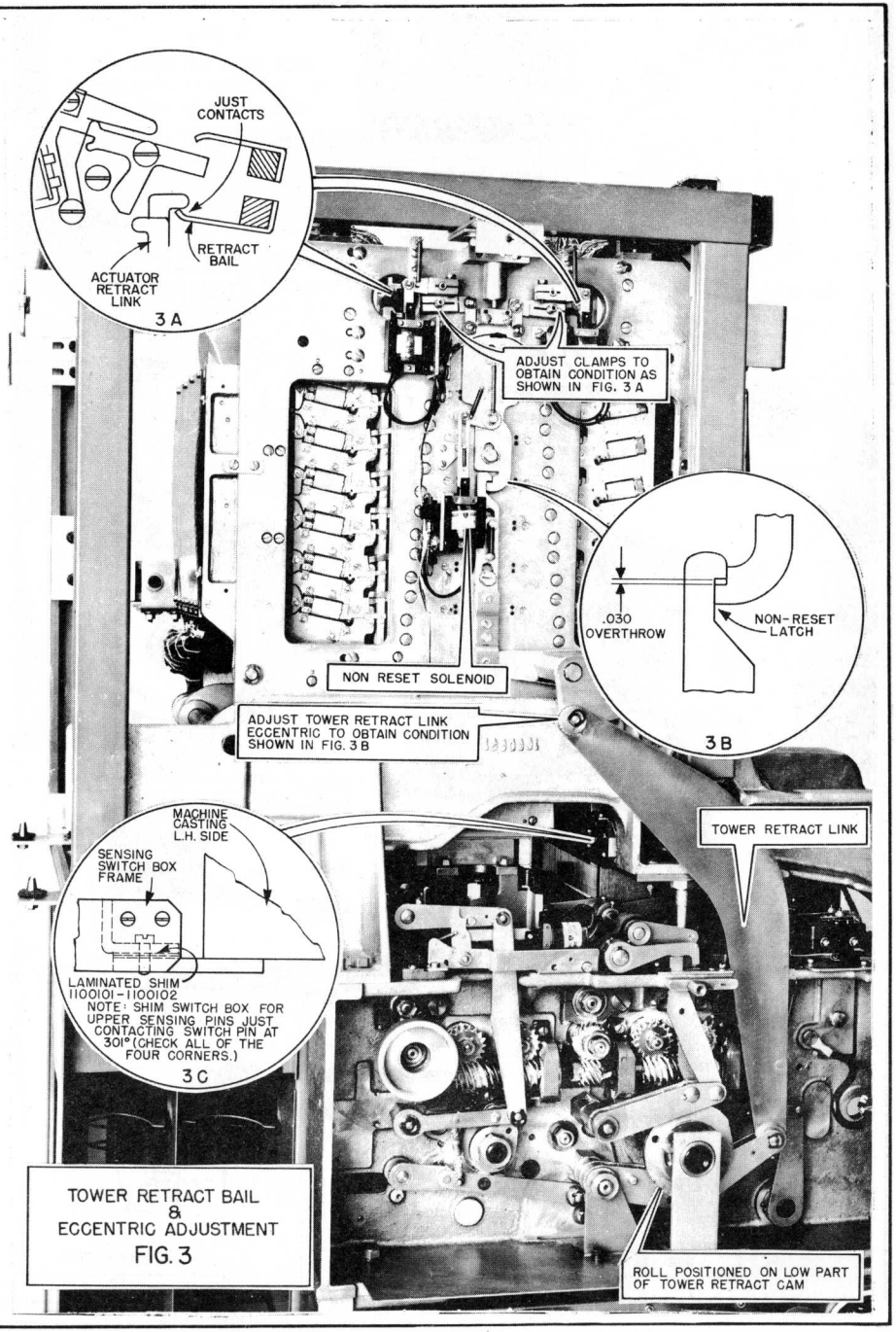
DUMMY CAM & PIN LOCK ADJUSTMENTS

FIG. 2



NON-RESTORE BAIL ADJUSTMENT

FIG. 4



TOWER RETRACT BAIL & ECCENTRIC ADJUSTMENT

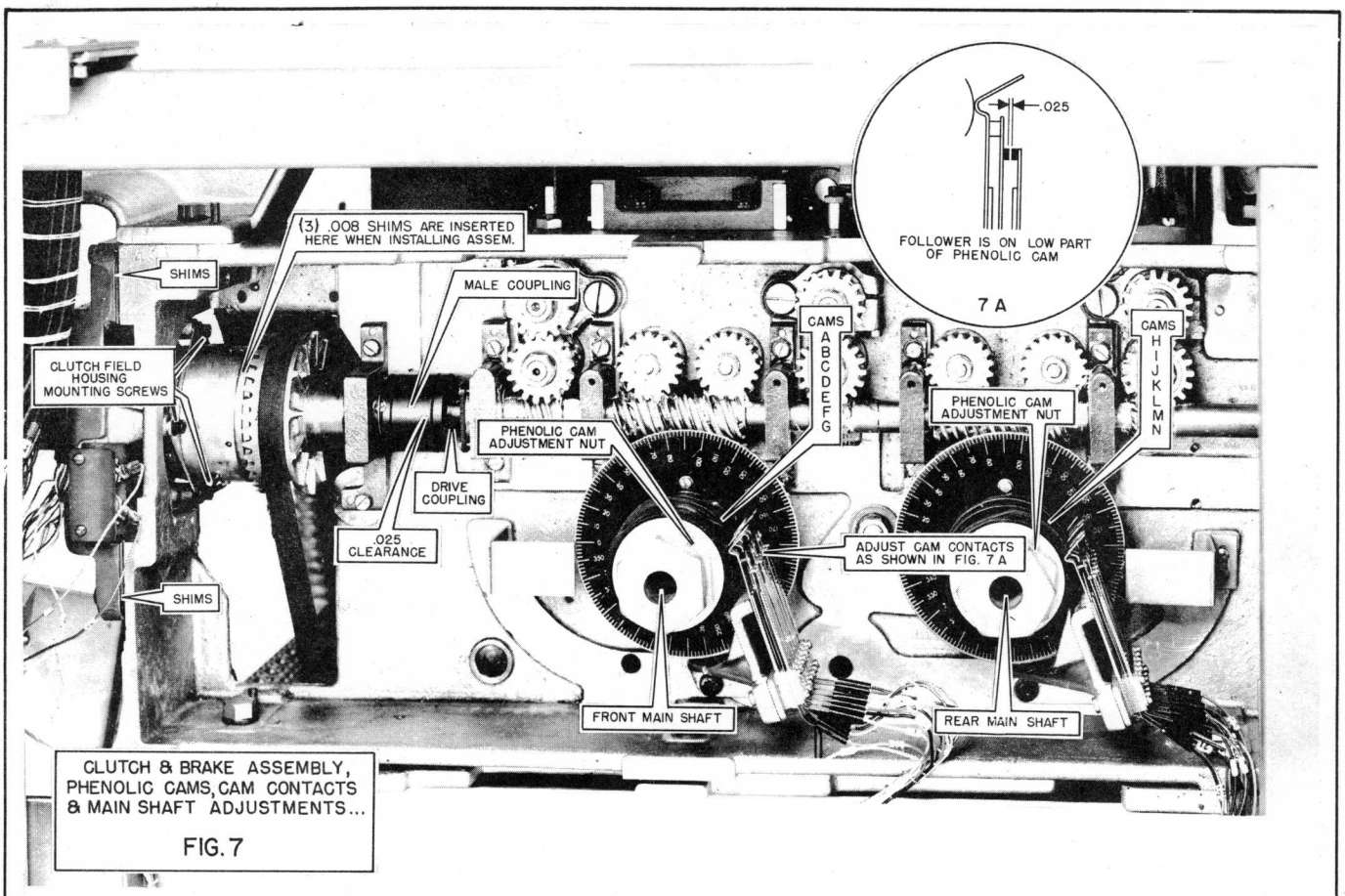
FIG. 3

SET BAR RETRACT, SKIP INTERPOSER ECCENTRIC & DIE SECTION CARD STOP

FIG. 5

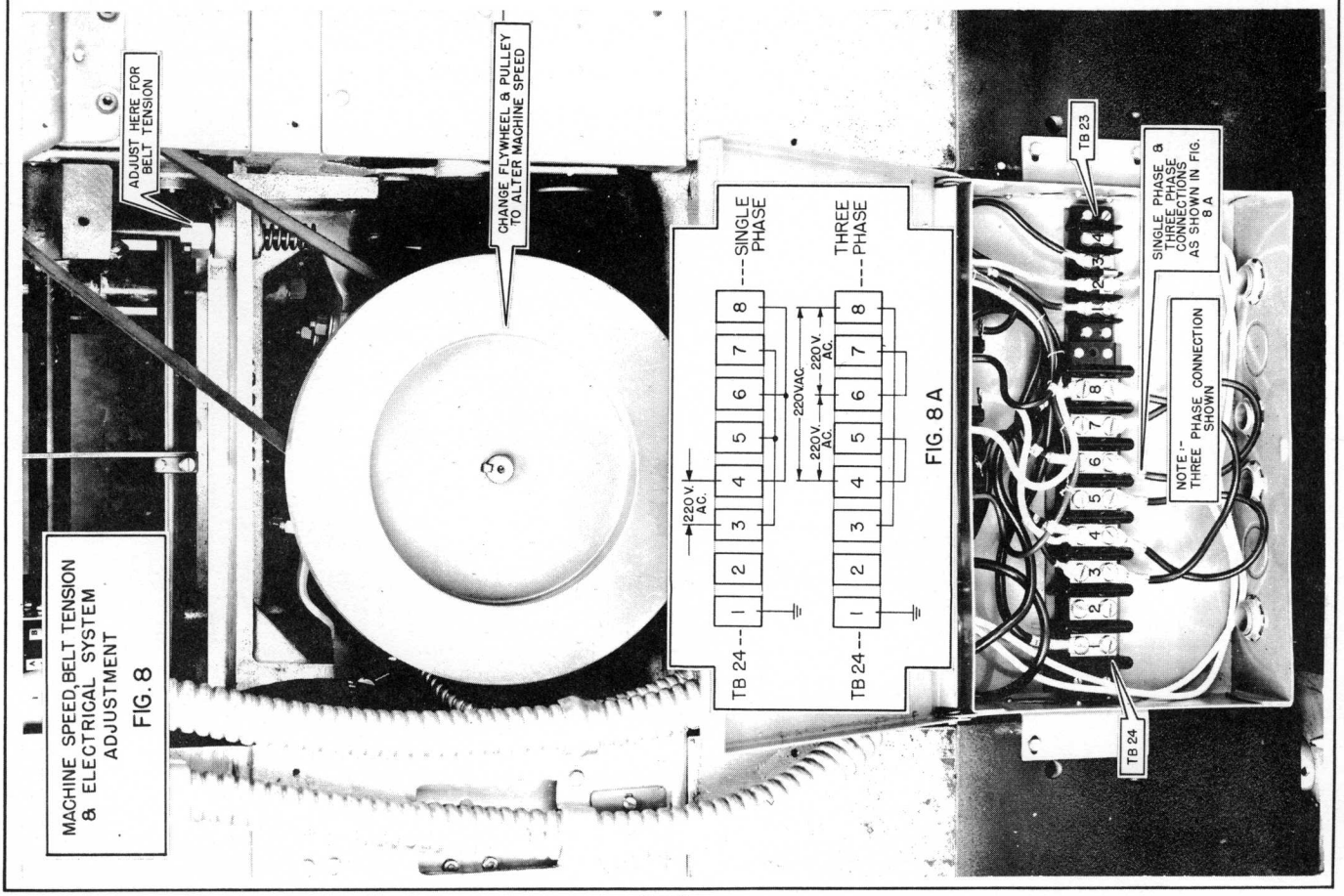
CARD JAM & SORT MICRO SWITCH & SHUTTER FINGER ADJUSTMENT

FIG. 6



CLUTCH & BRAKE ASSEMBLY, PHENOLIC CAMS, CAM CONTACTS & MAIN SHAFT ADJUSTMENTS...

FIG. 7



MACHINE SPEED, BELT TENSION & ELECTRICAL SYSTEM ADJUSTMENT

FIG. 8

FIG. 8 A

PREVENTIVE MAINTENANCE
for the
ELECTRONIC COMPUTER

UNIVAC 60 & 120

SECTION E

Remington Rand
DIVISION OF SPERRY RAND CORPORATION
315 FOURTH AVENUE
NEW YORK, N. Y.

FOREWORD

The preventive maintenance section of this manual is designed to establish a standard scheduled preventive maintenance procedure for the Electronic Computer Univac 60 & 120.

Punch

The Sensing and Punching Machine Inspection and Lubrication Procedure should be exercised every 30 days or after 350 hours usage, whichever comes first. This ordinarily would be performed during the Computer Corrective Inspection Period.

Computer

The intervals of scheduled maintenance for the Computer section are classified into three periods, Collective, Corrective and Connective.

The Collective inspection is scheduled bi-weekly as a rapid check to insure proper basic Computer operation.

The Corrective inspection is scheduled monthly as a complete check on circuits and voltages required to give optimum machine performance.

The Connective inspection is scheduled semi-annually as a check of all associated components and terminals for electrical as well as mechanical fitness.

The General inspection is a visual check on components and wiring as changes are necessitated and should be included during each of the Collective, Corrective and Connective inspections.

ELECTRONIC COMPUTER

UNIVAC 60 & 120

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Plugboard Depressor Mechanism.....	9E

UNIVAC 60 & 120 PUNCH

PREVENTIVE MAINTENANCE PROCEDURE

Frequency: Every 30 days or 350 hours of usage, whichever comes first.

Machine Covers

Remove covers from machine and put them in a convenient place so that the operators or personnel in the Tabulating Room will not trip over them.

Cleaning

Clean the entire machine by removing accumulated dirt, card lint and various substances. Also, remove displaced grease from all cams, rollers, gears and bearings. The entire machine must be cleaned throughout before lubrication is started.

Inspection Check List

1. Check Motor Belt Tension and Pulley Alignment.

2. Check Cam Contact gap for .025 inch.

3. Check Phenolic Cam Timings using an Ohm Meter to check Make and Break continuity on cam contacts.

Front Shaft

Cam	Make	Break	Cam	Make	Break
A	334°	30°	H	140°	196°
B	324°	200°	I	287°	73°
C	134°	280°	J	133°	94°
D	89°	280°	K	75°	131°
E	334°	70°	L	114°	75°
F	139°	235°	M	290°	116°
G	350°	46°	N	* 28°	*214°

* Cam N is adjusted to stop Punch between 268° and 275°.

4. Check Set Bar Section retract, All Set Bars must retract by 282°. At full retract, 302° to 313°, Retract Bar must not limit.

5. Check Upper Sensing Pin Box Retract, all Upper Sensing Pins must retract by 283°. At full retract, 291° to 345°, Retract Bar must not limit.

6. Check Sensing Switch Box Timing. Selected Upper Sensing Pins must contact Sensing Switch Box Intermediate Pins at 301°.

7. (a) Remove Upper Sensing Pin Box and check for broken Cell Plate Screws.
   (b) Check for sticky slides.
   (c) Check for binds in card stop action.
   (d) Check Comb Springs for wear and broken comb tines.

8. (a) Check Set Bar Section Comb Springs for wear and broken comb tines. This can be checked with Upper Sensing Pin Box removed. Remove Comb Spring protecting plate and check Comb Springs.
   (b) Check for sticky slides.

9. (a) Check clearance between Set Bar Section and Tower Rods. Maximum clearance .030 inch.
   (b) Check set up of Set Bar Section for set bar latching overthrow.

10. Check Die Section Card Stops.

   (a) Card Stops must not bottom.
   (b) Must open even and .025 inch below bottom surface of die plate.
   (c) Must not bind.

11. Check Micro Switch Operation.
   (a) Empty Feed Magazine Micro Switch.
   (b) No card in Sensing Micro Switch.
   (c) Card Jam Micro Switches.
   (d) Full Chip Pan Micro Switch.
   (e) Full Receiver Micro Switches.

12. Check Card Feed Magazine.

   (a) Picker Knife Adjustment .0045 inch go - .006 inch no go.
   (b) Throat Knife Adjustment .008 inch go - .010 inch no go.
   (c) Throat Knife release.
   (d) Card Feed Slide Side Play.
   (e) Magazine Alignment.

13. Check Clutch and Brake.

   (a) .025 inch to .035 inch clearance between Coupling and Drive Coupling.
   (b) Machine must stop between 268° and 275°. - 270°

14. Check all linkage for wear and all rolls for binds.

15. Check Non Restore Mechanism.

   (a) Reset Solenoids energized. Non Restore Actuator Interposer Assemblies must have maximum latching overthrow and not limit.
   (b) Reset Solenoids de-energized. Non Restore Actuators in a reset position must have .022 inch to .030 inch between Non Restore Bail and Non Restore Actuator Interposer Assemblies.
   (c) Non Restore Actuators in a tripped position must have .010 inch to .015 inch between Non Restore Bail and Non Restore Actuator Interposer Assemblies.

16. Check Set Up Actuators and Mechanism.

   (a) Set Up Actuators in a tripped position must have .031 inch $\pm$ .010 inch clearance between Rocker Arms and Interposer Assemblies.
   (b) Rocker Arms and Interposer Assemblies must align.
   (c) Set Up Actuators, in a latched position, must have passing clearance between Rocker Arm and Interposer Assemblies.
   (d) Machine dial reading 76° to 81°. Set Up Actuator Interposer Assemblies must have maximum latching overthrow and not limit.

(e) Check Set Hold Latch for proper bite and latching overthrow.

17. Machine dial reading 302° to 313°. When the Skip Interposer is in an operative position (Skip Solenoid energized) there must be .005 inch clearance between Skip Interposer and Stud.

18. Check Clear and Unit Switch Operation.

19. Check Card Release and Unit Switch Operation.

20. Check Skip Cycle Operation.

21. Check Non Restore Operation.

22. Check Sort Operation.

23. Check Reproduce Clear Operation.

Lubrication

After the machine has been thoroughly cleaned and generally inspected, it should be lubricated with lubricants prescribed for the various parts that appear in the plate drawings 1E through 9E.

Illustrations are provided with the intent that you familiarize yourself with the parts that require lubrication. The type of lubricants to be used is identified by code numbers on each plate drawing. The letter S included with some code numbers indicates that the lubricant should be applied as a Spray.

While it would be impossible to illustrate each part that requires lubrication, sufficient units of the machine are shown to establish identity of parts to be oiled or greased within the area of the unit.

The numbers 1, 2 and 3 on each illustration represent the code number of the three types of oil. Code #4 and #5 represent the type of grease to be used.

In all instances where parts are not illustrated or where parts are shown with the absense of a code number, it is assumed that the serviceman will use his own good judgment in selecting one of the five following types of lubricant prescribed for use on Tabulating equipment. This may easily be determined by observing the type of lubricant used on parts that are illustrated in the various drawings.

Types of Lubricant to Use

Three types of oil and two types of grease have been selected as standard for purpose of lubricating Tabulating equipment. Under no circumstances are lubricants other than those five standard types to be used. Experiments have proved that satisfactory lubrication results have been obtained using the following three types of oil and two types of grease.

CODE #1

Velocite "E" Oil - Symbol #SVC-325L - To be used on all light mechanisms operating with extremely close tolerances.

CODE #2

#318 White Industrial Oil - Symbol #SVC-95L - To be used on Shaft Casting Bearings 3/8" in diameter or less or parts operating under light friction.

CODE #3

Rubrex Medium Oil - Symbol #SVC-113L - To be used on Pivot Points, Hubs and general Shaft Casting Bearings with a diameter 7/16" and above or parts operating under excessive friction.

CODE #4

Lubriplate #130AA Grease - Symbol #SVC-370L - To be used on all Gears, Follower Rolls, Cams and sliding surfaces not lubricated with above oils.

CODE #5

Gargoyle BRB #4 Grease - Symbol #SVC-146L - To be used for machines equipped with a Transmission.

When lubricating the machine, it is suggested that you establish a systematic method of lubrication. The machine should be completely lubricated with each one of the five types of lubricants.

Start lubricating the machine by using Grease #4 on all parts listed and shown in the illustrations; then proceed by using Oil #3 first, then Oil #2. Use Oil #1 last for all light mechanisms operating with extremely close tolerances. Old grease and oil must be removed from parts that require grease; otherwise, the newly applied grease will not stick to the parts.

The purpose of this machine outline should not be misconstrued. Its purpose is to aid you in formulating a habit of systematically lubricating the entire machine by beginning with one section and proceeding until the machine is completely lubricated. The serviceman should follow this theoretical machine procedure outline until such time as he is thoroughly familiar with the proeedure and can systematically lubricate the entire machine without its use.

BI-WEEKLY (COLLECTIVE)

Inspection Time - 1½ Hours

Clean Dust Filters

Run Test Problem to check Input-Output, Storage, Shifts, Elements, Processes and Decimals. This Program should run without repeat for 30 Minutes.

Check Filament DC return Resistors for Burn-Out or Discoloration. These Resistors are located on a Terminal behind the Power Supply and are easily accessible once the Storage Door is opened. These Resistors burn-out due to Filament Cathode short which leaves the Filament Supply Floating

Resistors within the cages when seriously discolored should be checked for proper value.

MONTHLY (CORRECTIVE)

Inspection Time - 3 Hours

DC Voltages

1. Adjustment:
   The DC Voltages should be set with the line voltage at its normal value. If a regulator is not used then the DC Voltages should be changed by the percentage that the line voltage is off. For example, if the line is temporarily low by 3% then all the DC Voltages could be expected also to be 3% low when properly adjusted. However, if the line is observed to always be slightly low by a line voltage recording an adjustment could be made for the normal DC Voltages.

2. Meter Accuracy:
   a. The Computer Panel Meter should be calibrated at least once a year against a standard meter of at least 0.5% accuracy. The Panel Meter should indicate within ± 3%.

   b. The Computer Panel Meter may be used for adjustment of the voltages or a portable meter which is calibrated every 30 days against the standard meter, at the exact voltage points to be used, may be employed. An Oscilloscope may be used to measure the ripple by using the peak-to-peak readings. Excessive ripple is usually an indication of lowering of the effective capacity of the filter units. It should be noted, however, that the surge protective relays must be closed to shunt out the surge resistors in the power supplies.
   For Example: The -165V supply pulls in Relay 209 which shunts out R203, then Relay 210 pulls in to shunt out R201 and R202 so that C203 is now returned directly to Gnd.

3. DC Voltage Levels and Ripple:

SUPPLY	NOMINAL	MAX. RIPPLE R.M.S.	PEAK-TO-PEAK
a. +150V	±2 V	1.5 V	3.6 V
b. + 75V	±2 V	0.35V	0.85V
c. - 15V	±1 V	0.06V	0.15
d. - 40V	±1 V	0.07V	0.17
e. - 60V	±2 V	0.9 V	2.2
f. - 90V	±2 V***	0.55V	1.4 V
g. -150V	±2 V	0.8 V	2.0
h. -165V	±2 V*	0.08V	0.2 V
i. -375V	±10V	0.8 V	2.0
j. -400V (25V Bias Supply)	±2 V**	0.3 V	0.73

* The -165 Volt level is given for a maximum number of storage bits set. The nominal with all storages cleared is -167 Volts for the Univac 60 and -169 Volts for the Univac 120.

** Note that the -400 Volt supply is measured with respect to the -375 Volts supply and not to ground.

*** The B2 and B5 levels should be ± 2 volts within the -90 volt supply.

AC Voltages

1. With nominal line voltage the heater voltages should be within the following limits:

   a. All Chassis (at the chassis male contacts) 6.3V ± 0.2V

   b. All 6.3 volt tubes mounted in the frame 6.3V ± 0.2V

   c. All 6.3 volt rectifiers (measured at the socket) 6.3V ± 0.2V

   d. All 2.5V rectifiers & thyratrons (measured at the socket) 2.5V ± 0.1V

Filament Supply

1. Measure at chassis clips unless otherwise specified.

   a. ABC - Acc. 4A to 11A incl., 1M to 8M incl.

b. DEF - Acc. 1A to 3A incl., 9M to 11M incl., SB, CTL, ØF, CCT, RIG, MD, OCL-1 & OCL-2.

c. GHI - SS1 to SS10 incl., SCL, ZCL, DCL, DCR, TCR.

d. KLM - IO1 to IO10 incl., KB1 to KB4 incl., VAD, STL1 to STL6 incl.

e. NO - STL1 to STL6 incl., STA1 to STA6, (6AS7's) incl., VAD.

f. PQ - IO1 to IO10 incl.

g. RS - STL1 to STL6 incl.

h. T-21 - Rectifier Tubes (See Print 1940237) Measure at tube socket.

i. T-28 - -40V supply, select thyratrons (See Print 1940249) Measure at tube socket.

2. Suggested Check Points:

Filament	Trans.	Chassis	Clip Connection
ABC	T26A	5A	6-8, 8-10
DEF	T26B	3A	6-8, 8-10
GHI	T26C	SS4	45-47, 47-49
KLM	T26D	STL	40-42, 42-44
NO	T27	STL	36-38
PQ	T27	IO	12-14
RS	T27	STL	2-4

Full Chip Pan Detector Operation Check

Card Jam Device Operation Check

Input-Output Recovery Circuit

The Input-Output Recovery Circuit may be checked by observing the operation of stage ICL in the ZCL chassis. Each and every operation of DEA operates stage ICL, which in turn generates the voltage to return the Input-Output lines to normal through the assigned diodes (left side of (2) C09) in the individual IO chassis. This discharges all the gate grids to prevent any undesirable Alpha-Check indications while the Keyboard biases are changing. Check this on Cage Pin #7 of LL-3 of all IO Chassis.

Keyboard Bias Reset Circuit

This may be checked by observing the cathode of ØLD (1 & 2) in the ØF chassis. All keyboard bias lines are rapidly returned to normal by this circuit.

Storage Read Out Blocking Bias

This has been incorporated to prevent false Alpha-Check indications during the zeroizing of the selected storage. Its operation is controlled from stage EZ, CTL chassis, and may be observed on the cathode of stage SKBK, CCT chassis.

Storage Hold and Clear

Each Storage Clear Line of storages S1 through S12 shall be observed with Oscilloscope for proper operation as shown on Dwg. 1940409.

Zero Check Line

This is to be checked through cage pin "one" of stage Ø9C in Zero Factor chassis. This is a grid point and should operate from approximately -25 Volts to slightly above zero. The operation may be checked as follows:

1. Select N1 as V1 of Step 1 - plug for a one in Column 1A in the Accumulator.

2. Test counter set to pre-shift zero.

3. Observe the grid point, allowing shifting one position at a time until the digit reaches Column 11A. While the digit remains in Columns 1A through 10A, the grid should remain slightly above zero. When the digit reaches Column 11A, the grid voltage will change to -25 Volts.

Keyboard Bias Detector Circuit

This is to be checked by removing the element call line from a normal step and observing the stopping of the step on the CX pulse for the RIG cycle associated with that element registration.

Plugboard Mechanism Check

SEMI-ANNUAL (CONNECTIVE)

Inspection Time - 8 Hours

Relays

1. Relay contacts should be dusted whenever it is necessary to remove their dust covers or otherwise inspect them. For those which are covered, this should be done at least once every six months. Those which have no dust covers should be dusted at least every 60 days. The movable contacts of relays should never be adjusted: if this contact spring requires adjustment the relay is to be replaced.

2. The mercury plunger type relays in the power control section should be checked to see that the glass tube is at the correct height within the operating coil. This height is indicated by a mark on the tube.

Screw Type Terminals

All screw type terminals should be checked at least once every six months to

insure that they are mechanically tight. A loose terminal in a high current circuit can cause burning of the terminal block if allowed to continue.

Installation Test Board Operation

Every six (6) months each machine shall be checked with the installation test boards; this is to include Alpha-Check of Input-Output Section and "Service Boards" test as described in the Installation Procedure. The Step, Storage, and Branching Program should be run with simulated high and low line conditions (±8%). This requires one external jumper on the VAD chassis. (Lug #34 to Lug #3).

Switches and Lights Check

All switches, lights, etc. shall be tested for proper operation.

Spare Chassis Check

All spare chassis shall be checked on related programs of above.

VAD Chassis Setting Check

The Grid Level of the Thyratron #1 (Pin 1 of RC-46 high level * adjustment) is set to -162 Volts. The grid level of Thyratron #2 (Pin 1 of RC-9 low level * adjustment) is set according to the relation of +138+E, where E is the actual meter reading of the -150 volt supply. If the -150 volts supply is normal, then the voltage level would be -12 Volts. The operation of this chassis for voltage fluctuations is checked by blocking the -150 lug to the VAD chassis and supplying an external DC voltage of -150 Volts to the chassis. This voltage is then varied from -162 to -138. At both the high and low voltage variations, the relay operated from stage OTP will de-energize and open the B+ (+150) to the Punching Sensing Unit, Reproduce transfer relay and light the Voltage Indicator Light on the Control Panel of the Punching-Sensing Unit. Blocking of the -150V lug may be done by removing the chassis and inserting a strip of paper around the chassis lug and reinserting the chassis. When the voltage is returned to normal the relay is reset by operating the Clear-Punch Switch or ground lug #19 on the VAD Chassis.

* If a regulator or a Variac is not available at the installation, two 6 Volt lantern batteries may be connected in series aiding to obtain -162 Volts or in series bucking to obtain -138 Volts.

GENERAL INSPECTION

Chassis Contacts

When Chassis are removed and any dust is present, the Chassis Contacts and the frame contacts should be dusted with a typewriter cleaning brush to remove any dust that might interfere with contact when the Chassis is reinserted. If the environment should cause any greasy film to accumulate, this should be removed with a cloth saturated with perchlorethylene. Never use an abrasive material on the contacts. The black discoloration which forms on silver is a good conductor; therefore, it is not necessary that the

material be bright. Both the chassis and frame contacts should be checked for distortion in a direction which would cause either light pressure or misalignment when the Chassis is inserted.

Disconnect Contacts (only when disconnects need to be opened)

All disconnect contacts should be inspected visually for distortion prior to closing the block, and as the block is closed a light should be used to insure that a small misalignment does not cause the contact blade to fall outside the contact springs.

Wiring

During the course of trouble shooting at all times the serviceman should be on the lookout for possible trouble due to wires under tension which might cause failure due to pull-out of the wire from the pressure type connector, or chafing through the insulation to ground against the frame. If necessary these wires can be tied back or taped with "Scotch Electrical" tape to relieve this condition.

Cage Components

Whenever a cage must be handled a visual inspection should be made for mechanical shorts or for spacings which are so close that a metallic dust particle could cause a short. This is especially true of the STB-1 cages because of the large number of components contained and of the construction of the small diodes used. Excessive bending of these diodes leads should be avoided since the diode will fracture. A slight spacing is sufficient if a few drops of glyptol are placed into the spaces.

Chassis Internal Wiring

If a trouble appears and disappears when a cage or tube is moved the Chassis should be opened and visually inspected for unsoldered or poorly soldered connections, broken wires, broken resistors, or shorting of wires.

Punch Actuators

Actuators should be kept free of dust by keeping the punch covers on <u>at all times</u> except when actual service of the tower is required. Adjustment of actuators should never be made in the field since special test equipment is necessary for this purpose.

Cooling System

The Univac 60-120 Computer Cooling Systems require that the covers of the computing unit be kept in place at all times except when actual service is taking place. These covers are an integral part of the cooling system.

Fan Motors

The fan motor bearings are life-time grease packed and should not require attention. After a days run, however, the motor housings and bearing ends should be checked for excessive heating by placing the hand on each motor.

Marginal Operation

1. At normal voltages
   A measure of the operating condition of the computer may be obtained by plugging any program that uses a reasonable part of the capabilities of the machine, so that instead of branching to "Trip" the computer will continue to calculate by branching back to the first step. If this is done with the "Restart" not plugged, then the computer should cycle itself for a period of from at least ten minutes up to eight hours or more. A line transient may cause the computer to stop, how ever, even though no marginal condition exists. The point of stopping each time should be recorded from the Program Test Panel in order to pin point the common trouble point if possible.

2. At high or low line voltage
   If no common trouble point can be arrived at, then a slight lowering or raising of the line voltage by means of the voltage regulator will sometimes help to make the trouble appear frequently enough to be located with the scope. Should the change in line voltage fail to make a noticeable difference in the frequency of hangups, then the voltage should be returned to normal.

PREVENTIVE MAINTENANCE STICKER

MACHINE INSPECTION RECORD

PHASE Collective Corrective Connective	DATE				RTM
D. C. Supply D. C. Actual	+150	+75	-15	-40	-60
D. C. Supply D. C. Actual	-90	-150	-165	-375	-400
Filament A. C. Actual	ABC 6.3	DEF 6.3	GHI 6.3	JK 6.3	LM 6.3
Filament A. C. Actual	NO 6.3	PQ 6.3	RS 6.3	T-21	T-28

REMARKS:

Service Technician_____

REMINGTON RAND DIVISION
SPERRY RAND CORPORATION

This sticker is to be mounted on the Power Control frame to the left of the meter panel.

The sticker is to be replaced after each collective or bi-weekly inspection. The date and RTM (running time meter) values should be recorded at each inspection.

The voltage values required should be measured at the Power Supply on TB 110 except -165 volts and -40 volts which can be measured at the STL chassis. The Filament voltages are to be measured at the chassis clips except those so designated to be measured at the tube sockets.

Any variation over $\pm$ 2 volts between the 90 volt readings and the B2 or B5 voltage readings should be so noted under remarks.

The sticker is to be signed by the technician performing the inspection.

TEST PROGRAM

This test program is designed to check the fundamental circuits of the computer.

All storage digits as well as minus indication are checked. The various processes are checked. All decimals are checked.

The following is the sequence of the program.

1. The V1 of step 1 is N1 (all Relays de-energized).
2. Branch of step 20 fires Select I Thyratron and energizes Relay 1.
3. The V1 of step 1 is N2 (Relay 1 energized).
4. Branch of step 20 fires Select II Thyratron and energizes Relay 3. (Relay 1 de-energized).
5. The V1 of step 1 is N3 (Relay 3 energized).
6. Branch of step 20 fires Select III Thyratron and energizes Relays 5 and 2. (Relay 3 de-energized).
7. The V1 of step 1 is N4 (Relay 3 energized).
8. Branch of step 20 fires Select I Thyratron and energizes Relay 9. (Relay 2 energized).
9. Start to Select step IV (Relay 9 energized).
10. Select IV Thyratron energizes Relay 7. (Relays 5, 2 & 9 are de-energized).
11. The V1 of Step 1 is N5 (Relay 7 energized).
12. Branch of step 20 goes to trip and problem is ready to repeat. (Trip de-energizes Relay 7).

This program can also be used to check the punching circuitry. A suggested method would be as follows.

1. The + and - branch of step 12 should be wired to COM 1-2 (present + branch of step 20).
2. Plug all storages for Set 1.
3. Plug storages S1 through S9 on the plugboard to columns 1-90.
4. Plug storage S10 and 8 columns of storage S11 to the zero positions of columns 1-90.
5. Plug Clear to Trip instead of Start.
6. Plug S 7-2 to Set I instead of Trip.
7. Use blank cards.

8. Five cards must be fed for every tower set up actuator to be operated.

NOTE: In a Univac 60 it would require replugging the punch plugboard in order to check all tower actuators. The branch of step 6 would be plugged to COM 1-2.

SELECTOR CHART EXPLANATION

1. Relay Contacts

   A. COM 3-1

      (1) This refers to the fact that this position is wired on line 3-1 under the common position.

   B. NS 5-2

      (1) This refers to the fact that this position is wired on line 5-2 under the non-select position.

   C. S 1-3

      (1) This refers to the fact that this position is wired on line 1-3 under the select position.

2. Relays

   A. P.U. Ry 9

      (1) This refers to the fact that this position is wired to the pick up of Relay 9.

3. Select Step

   A. SEL. III

      (1) This refers to the fact that this position is wired to the "IN" hub of the Select Step III.

   B. P. S. III THY.

      (1) This refers to the fact that this position is wired to the PROG. SEL. III bus on the plugboard. This bus represents the plate of the Select III Thyratron which is fired during a Select III Step.

SELECTOR CHART NO.:

APPLICATION:

UNIVAC 60 & 120

PUNCHED-CARD ELECTRONIC COMPUTERS

Remington Rand

TABULATING MACHINES

ELEMENTS

CONSTANT FACTORS: INDICATE DECIMAL LOCATION, NEGATIVE CONTROL AND VALUE IN DESIRED ACCUMULATOR COLUMNS.
CARD FACTORS: INDICATE TRANSFER LINE (FIELD.F1, F2, ETC: CONTROL - C1, C2, ETC.) DECIMAL LOCATION. NEGATIVE CONTROL AND TRANSFER LINE. INDICATE CARD COLUMNS IN ACCUMULATOR INPUTS ON RIGHT.

ELEM DESIG	TO	NEG. CONT. COL	NEG. CONT. POS	NEG. CONT. TRF LINE	DEC LOC	ACCUMULATOR COLUMNS 10	9	8	7	6	5	4	3	2	1
N1					10/1	1	3	5	7	9	1	3	5	7	9.
N2			-		10/1	3	5	7	9	1	3	5	7	9	1.
N3					10/1	5	7	9	1	3	5	7	9	1	3.
N4			-		10/1	7	9	1	3	5	7	9	1	3	5.
N5					10/1	9	1	3	5	7	9	1	3	5	7.
N6					10/1	0	0	0	0	0	0	0	0	0	0.
N7					5/4					4	4.	4	4		
N8					5/5					2.	2				
N9			-		6/5				3	3.	3	3			
N10					4/3						3	3.	8	8	
N11					5/4			1	1	1	1.				
N12					3/2					3	3	3	3.		
N13					7/6			6	6.	6	6				
N14					8/7				.9	9	8	3	2	6	3
N15					9/8			.1	0	0	2	3	9	9	
N16					10/9	2.	1	5							
N17					11/10	.1	5								
N18					2/1									1.	0

ELEM DESIG	TO	NEG. CONT. COL	NEG. CONT. POS	NEG. CONT. TRF LINE	DEC LOC	ACCUMULATED COLUMNS 10	9	8	7	6	5	4	3	2	1
N19															
N20															
N21															
N22															
N23															
N24															
N25															
N26															
N27															
N28															
N29															
N30															
N31															
N32															
N33															
N34															
N35															
N36															

ACCUMULATOR INPUTS

TOP LINE - TRANSFER LINE (F1.F2, ETC.)
INDICATE:
BOTTOM LINE - CARD COLUMNS

SYM.	ACCUMULATED COLUMNS 10	9	8	7	6	5	4	3	2	1
A1										
A2										
A3										
A4										
A5										
A6										
A7										
A8										
A9										
A10										
A11										
A12										

REPRODUCE

| | | | | | | | | | | | | | | |

PROGRAM CHART NO.

APPLICATION:

UNIVAC 60 & 120

PUNCHED-CARD ELECTRONIC COMPUTERS

Remington Rand

TABULATING MACHINES

TABLE OF FACTORS

SYM	SIGN	CARD NO.	CARD FIELD TITLE OR CONSTANT VALUE	SYM	SIGN	CARD NO.	CARD FIELD TITLE OR CONSTANT VALUE	SYM	SIGN	CARD NO.	CARD FIELD TITLE OR CONSTANT VALUE
N1			1 3 5 7 9 1 3 5 7 9.	N13			6 6 . 6 6	N25			
N2	-		3 5 7 9 1 3 5 7 9 1.	N14			.9 9 8 3 2 6 3	N26			
N3			5 7 9 1 3 5 7 9 1 3.	N15			.1 0 0 2 3 9 9	N27			
N4	-		7 9 1 3 5 7 9 1 3 5.	N16			2 . 1 5	N28			
N5			9 1 3 5 7 9 1 3 5 7.	N17			.1 5	N29			
N6			ZERO	N18			1 . 0	N30			
N7			4 4 . 4 4	N19				N31			
N8			2 . 2	N20				N32			
N9	-		3 3 . 3 3	N21				N33			
N10			3 3 . 8 8	N22				N34			
N11			1 1 1 1 .	N23				N35			
N12			3 3 3 3 .	N24				N36			

CARD DESCRIPTION

STEP NO.	CARD NO.	VALUE 1 DESCRIPTION	SIGN	SYM	PROCESS	VALUE 2 DESCRIPTION	SIGN	SYM	RESULT DESCRIPTION	SIGN	SYM	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	NEXT STEP —	NEXT STEP +
1		COM 1-1			+	N6 ZERO			S1 STOR. & IO CHECK															2	2
2		S1			+	N6 ZERO			S2 STOR. & IO CHECK															3	3
3		S2			+	N6 ZERO			S3 STOR. & IO CHECK															4	4
4		S3			+	N6 ZERO			S4 STOR. & IO CHECK															5	5
5		S4			+	N6 ZERO			S5 STOR. & IO CHECK															6	6
6		S5			+	N6 ZERO			S6 STOR. & IO CHECK															7	7
7		S6			+	N6 ZERO			S7 STOR. & IO CHECK															8	8
8		S7			+	N6 ZERO			S8 STOR. & IO CHECK															9	9
9		S8			+	N6 ZERO			S9 STOR. & IO CHECK															10	10
10		S9			+	N6 ZERO			S10 STOR. & IO CHECK															11	11
11		S10			+	N6 ZERO			S11 STOR. & IO CHECK															12	12
12		S11			+	N6 ZERO			S12 STOR. & IO CHECK															13	13
13		N11 1111.			-	N12 3333.			S1 COMPLEMENTIZE															14	
14		N9 -33.33			x	N10 33.88			S2 MULT. IN NOTES															15	
15		N7 44.44			÷	N8 2.2			S3 DIV. IN NOTES																16
16		N8 2.2			÷	N6 ZERO			S4 N ÷ 0																17
17		N6 ZERO			÷	N6 ZERO			S5 0 ÷ 0																18
18		N14 .9983263			x	N15 .1002399			S6 1M/2M CARRY BLOCK																19
19		N18 1.0			+	N17 .15			S5 IO ZERO CHECK																20
20		N13 66.66			-	N16 2.15			S4 DECIMAL TEST																COM 1-2
21																									
22																									
23		FOR A UNIVAC 60 OMIT STEPS 7 THRU 12 INCLUSIVE.																							
24																									
25																									
26		FOR A UNIVAC WITH ONLY ONE KB CHASSIS OMIT STEPS 18, 19 & 20. THE FOLLOWING																							
27		DECIMALS WOULD BE LEFT UNCHECKED 2/1, 8/7, 9/8, 10/9 & 11/10.																							
28																									
29																									
30		PLUG FOR PROGRAM REPEAT, BLOCK CLIP #18 OF SCL CHASSIS AND PROGRAM WILL																							
31		CONTINUOUSLY RECYCLE WHEN THE PUNCH MOTOR IS TURNED OFF.																							
32																									
33																									
34																									
35																									
36																									
37																									
38																									
39																									
40																									

SYM	CARD FIELD TITLE	NEG. COL	NEG. POS	OUTPUT PUNCHING 10	9	8	7	6	5	4	3	2	1	DEC LOC	SET 1	SET 2	CLEAR	SYM
S1														1/0			X	S1
S2														1/0			X	S2
S3														1/0			X	S3
S4														1/0			X	S4
S5														1/0			X	S5
S6														1/0			X	S6
S7														1/0			X	S7
S8														1/0			X	S8
S9														1/0			X	S9
S10														1/0			X	S10
S11														1/0			X	S11
S12														1/0			X	S12

FROM OUT	TO IN
START	COM 9-1
SET 1	SET 2
SET 2	CLEAR
SORT 1	SET 1
SORT 2	SET 1
CLEAR	START
P.S. I	SET 1
P.S. II	SORT1
P.S. III	SORT2
P.S. IV	STEP1

REPRODUCE CONTROLS	COL.	POS.
REP		
SKIP		
SET HOLD		
SEC REP		

	0 ÷ 0	N ÷ 0
STOP		
SORT		

RESTART	
STEP	
PROGRAM	X

81-1389 RRBH 12456

PUNCH BASE (FRONT VIEW)

PLATE IE

LUBRICATION CHART

1. Velocite "E" Oil
2. White Industrial Oil
3. Medium Oil
4. Lubriplate #130AA Grease

NOTE:
(S) SPRAY with designated oil

PUNCH BASE (LOWER LEFT SIDE)

PLATE 2E

LUBRICATION CHART

1. Velocite "E" Oil
2. White Industrial Oil
3. Medium Oil
4. Lubriplate #130AA Grease

NOTE:
(3) SPRAY with designated oil

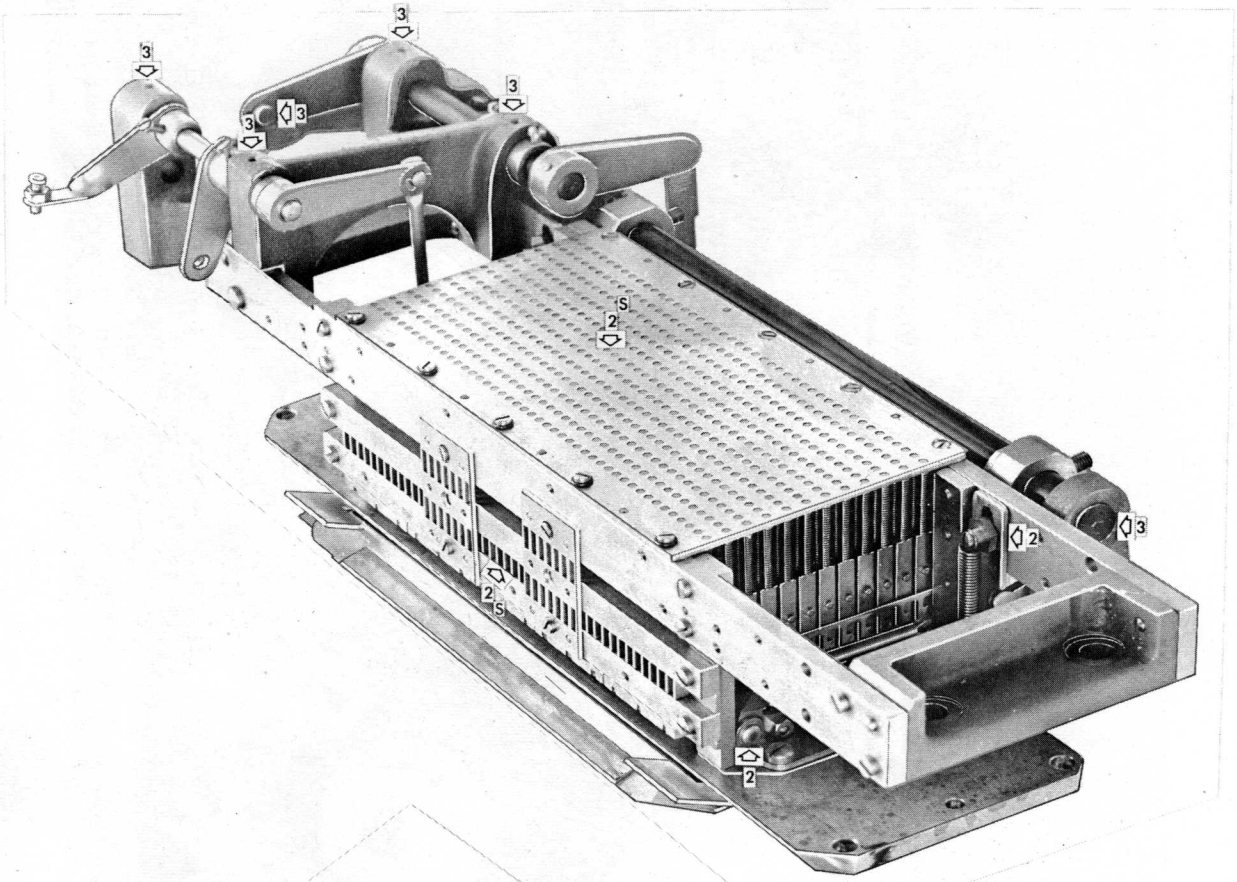
PUNCH BASE (LOWER RIGHT SIDE)

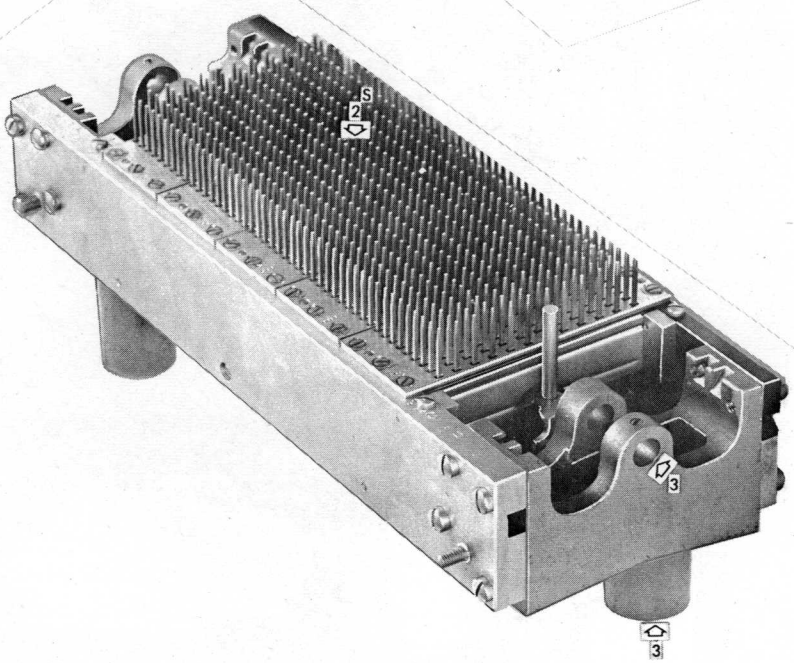
LUBRICATION CHART

1. Velocite "E" Oil
2. White Industrial Oil
3. Medium Oil
4. Lubriplate #130AA Grease

NOTE:
(S) SPRAY with designated oil

PLATE 3E





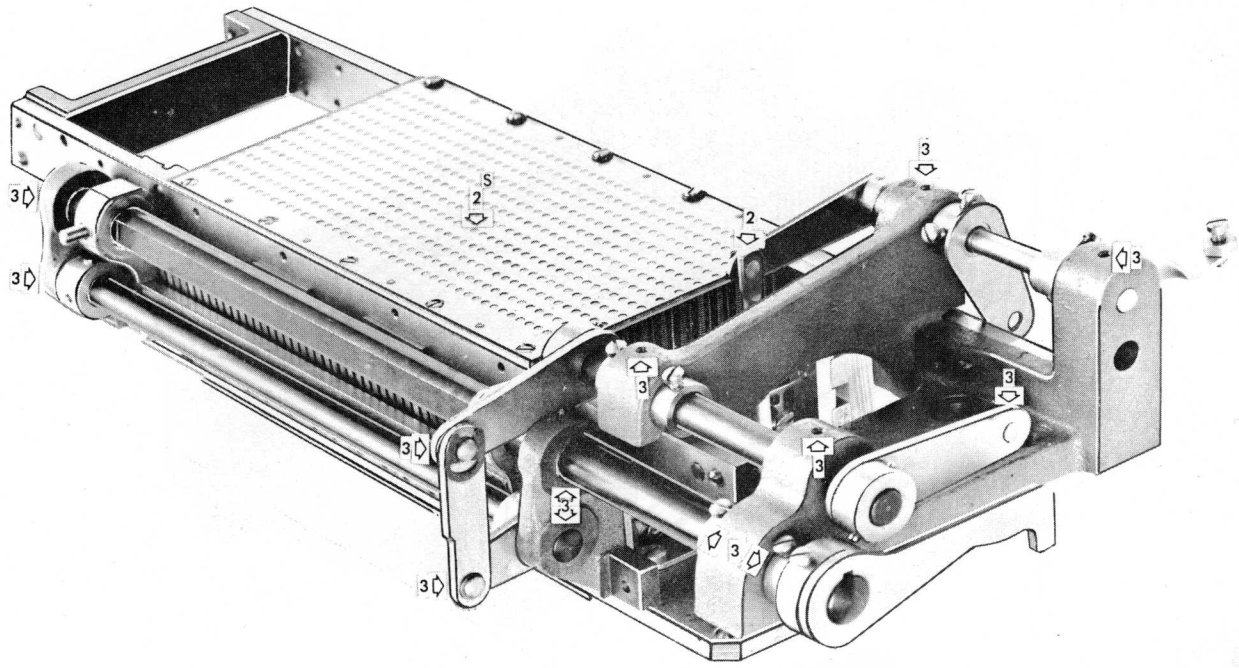
LUBRICATION CHART

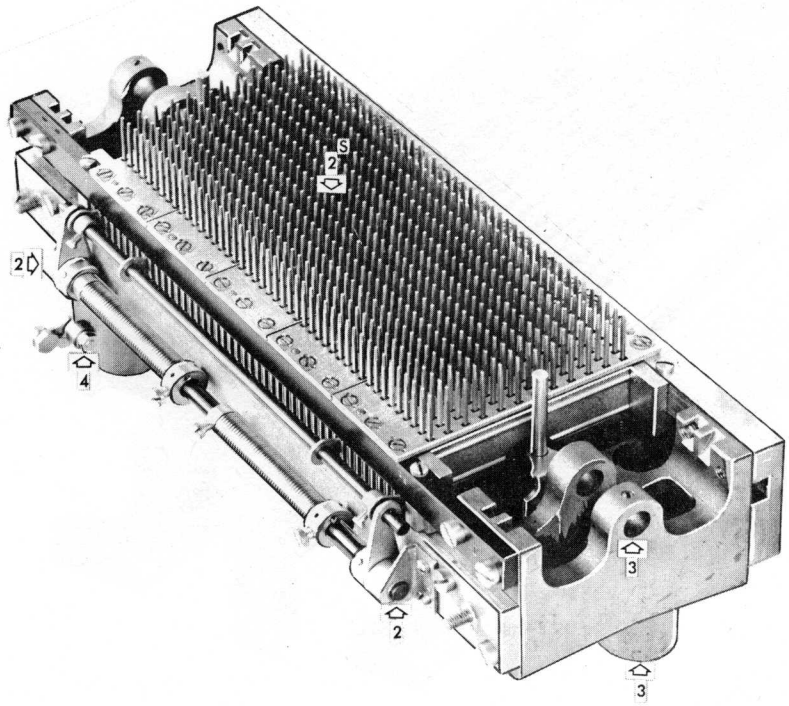
1. Velocite "E" Oil
2. White Industrial Oil
3. Medium Oil
4. Lubriplate #130AA Grease

NOTE:
(S) SPRAY with designated oil

UPPER & LOWER SENSING PIN BOX (FRONT VIEW)

PLATE 4E





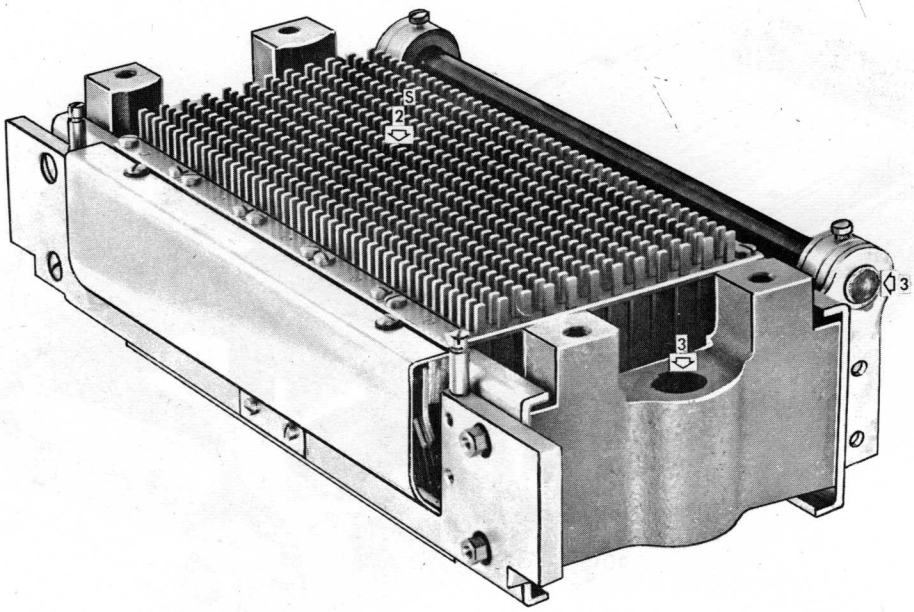
LUBRICATION CHART

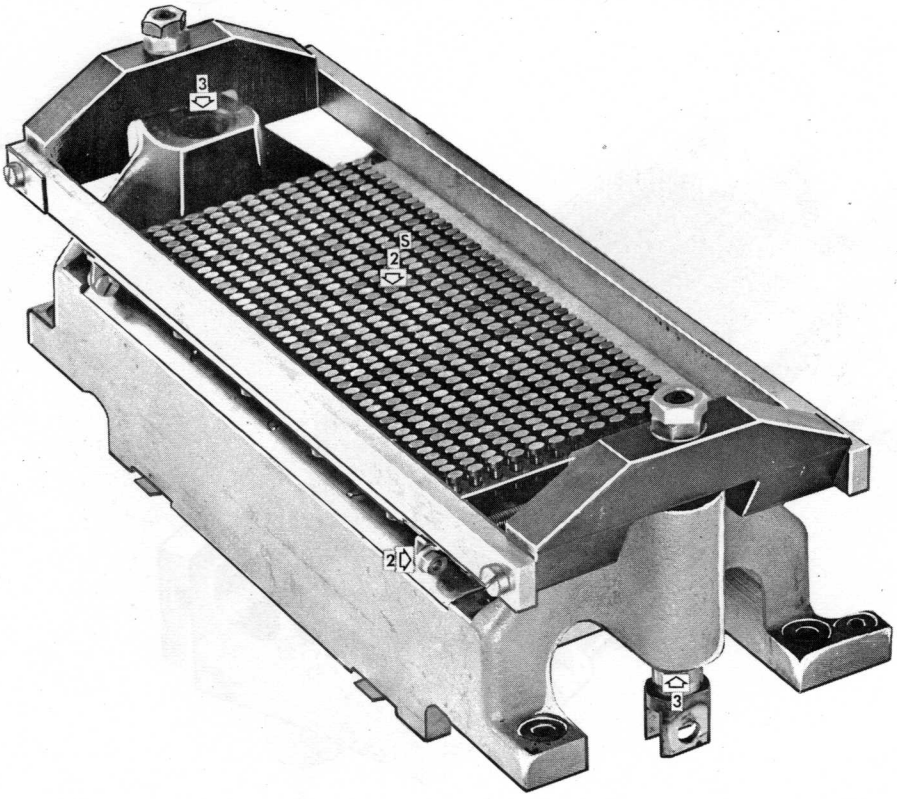
1. Velocite "E" Oil
2. White Industrial Oil
3. Medium Oil
4. Lubriplate #130AA Grease

NOTE:
(S) SPRAY with designated oil

UPPER & LOWER SENSING PIN BOX (REAR VIEW)

PLATE 5E





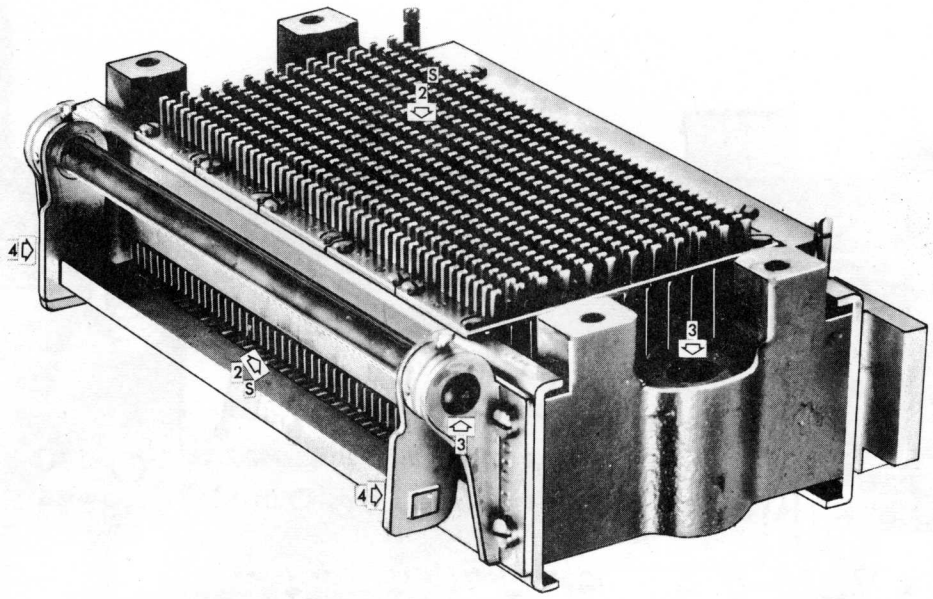
LUBRICATION CHART

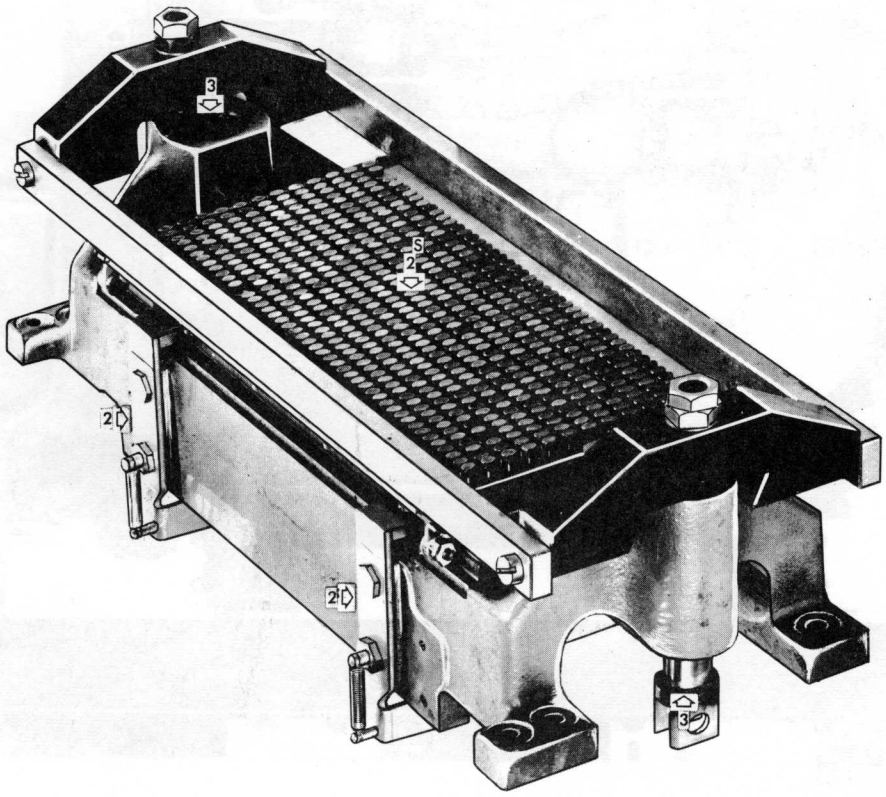
1. Velocite "E" Oil.
2. White Industrial Oil
3. Medium Oil
4. Lubriplate #130AA Grease

NOTE:
(S) SPRAY with designated oil

SET BAR SECTION & DIE SECTION (FRONT VIEW)

PLATE 6E





LUBRICATION CHART

1. Velocite "E" Oil
2. White Industrial Oil
3. Medium Oil
4. Lubriplate #130AA Grease

NOTE:
(S) SPRAY with designated oil

SET BAR SECTION & DIE SECTION (REAR VIEW)

PLATE 7E

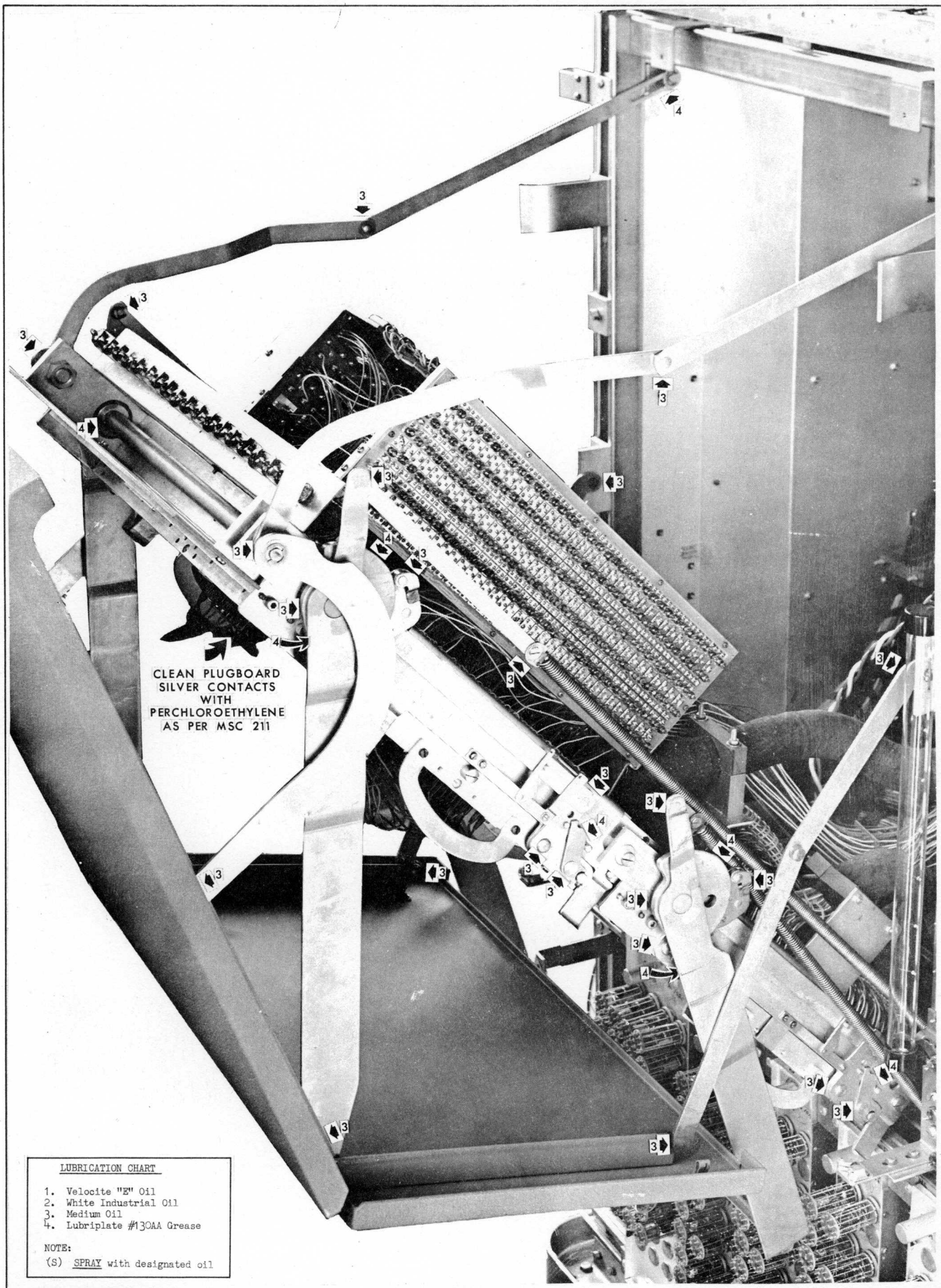
PUNCH TOWER (LEFT SIDE)

PLATE 8E

LUBRICATION CHART

1. Velocite "E" Oil
2. White Industrial Oil
3. Medium Oil
4. Lubriplate #130AA Grease

NOTE:
(S) SPRAY with designated oil

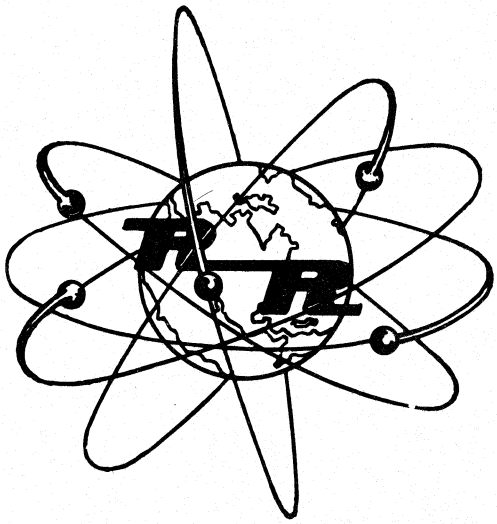


PLUGBOARD DEPRESSOR MECHANISM

PLATE 9E

ELECTRONIC COMPUTER
UNIVAC 60 & 120
SUPPLEMENT I

CONSTANT VOLTAGE
TRANSFORMER
C. V. T.



Remington Rand
DIVISION OF SPERRY RAND CORPORATION
315 FOURTH AVENUE
NEW YORK, N. Y.

F O R E W O R D

We have standardized on the use of the Sola Constant Voltage Transformer Regulator for Univac 60 & 120 Computers. The complete specifications and installation instructions for this C.V.T. Regulator are explained in the following pages.

These instructions have been prepared in sections as follows:

Section A - Description & Specifications
Section B - Service Technician Instructions
Section C - Electrical Contractor Instructions
Section D - C.V.T. Service Information
Section E - Changes Necessary when Removing C.V.T.

ELECTRONIC COMPUTER
UNIVAC 60 & 120

CONSTANT VOLTAGE TRANSFORMER

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Printed In U. S. A.
1957

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Description & Specifications for the ELECTRONIC COMPUTERS UNIVAC 60 & 120

CONSTANT VOLTAGE TRANSFORMER

SECTION A

Remington Rand
DIVISION OF SPERRY RAND CORPORATION
315 FOURTH AVENUE
NEW YORK, N. Y.

DESCRIPTION and SPECIFICATIONS

When the C.V.T. is installed, it is necessary to change the Computer Power Distribution Wiring and to install two adapters in the Computer section. These changes will be made by the Service Technician. The actual C.V.T. installation must be made by a local Electrical Contractor. The C.V.T. is connected to conform with the customer Power System specifications.

When Used:

Constant Voltage Transformers are used with Univac 60 or 120 when power input varies more than plus or minus five percent and not more than plus or minus fifteen percent of one of the listed nominal voltages; 208, 220 or 230 volts. In addition to the listed nominals, these CV Transformers may be used on nominal input voltages of 240 and 250 volts. The maximum plus tolerance voltage input is 276 volts for either of these nominals. When the 220 volt tap is employed as being closest to nominal, the lower limit of regulation is 187 volts. If the 208 volt tap is used, then the lower limit is 177 volts.

In any event, the excursions for the power line, whether steady, semi-steady, varying or transient in nature, when added together must not exceed the aformentioned limits. In the event a system varies more than 15% from nominal, additional means of regulation must be employed.

The steady and semi-steady excursions of the power line can be measured and recorded by commercial line voltage recorders of the disk type. The varying condition can be measured by roll type recorders of medium-speed paper feed. The transients can be recorded only on a fast paper feed "Brush", or equivalent, High Speed Pen Recorder. If the transients are frequent enough, they may be observed and measured on an Oscilloscope.

Electrical Circuits:

The Constant Voltage Transformer is designed for operation on a single or three phase system, referred to in "Specifications Manual" as Systems I, II, III, IV and V. It is not designed for 50 cycle operation, although it can be used as in System VI if on 60 cycles.

The C.V.T. construction is in the form of three separate single phase transformers of the resonant winding type. The primaries are for 220, 230, 240 volts on the full winding, with a tap for 208 volts operation. These primaries are connected the same as the Computer would be connected on these systems. The secondaries are connected individually to the Service Entrance Box in the right rear base of the Sensing-Punching Section. They are interconnected in the Computer Power Distribution Box as a Wye Connection with 220 volts from neutral to line. Neutral is grounded to frame ground.

Provision has been made for the C.V.T. section to be energized by a Magnetic Contactor, size 2, having a 230 volt AC coil. One side of the coil circuit is closed to the line by the Circuit Breaker on the front of the Sensing-Punching Section. This allows simple automatic control in normal machine operation sequence. Of course, the C.V.T. may be energized by a wall switch if desired for special reasons. In either case, it is necessary to push the "Start" Button on the Calculating section before the Computer is energized.

Where Located:

The C.V.T. section should be located as close to the Computer as it is practical. This will insure minimum installation cost. The working area of four feet around the Computer should not be infringed upon by this Section.

Generally speaking, the C.V.T. section should be located outside of air-conditioned spaces, and in close proximity to a window, exhaust fan, or air shaft. It may be mounted on the floor above or below that on which the Computer is located. Since the conditions change with each installation, it is necessary for the electrical wiring installation to be made by a local Electrical Contractor.

Adapters "A" & "B":-Figs. #10 & #11

Application -- All installations of the Univac 60 or 120 which have Constant Voltage Transformer Regulation for the power line will require modification of the Calculating Section.

This modification is made by the addition of two small chassis identified as Adapter "A", which mounts in the Power Control Section; and Adapter "B", which mounts in the Power Supply Section.

These Adapters are required to prevent alternating current control relays from opening during partial collapse of the Constant Voltage Transformer output voltage. This occurs when certain transformers are energized during the first few cycles of alternating current. Their function is to change the alternating current to direct current so that it may be stored for a short time, or until the voltage comes back to normal.

The control relays affected and operated by Adapter "A" are K201 (Start); K208 (-165V Surge Limit); and K215, which has been added as a filament checking relay on the "C" phase filament line. Adapter "B" operates K119 (-375V Surge Limit). These relays are now operating on approximately 80 volts direct current and have a drop out time of 125 milliseconds.

Service Technician Instructions for the ELECTRONIC COMPUTER UNIVAC 60 & 120

CONSTANT VOLTAGE TRANSFORMER

SECTION B

Remington Rand
DIVISION OF SPERRY RAND CORPORATION
315 FOURTH AVENUE
NEW YORK, N. Y.

SERVICE TECHNICIAN INSTRUCTIONS

Changes - Sensing-Punching Unit:

A. Service Entrance Box:

( ) Check each step when completed:

( ) 1. Remove Card Receiver Assembly.

( ) 2. Remove 4 Conductor Service Entrance Cable and Bracket. Fasten connectors to Service Cable Leads and retain cable with machine for future use.

( ) 3. Remove Service Entrance Box.

( ) 4. Disconnect Conduit and Straight Conduit Fitting from Service Entrance Box. Remove Straight Conduit Fitting from Conduit. Install new 90° angle Conduit Fitting #1660172 on this Conduit.

( ) 5. Drill and tap 4 new holes as shown on Fig. #3 using a #22 Drill and 10-30 tap.

( ) 6. Install new Service Entrance Box #1200587 (hinge to the right) with screws #5518 and Washer #MX6690. Install Buchanan Connector Block #1660407 with Screws #5127 and Washer #MX6690 as shown in Fig. #2. (Use washers or spacers on top fastenings to prevent breakage of Connector Block as screws are tightened. Connector Block is fragile.)

( ) 7. Install existing Conduit Cable (from Circuit Breaker) in center right side of Service Entrance Box as shown in Fig. #2.

( ) 8. Install new flexible Conduit #1660406 with 6 wires, in lower right side of Service Entrance Box as shown in Fig. #2.

NOTE: Use 6 black wires from Bundle #1701050, wires EZ coded #3 and #4, 46" length, #5 and #6, 44" length; and #7 and #8, 42" length.

( ) 9. Connect the wires to Buchanan Connector Block as shown in Fig. #4 and #5. Make new ground connection with 8" length of #10 wire from Bundle #1701050 from Buchanan Connector Terminal #1 to Service Entrance Box Mounting Screw.

( ) 10. Remove old ground connection from TB14-1 in back of Punch Circuit Breaker.

( ) 11. Install 90° angle Conduit Fitting #1660403 at lower left of Service Entrance Box as shown in Fig. #2. (This fitting will receive wires from C.V.T.).

B. Power Distribution Box - Figs. #4 and #5

( ) 1. On TB23 and TB24 make changes as in a or b to c below.

a. If machine was connected as 3 Phase Load, then remove all 3 jumpers from TB24. Move wire EZ coded #2, at TB24-8, coming from Punch Circuit Breaker to TB24-2.

b. If machine was connected as a Single Phase Load, then remove 2 jumpers; one from A2 to B2 and one from B2 to C2.

c. Connect these jumpers as follows: Connect from A1 to B1. Connect from B1 to C1.

NOTE: Extra jumper wires must be retained with machine for future use.

( ) 2. Disconnect wire on TB24-3 coming from Fuse F5 and connect to TB24-1.

( ) 3. Disconnect wire on TB24-4 coming from Fuse F6 and connect to TB24-2.

( ) 4. Disconnect wire (EZ code 1) from TB24-1 (top) and connect to TB23-4 (top).

( ) 5. Disconnect wire (EZ code 1) from TB24-1 (bottom) and connect to TB23-4 (bottom).

( ) 6. Disconnect wire (EZ code 5) from TB24-4 or TB24-5 and connect to TB24-2.

( ) 7. Disconnect wire (EZ code 6) from TB24-6 and connect to TB24-1.

( ) 8. Remove #14 brown wire (EZ code TB10-5) from side terminal of Fuse F5 and connect to TB24-5. Change wire EZ coding to read TB10-1.

( ) 9. Remove and tape #14 orange wire (EZ code TB10-3) from TB23-2. Connect a new wire (from Bundle #1701050) size #14, 10-1/2" length, from Fuse F5 side terminal to TB23-2. Remove metal jumper between TB23-2 and TB23-3.

( ) 10. Connect a new wire (from Bundle #1701050) size #14, 9-1/2" length, from TB24-6 to TB23-3.

( ) 11. Connect a new wire (from Bundle #1701050) size #14, 9-1/2" length, from TB24-7 to TB23-4.

( ) 12. Connect a new flexible Conduit (previously installed in Service Entrance Box) with a 90° angle Conduit Fitting #1660172 to lower right side of Power Distribution Box, as shown in Fig. #5.

( ) 13. Connect the 6 wires (EZ coded #3, #4, #5, #6, #7 and #8) to corresponding numbered terminals on TB24.

C. Operating Panel Terminal Board TB10 - Figs. #4 and #6

( ) 1. At TB10-3 disconnect and tape #14 orange wire (EZ coded TB23-2).

( ) 2. At TB10-4 disconnect #14 white wire (EZ coded F6-2) and connect to TB10-3.

( ) 3. At TB10-1 disconnect #14 black wire (EZ coded F3-2) and connect to TB10-4.

( ) 4. At TB10-5 disconnect #14 brown wire (EZ coded F5-2) and connect to TB10-1. (The destination of the other end of this wire is also being changed, therefore, the EZ code should now be changed to read TB24-5).

( ) 5. At TB10-7 disconnect #14 brown wire (EZ coded TB23-1) and connect to TB10-5.

NOTE: Punch Power Supply is now fused separately from motor. This allows the Punch Power Supply to be operated with the Motor "Off" by pulling out the Motor Fuse.

Changes - Electronic Calculator Unit:

A. Power Control Chassis Fuse Panel - Figs. #7 and #12

( ) 1. Remove the smaller of the side wires from Fuse F-203 (the other end of this wire is connected to Fuse F-201 rear). Connect this wire to Fuse F-204 rear. It will reach this terminal if pulled through cable sufficiently.

( ) 2. Remove wire (EZ code F-202R) from F-203R and tape well.

( ) 3. Connect new wire (from Bundle #1701050) size #14, 34-1/2" length, between F-203R and TB201-7. Follow contour of cable and secure to cable where necessary.

( ) 4. Remove lower wire from TB202-3 and tape. Connect new wire (from Bundle #1701050) size #14, 11' length, to TB202-3 lower side. Run this wire through tunnel to the Sensing-Punching Unit and connect to TB24-1 in Power Distribution Box.

(5) DISCONNECT WIRE F201R from rear of F204 & connect to rear of F202

B. Adapter "A" - Figs. #8 and #12

( ) 1. Remove cover screen below Program Test Panel.

( ) 2. Loosen 2 top Regulator Chassis Phillip Mounting Screws and mount Adapter "A" (#1701053) behind flange of Chassis. Tighten screws.

( ) 3. Remove wire from TB203-5 left side and splice to 4" extension wire connected to TB203A-7.

( ) 4. Remove wire from TB203-3 and connect to TB203A-6.

( ) 5. Connect orange wire, coming from Rectifier CR205 in Adapter "A" to TB203-3.

( ) 6. Connect the 8" wire, connected to TB203A-8, to TB203-8 right side.

( ) 7. Disconnect wire connected to Relay K205 terminal #8 (top normally open contact) and splice to 5" extension wire coming from TB203A-4.

( ) 8. Connect 11" extension wire coming from TB203A-5 to Relay K205 terminal 8.

( ) 9. Connect upper end of red wire on Adapter "A" Cable to TB203-5.

( ) 10. Run cable coming from Adapter "A" down between Timer and Regulator and to the left rear of the RCS Chassis. The shortest section goes out to the meter panel. The orange wire coming from TB203A-3, connects to TB206-5. The red wire, coming from TB203-5, connects to TB206-6. The remaining cable section is run down to the -165 Chassis and terminates on TB207. The green wire, coming from TB203A-1, connects to TB207-1. The yellow wire coming from TB203A-2 connects to TB207-3. Tape or tie cable to existing cables where necessary.

( ) 11. Disconnect wire coded #227 connected to TB207-3 (inside); splice 5" extension wire to wire #227 and connect to TB207-1.

( ) 12. Replace cover screen and check for adequate clearance between Adapter "A" and screen.

C. Adapter "B" - Fig. #9

( ) 1. Mount Adapter "B" #1701054, with attached cable, in Power Supply Chassis under Choke L-22 by loosening Lower 1/4-20 mounting screws of L-22 and sliding Chassis between L-22 feed and the flat washers.

( ) 2. Remove two terminal screws, on right side of TB110-5 and TB110-7, located opposite C1-220 and 1-115.

( ) 3. Mount new Terminal Board TB110-A on these two terminals using the jumper strips provided. Replace the wires removed in step 2 on top of the strips.

( ) 4. Remove wire coded #79 from TB110-6 (C2) and connect it to TB110A-2 (center terminal).

( ) 5. Connect third wire of new cable (C2) to TB110-6 opposite wire coded #85.

D. Bottom Rear Cover - Fig. #13

( ) 1. A section of the cover must be cut out, as shown in the Fig. #11, to provide power cable clearance.

( ) 2. An 8" piece of insulation #6860-8-76310400 is inserted over the cut surface to protect the power cable.

Parts Ordering:

The C.V.T. and necessary parts are not available on the Standard Factory Parts Order. These items must be ordered through the Sales Department on the regular Sales Order.

Electrical Contractor Instructions for the ELECTRONIC COMPUTERS UNIVAC 60 & 120

CONSTANT VOLTAGE TRANSFORMER

SECTION C

Remington Rand
DIVISION OF SPERRY RAND CORPORATION
315 FOURTH AVENUE
NEW YORK, N. Y.

ELECTRICAL CONTRACTOR INSTRUCTIONS

The C.V.T. section should be located as close to the Computer as is practical. This will insure minimum installation cost. The working area of four feet around the Computer should not be infringed upon by this section (see Fig. #17).

Generally speaking, the C.V.T. section should be located outside of air-conditioned spaces, and in close proximity to a window, exhaust fan, or air shaft. It may be mounted on the floor above or below that on which the Computer is located. Since the conditions change with each installation, it is necessary for the Electrical Wiring installation to be made by a local Electrical Contractor.

The C.V.T. is designed for operation on a Single or Three Phase System referred to in Fig. #14 as Systems I, II, III, IV and V. It is not designed for 50 cycle operation, although it can be used as in Systems VI if on 60 cycles.

Provision has been made for the C.V.T. section to be energized by a Magnetic Contactor, size 2, having a 230 volt AC coil. One side of the coil circuit is closed to the line by the circuit breaker on the front of the Sensing-Punching Section. This allows simple automatic control in normal machine operation sequence. Of course, the C.V.T. may be energized by a wall switch if desired for special reasons.

C.V.T. Specifications:

Output rating:	300 volt-amperes, each section. Total 9KVA.
Output voltage:	220 volts, single phase, each section.
(A) Input voltage:	240 volt primary with tap at 208 volts, each section.
Frequency:	60 cycles.
Surge:	Load starting surge 25 amperes, each section. Additional random surge up to 75 amperes maximum for one half cycle.
Load power factor:	95% inductive, each section.
Regulation:	Output $\pm$ 1% with input variations of 30% and load variations from 66 to 100%. No-load voltage and voltage at loads under 66% may be + or - 5%. The input variations of 30% should be as close as possible to + or - 15% of the input nominal. Correction must be made within two cycles.
Harmonic content:	Not more than 3% total harmonic content from 66% load to full load for each section.
Terminals:	Pressure - screw type, clearly marked "Primary", "Secondary", and tape voltages, to receive AWG #4 max.
Ambient:	40°C. Rise 60° maximum.
Dimensions:	Height - 47 inches; Width - 24 inches; Length - 28 inches; Weight 1228 lbs.
Heat Dissipation:	Variable, max. estimated 6800 BTU/HR.

Sola C.V.T. Service Information for the ELECTRONIC COMPUTER UNIVAC 60 & 120

CONSTANT VOLTAGE TRANSFORMER

SECTION D

Remington Rand
DIVISION OF SPERRY RAND CORPORATION
315 FOURTH AVENUE
NEW YORK, N. Y.

SOLA C.V.T. SERVICE INFORMATION

SAFETY NOTICE:

THIS EQUIPMENT EMPLOYS VOLTAGES WHICH ARE DANGEROUS AND MAY BE FATAL IF CONTACTED. EXTREME CAUTION SHOULD BE EXERCISED WHEN WORKING WITH THE C.V.T. DO NOT TOUCH ANY INTERNAL CONNECTIONS WHILE PRIMARY CIRCUIT IS ENERGIZED. OPERATING VOLTAGE AT CAPACITOR TERMINALS IS APPROXIMATELY 700 VOLTS. ALWAYS REMOVE POWER BEFORE ATTEMPTING ANY MAINTENANCE.

No Routine Maintenance Necessary:

Since the C.V.T. is a simple rugged device without moving parts or manual adjustments, no "Service" or "Maintenance" is needed in the ordinary sense; and the per cent of possible poor performance or failure is exceedingly low. In any case of apparent poor performances, the user is urged to check the following points immediately:

Check List of Factors Effecting Performance:

Checking with Voltmeters: All checks on the AC output voltage of the C.V.T. should be made with a Dynamometer type Voltmeter. A certain amount of harmonics in the output may cause other types (particularly Rectifier types) to give inaccurate readings; for instance: Some Vacuum Tube Voltmeters, Multi-Meters, etc., may read as much as 8% high on Sola RMS output of 115 volts.

1. Probable Trouble -- If the output voltage is too low and it has been established that the unit is not overloaded and that the load power factor is correct, either a defective Capacitor or Transformer Winding is indicated. A defective Capacitor is the most likely trouble. To check, proceed as follows:

   De-energize the C.V.T. and remove the C.V.T. front cover as shown in Fig. #16. Disconnect the load and connect a 0-300 Volt AC Voltmeter across the output terminals. Re-energize the C.V.T. and check meter reading. If meter reads about 20 volts, a shorted Capacitor is indicated. If the meter reads a little below the normal value voltage, an open capacitor or a damaged transformer winding may be the cause of trouble.

2. Capacitor Short Test -- To determine which Capacitor is shorted, de-energize the C.V.T. and disconnect Capacitor C-1 by removing 1 terminal connection. Energize the C.V.T. and check the meter reading. If output voltage does not rise to approximately normal value, de-energize the C.V.T., re-connect C-1 and disconnect C-2. Continue with each succeeding Capacitor until voltage does rise to near the rated value.

   REMEMBER TO DE-ENERGIZE EQUIPMENT BEFORE CONNECTING OR DIS-CONNECTING ANY CAPACITOR.

3. Capacitor Open Test -- To determine whether a Capacitor is open or a Transformer winding is damaged, a new Capacitor having approximately the same capacity and voltage rating must be connected in parallel with the existing Capacitors. If one Capacitor is open, adding a new Capacitor in parallel will bring the voltmeter reading to a normal value. If the meter reading does not return to approximately normal value, a damaged Transformer Winding is indicated. To determine which Capacitor is open, de-energize the C.V.T. and disconnect C-1. Energize the C.V.T. If reading of voltage meter drops somewhat below normal value, de-energize the C.V.T., re-connect C-1 and disconnect C-2. Continue with the

other Capacitors until voltage reading of meter does not drop.

4. Damaged Transformer Winding -- If all checks indicate a damaged Transformer Winding, the C.V.T. must be returned to the factory for repair. If after two Capacitors have been replaced, a third Capacitor becomes defective, the entire unit should also be returned to the factory to be repaired. Since the total capacitance is matched to the coils, replacing more than 1 or 2 Capacitors with Capacitors of only approximate value may cause improper functioning of the Voltage Regulator.

5. Output Voltage Too High:

   a. Load may be considerably less than normal.

   b. Load may have leading power factor.

   c. Line frequency high.

6. Output Voltage Too Low:

   a. Unit may be overloaded.

   b. Primary voltage below 190 volts.

   c. Line frequency low.

   d. Defective Transformer Winding.

   e. Defective Capacitor.

7. No Output Voltage:

   a. Open terminal connection.

   b. Open Primary or Secondary Transformer Winding.

GUARANTEE

Sola Constant Voltage Transformers are guaranteed against failure due to faulty materials or workmanship for a period of one year from date of sale.

LIST OF SOLA ELECTRIC CO. REPRESENTATIVES

SOLA ELECTRIC CO.
Plant & General Offices
4633 West 16th Street
Chicago 50, Illinois

ATLANTA 5, Georgia
James Millar Associates
1036 W. Peachtree St. NE

BOSTON, Massachusetts
Sola Electric Co.
272 Centre St.
Newton 58, Massachusetts

BUFFALO 3, New York
R.W. Mitscher
487 Ellicot Square Bldg.

CHARLOTTE 2, North Carolina
Ranson, Wallace & Co.
116-1/2 E. Fourth St.

CLEVELAND 15, Ohio
Sola Electric Co.
1836 Euclid Avenue

DALLAS, Texas
J. B. Stuart
4401 Caruth St.

DENVER 4, Colorado
Slaybough & Thompson
100 W. 13th Avenue

KANSAS CITY 2, Missouri
Sola Electric Co.
406 West 34th St.

LOS ANGELES 27, California
Edward S. Sievers
1662 Hillhurst Avenue

NEW YORK 35, New York
Sola Electric Co.
103 E. 125 St.

PHILADELPHIA, Pennsylvania
Sola Electric Co.
Commercial Trust Building
15th & Market Streets

PITTSBURGH 18, Pennsylvania
Burke Electrical Equipment Co.
416 Maple Avenue

PORTLAND 10, Oregon
Marshall B. James
2941 NW Quimby St.

SAN FRANCISCO, California
Joseph M. Smith
3625 South Grand Avenue
Los Angeles 7, California

SEATTLE 4, Washington
Northwestern Agencies
4130 First Avenue, South

Changes Necessary When Removing the CONSTANT VOLTAGE TRANSFORMER

ELECTRONIC COMPUTERS

UNIVAC 60 & 120

SECTION E

Remington Rand
DIVISION OF SPERRY RAND CORPORATION
315 FOURTH AVENUE
NEW YORK, N. Y.

CHANGES NECESSARY WHEN REMOVING C.V.T.

General:

1. In the event a Computer having a Constant Voltage Transformer is re-shipped to an installation not requiring the Transformer, certain changes are necessary, but not all of the original changes.

2. The Calculating Section will operate with Adapters A and B, regardless of whether or not there is a regulator of any type on the input line.

   They should not be removed once installed, for they tend to improve the reliability of the control relays concerned. In addition, there is a "C Line" filament failure check circuit incorporated which is of possible benefit.

Electronic Calculating Unit:

There are no changes to be made in this section.

Sensing-Punching Unit:

Changes in this section are confined to those which are absolutely necessary as follows:

A. Power Distribution Box

( ) 1. Wire coming from TB202-3 in Computer, now on TB24-1 (D-1), is disconnected and re-connected to TB24-3 (A-1).

( ) 2. Wire coming from TB201-7 in Computer, now on TB24-2 (EZ coded 2), is disconnected and re-connected to TB24-4 (A-2).

( ) 3. Wire coming from Fuse F-5 is disconnected from TB24-1 (D-1) and is re-connected to TB24-3 (A-1).

( ) 4. Wire coming from Fuse F-6 is disconnected from TB24-2 (D-2) and is re-connected to TB24-4 (A-2).

( ) 5. Remove Jumper between TB24-7 (C-1) and TB23-4 (ground). Retain this Jumper in machine for future use.

6. Three of the four AWG #8 wires coming from the Punch Unit Circuit Breaker and TB14 are now connected in the normal manner for the Power System employed. If Single Phase System is employed, make connections as in (a) below. If Three Phase System is employed, make connections as in (b) below.

   a. Single Phase - Fig. #18

( ) 1. Disconnect wire (EZ coded #5) from TB24-2 and re-connect to TB24-5.

( ) 2. Disconnect wire (EZ coded #6) from TB24-1 and re-connect to TB24-6.

( ) 3. Connect jumper wires between TB24-4 (A2), TB24-6 (B2), and TB24-8 (C2).

   Wire EZ coded #1 remains on TB23-4 ground.

b. Three Phase - Fig. #19

( ) 1. Disconnect wire (EZ coded #5) from TB24-2 and re-connect to TB24-4 or 5.

( ) 2. Disconnect wire (EZ coded #6) from TB24-1 and re-connect to TB24-6.

( ) 3. Disconnect wire (EZ coded #2) from TB24-2 and re-connect to TB24-8.

( ) 4. Disconnect jumper wires between TB24-3 (A1), TB24-5 (B1) and TB24-7 (C1).

( ) 5. Connect jumper wire between TB24-3 (A1) and TB24-8 (C2).

( ) 6. Connect jumper wire between TB24-4 (A2), and TB24-5 (B1).

( ) 7. Connect jumper wire between TB24-6 (B2) and TB24-7 (C1).

Wire EZ coded #1 remains on TB23-4 ground.

B. Service Entrance Box

At the Service Entrance Box, the AWG #8 wires are terminated at Buchanan Block Terminals #9 (D1), #10 (D2), #1 (Ground) and #2 (D2C).

1. Terminal #9 (D1) becomes line A. (Red wire)

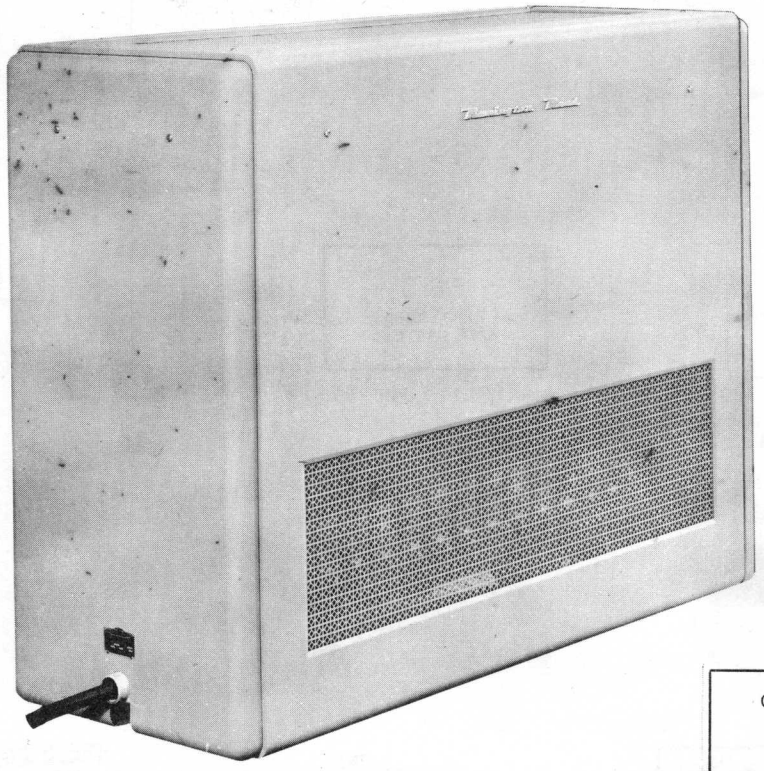
2. Terminal #10 (D2) becomes line B. (Black wire)

3. Terminal #2 (D2C) becomes line C, used in both three phase systems. (White wire)

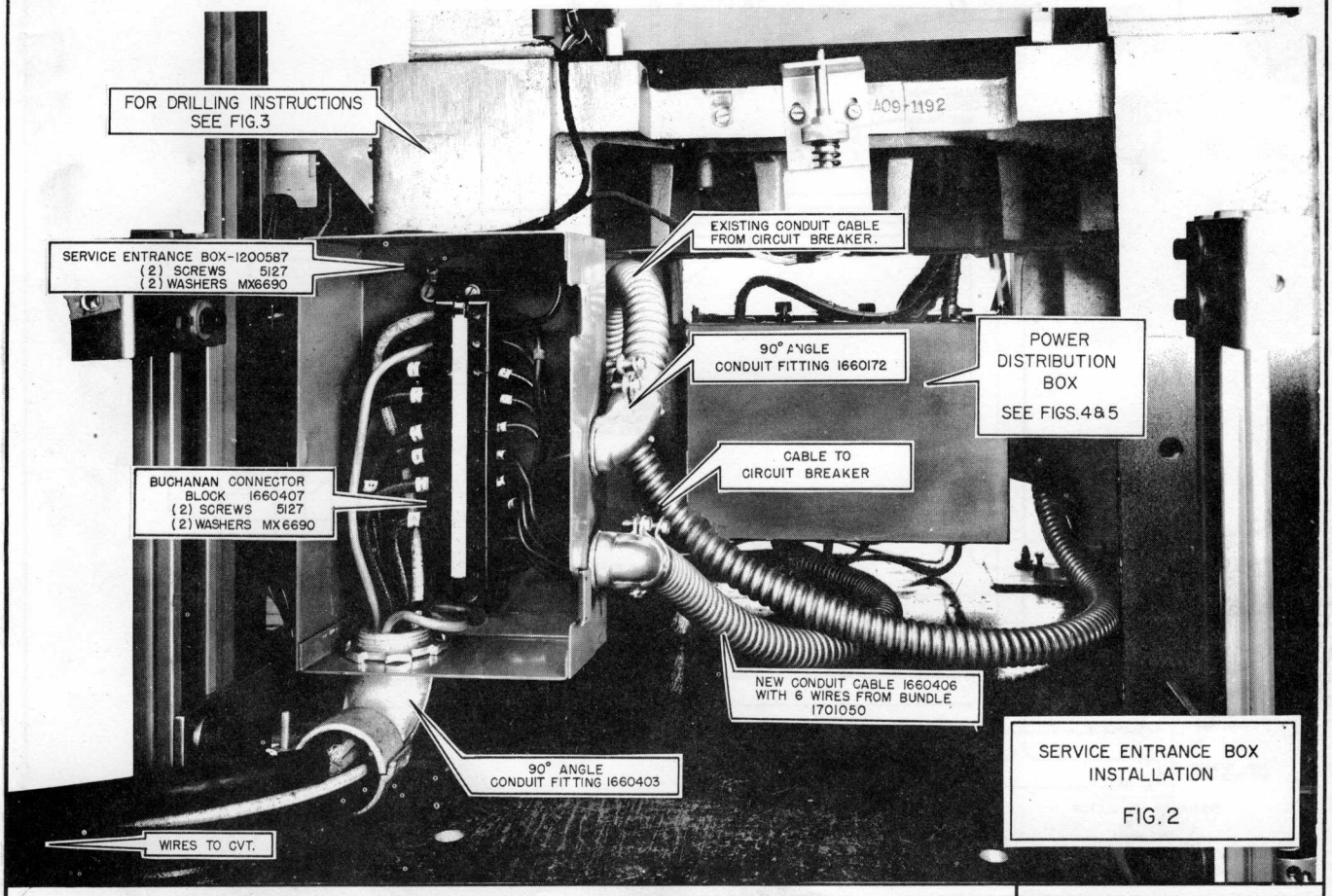
4. Three Phase Circuit Breaker would, of course, be required as in standard Three Phase connection.

5. Terminals #3, #4, #5, #6, #7 and #8 are left as is, connected only to TB24 identical terminals.

Four wire power cable now may be connected using standard entrance bracket and clamp or going through opening in left side cover. It should enter Service Entrance Box through 1-1/4" hole in bottom by use of reducing washers, or may be passed through 1-1/4" right angle conduit clamp.



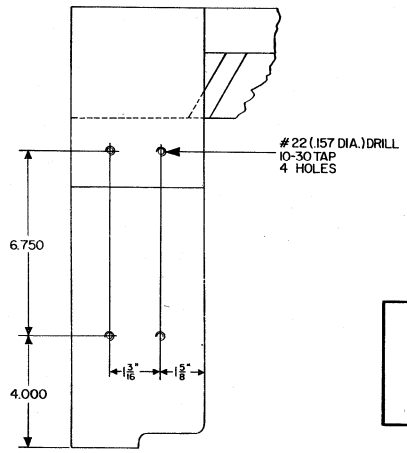
CONSTANT VOLTAGE
TRANSFORMER
•CVT• ASSEMBLY
FIG. 1



SERVICE ENTRANCE BOX
INSTALLATION
FIG. 2

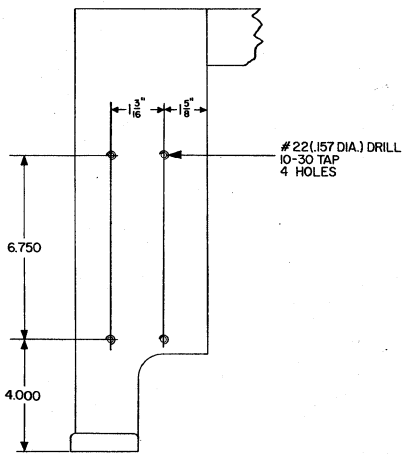
CONSTANT VOLTAGE TRANSFORMER INSTALLATION

PLATE 1



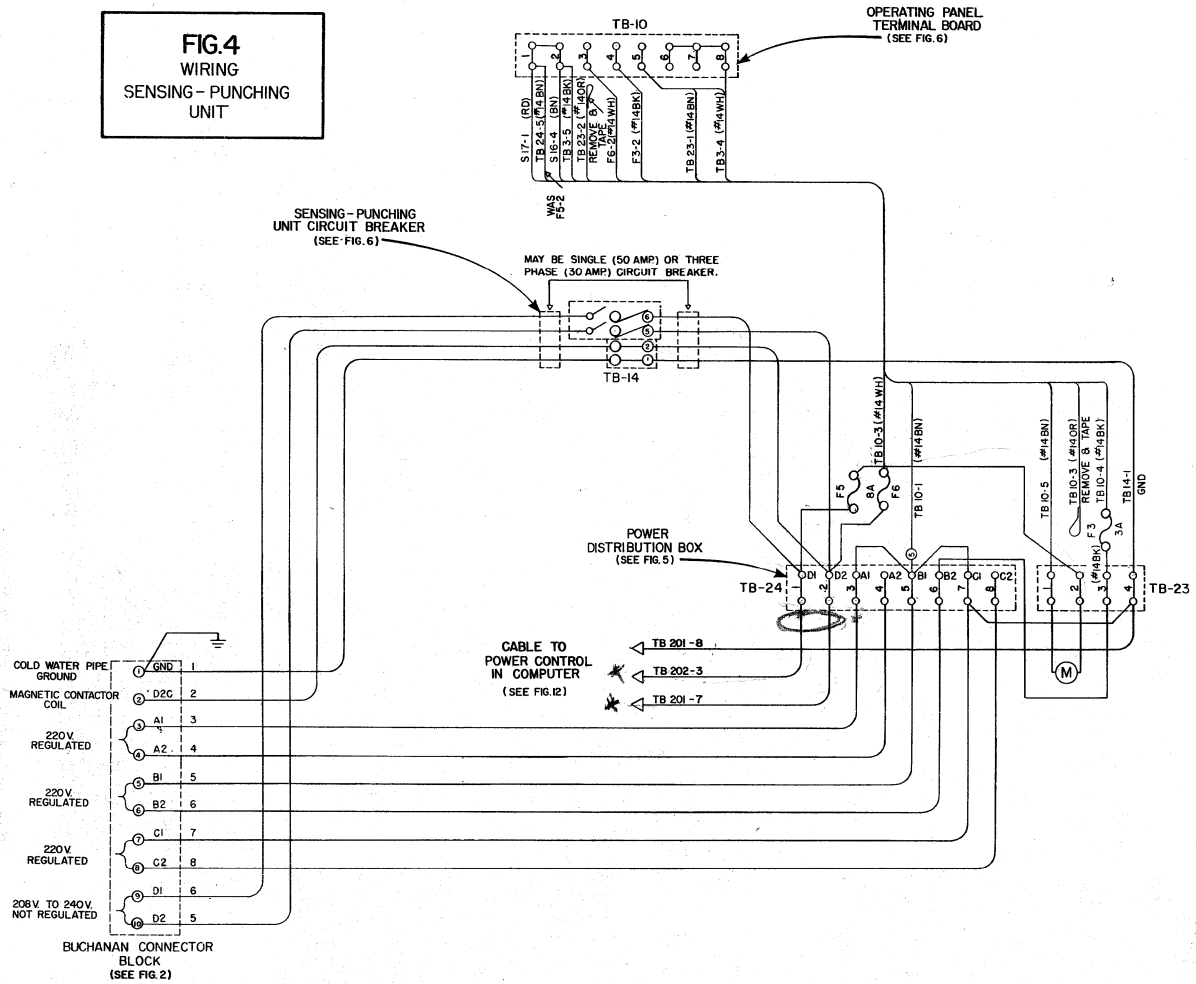
TWO SECTION BASE

FIG. 3
LEFT REAR BASE CASTING



SINGLE SECTION BASE

FIG.4
WIRING
SENSING - PUNCHING UNIT



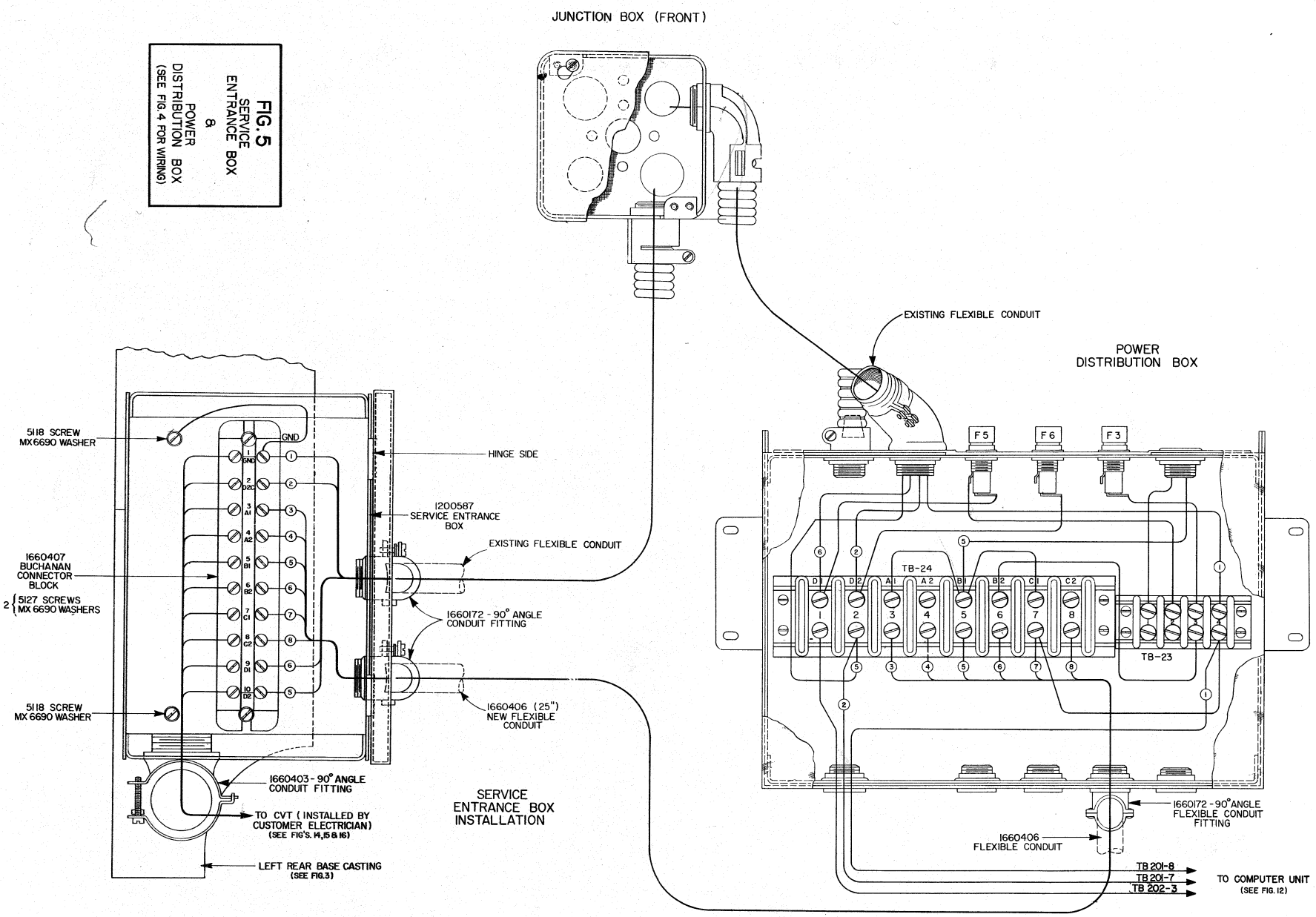
CONSTANT VOLTAGE TRANSFORMER INSTALLATION

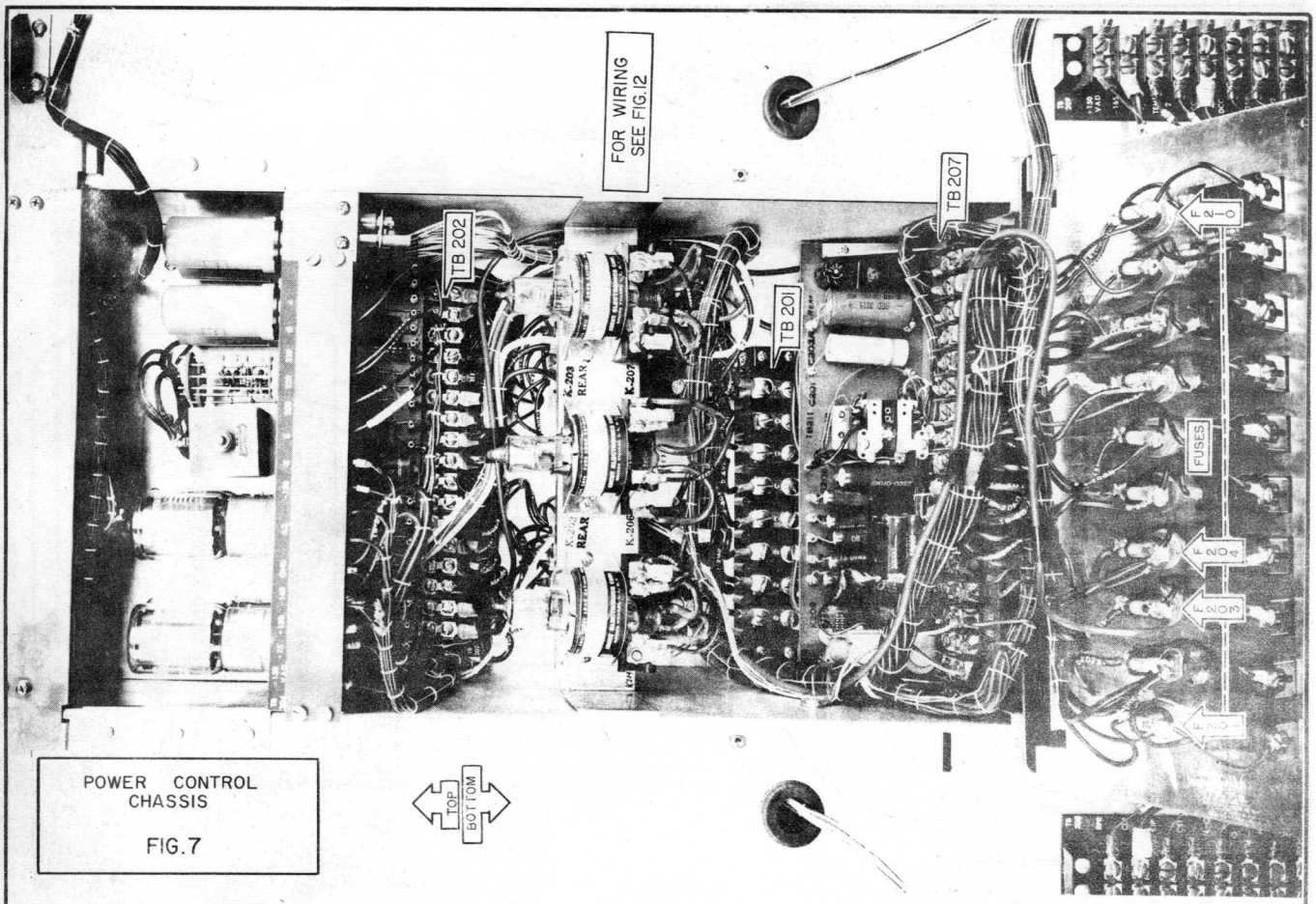
PLATE 2

CONSTANT VOLTAGE TRANSFORMER INSTALLATION

PLATE 3

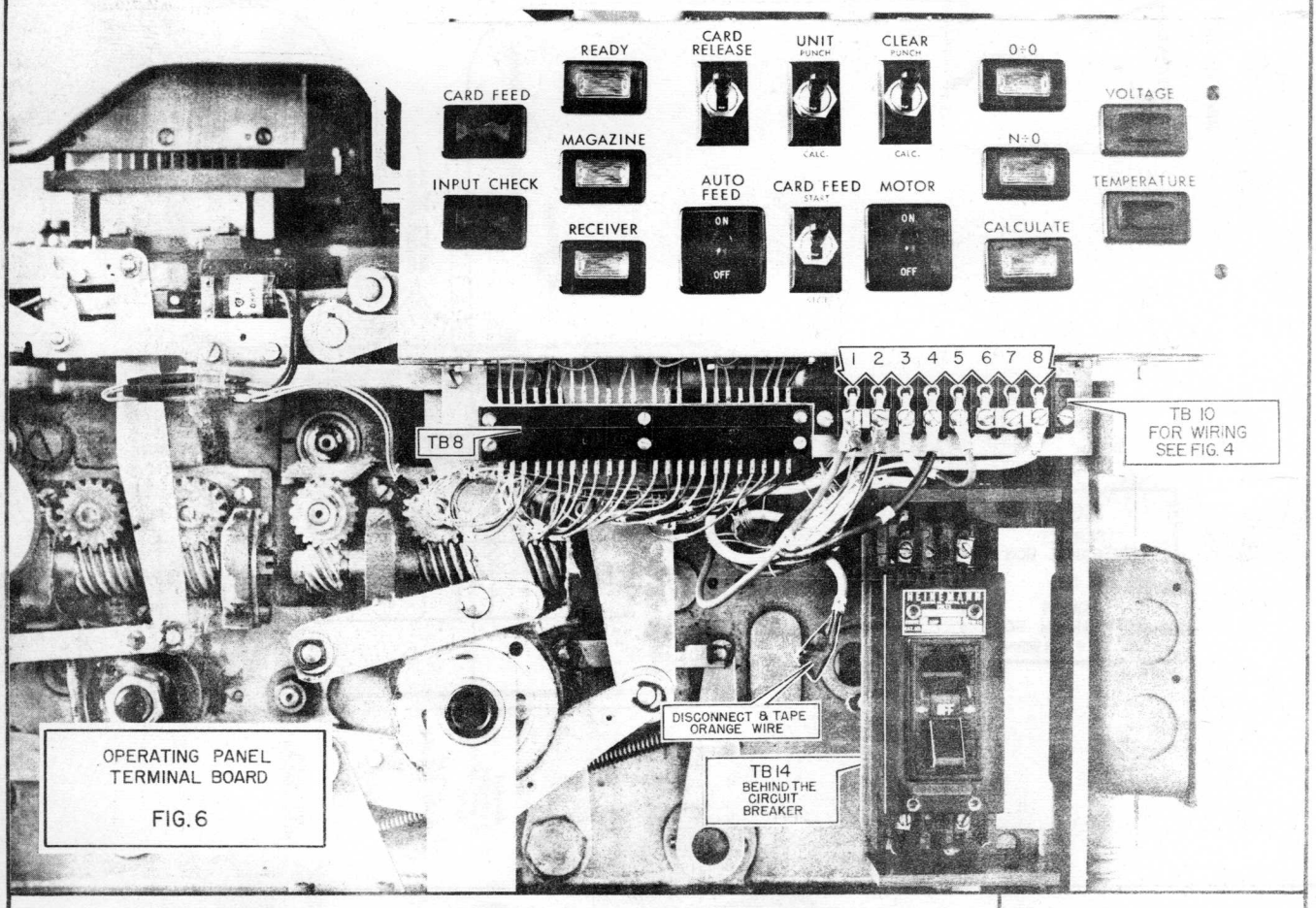
FIG. 5
SERVICE ENTRANCE BOX
&
POWER DISTRIBUTION BOX
(SEE FIG. 4 FOR WIRING)





POWER CONTROL CHASSIS

FIG.7

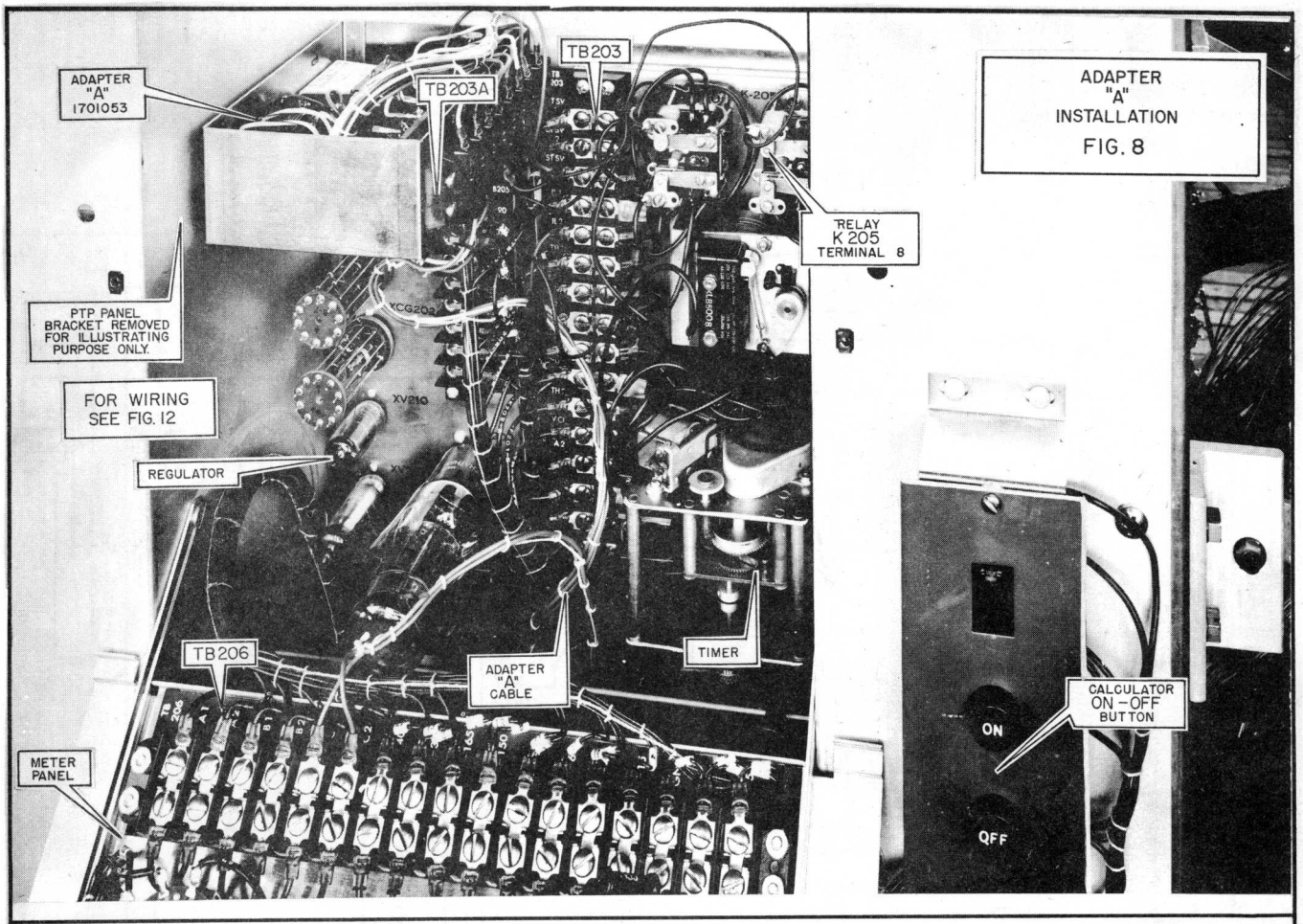


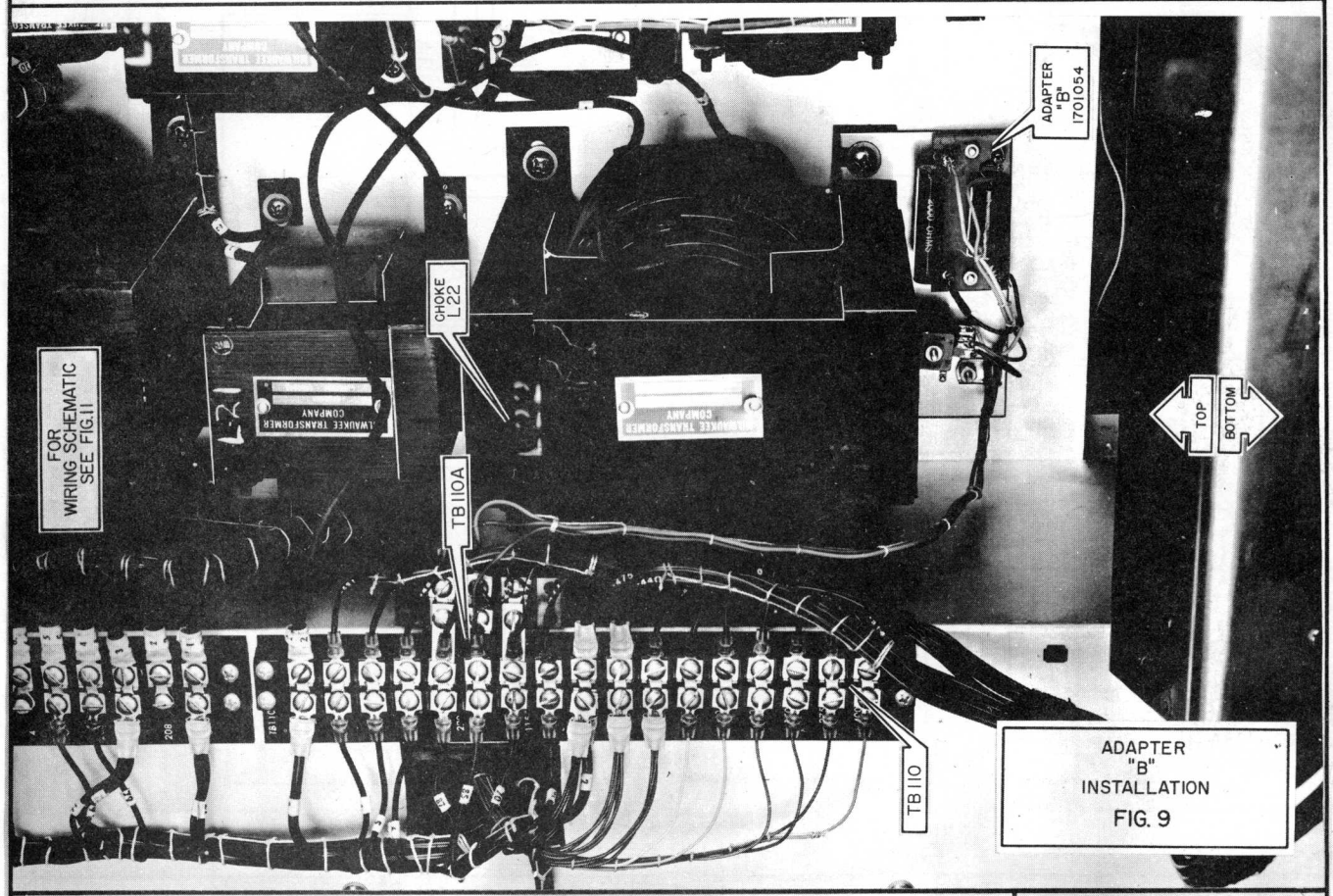
OPERATING PANEL TERMINAL BOARD

FIG.6

CONSTANT VOLTAGE TRANSFORMER INSTALLATION

PLATE 4





CONSTANT VOLTAGE TRANSFORMER INSTALLATION

PLATE 5

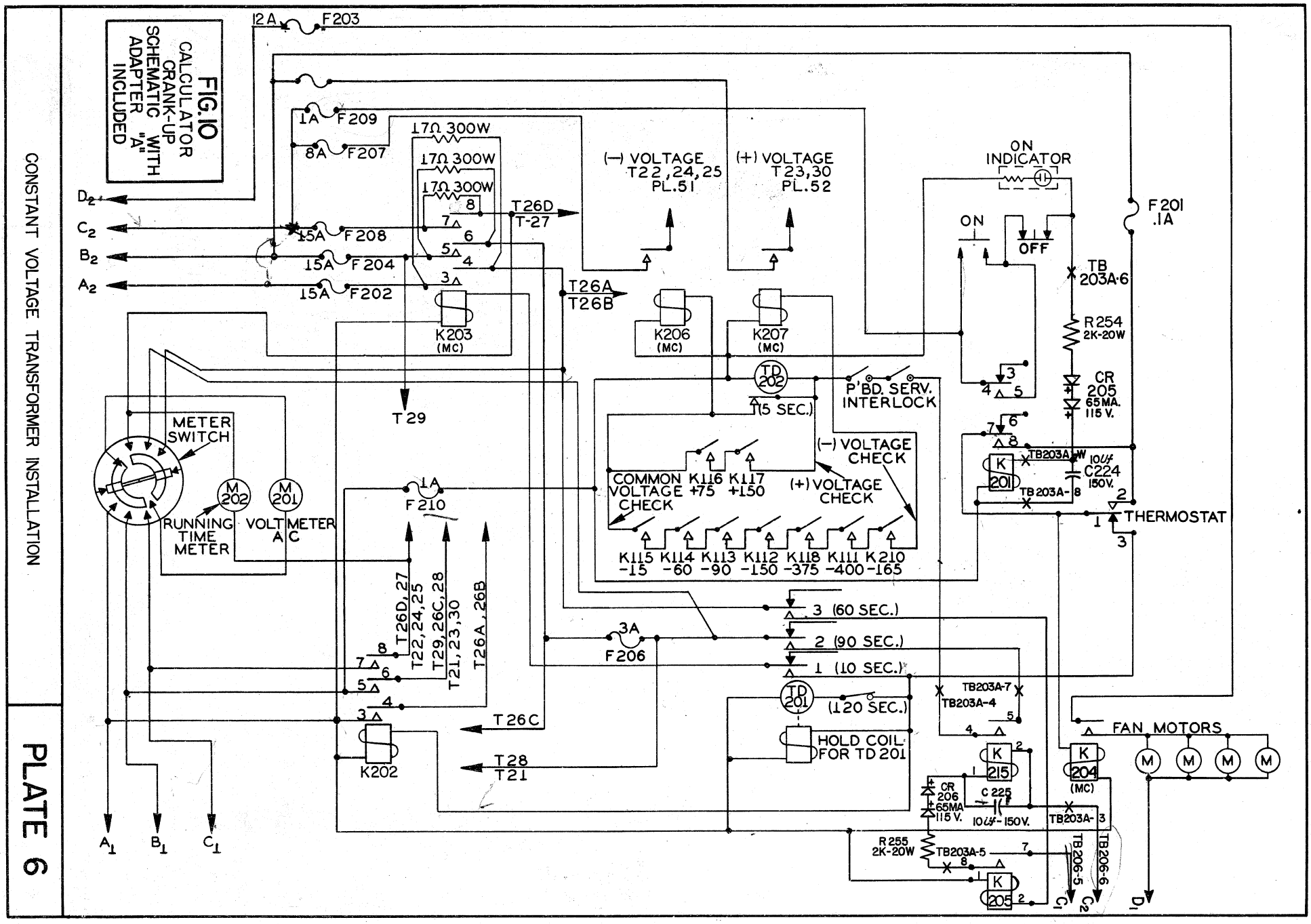


FIG. 10
CALCULATOR CRANK-UP SCHEMATIC WITH "A" ADAPTER INCLUDED
CONSTANT VOLTAGE TRANSFORMER INSTALLATION
PLATE 6
12A F203
1A F209
8A F207
17Ω 300W
17Ω 300W
17Ω 300W
D2
C2
B2
A2
15A F208
15A F204
15A F202
T26D T-27
T26A T26B
K203 (MC)
K206 (MC)
K207 (MC)
(−) VOLTAGE T22,24,25 PL.51
(+) VOLTAGE T23,30 PL.52
ON INDICATOR
ON
OFF
F201 .1A
TB 203A-6
R254 2K-20W
CR 205 65MA. 115 V.
TD 202
(15 SEC.)
P'BD. SERV. INTERLOCK
T29
METER SWITCH
M 202
M 201
RUNNING TIME METER
VOLT METER A C
1A F210
COMMON VOLTAGE CHECK
K116 +75
K117 +150
(−) VOLTAGE CHECK
(+) VOLTAGE CHECK
K115 -15
K114 -60
K113 -90
K112 -150
K118 -375
K111 -400
K210 -165
TB203A-W
10μf C224 150V.
TB 203A-8
K 201
THERMOSTAT
T26D,27 T22,24,25
T29,26C,28 T21,23,30
T26A,26B
3A F206
3 (60 SEC.)
2 (90 SEC.)
1 (10 SEC.)
TD 201
(120 SEC.)
HOLD COIL FOR TD 201
TB203A-7
TB203A-4
T26C
T28 T21
K202
K 215
K 204 (MC)
FAN MOTORS
M M M M
CR 206 65MA 115 V.
C 225 10μf-150V.
TB203A-3
R 255 2K-20W
TB203A-5
TB206-5
TB206-6
K 205
A1 B1 C1
C1 C2 D1

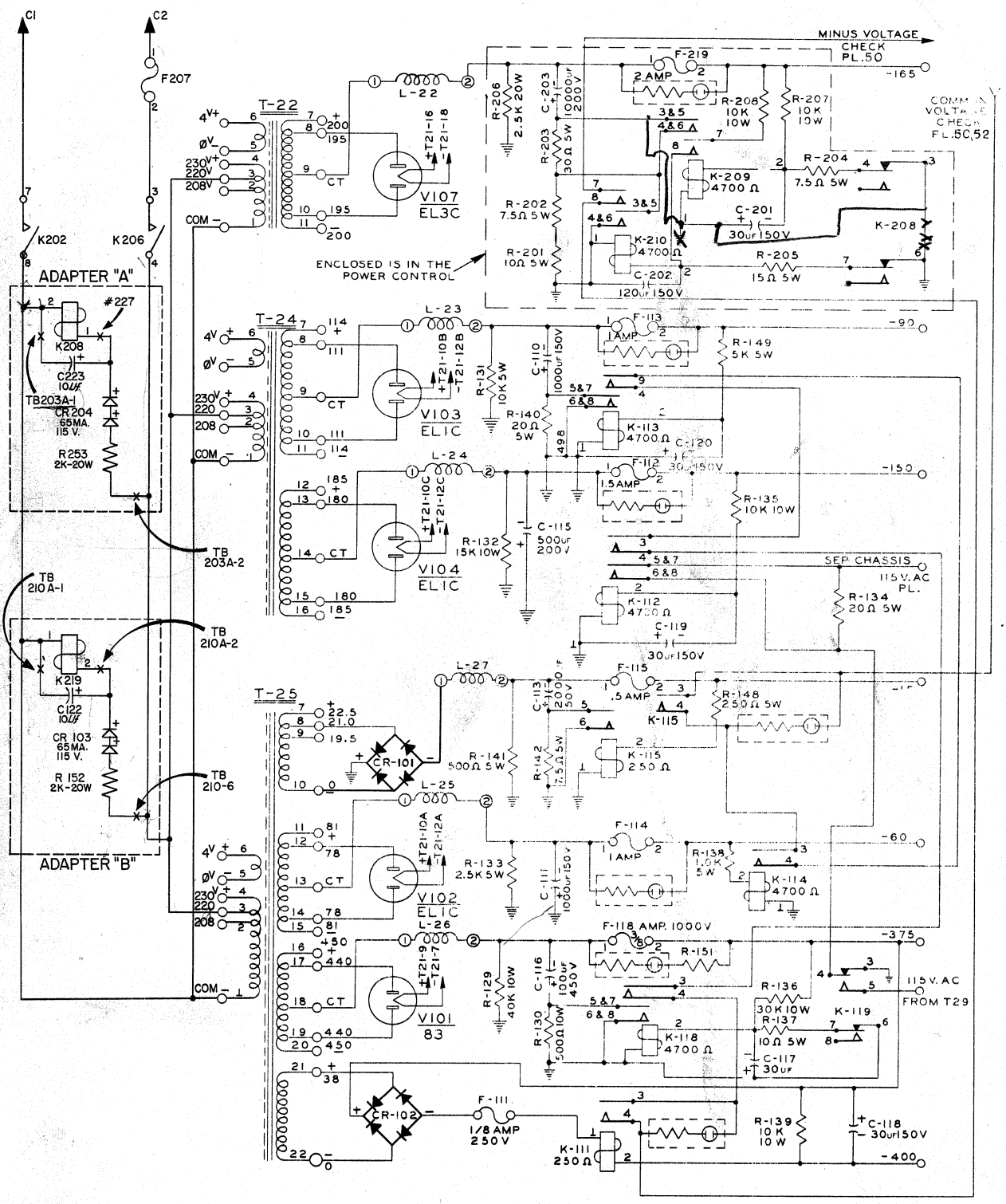


FIG. 11
POWER SUPPLY MINUS - VOLTAGES WITH ADAPTER A & B INCLUDED.

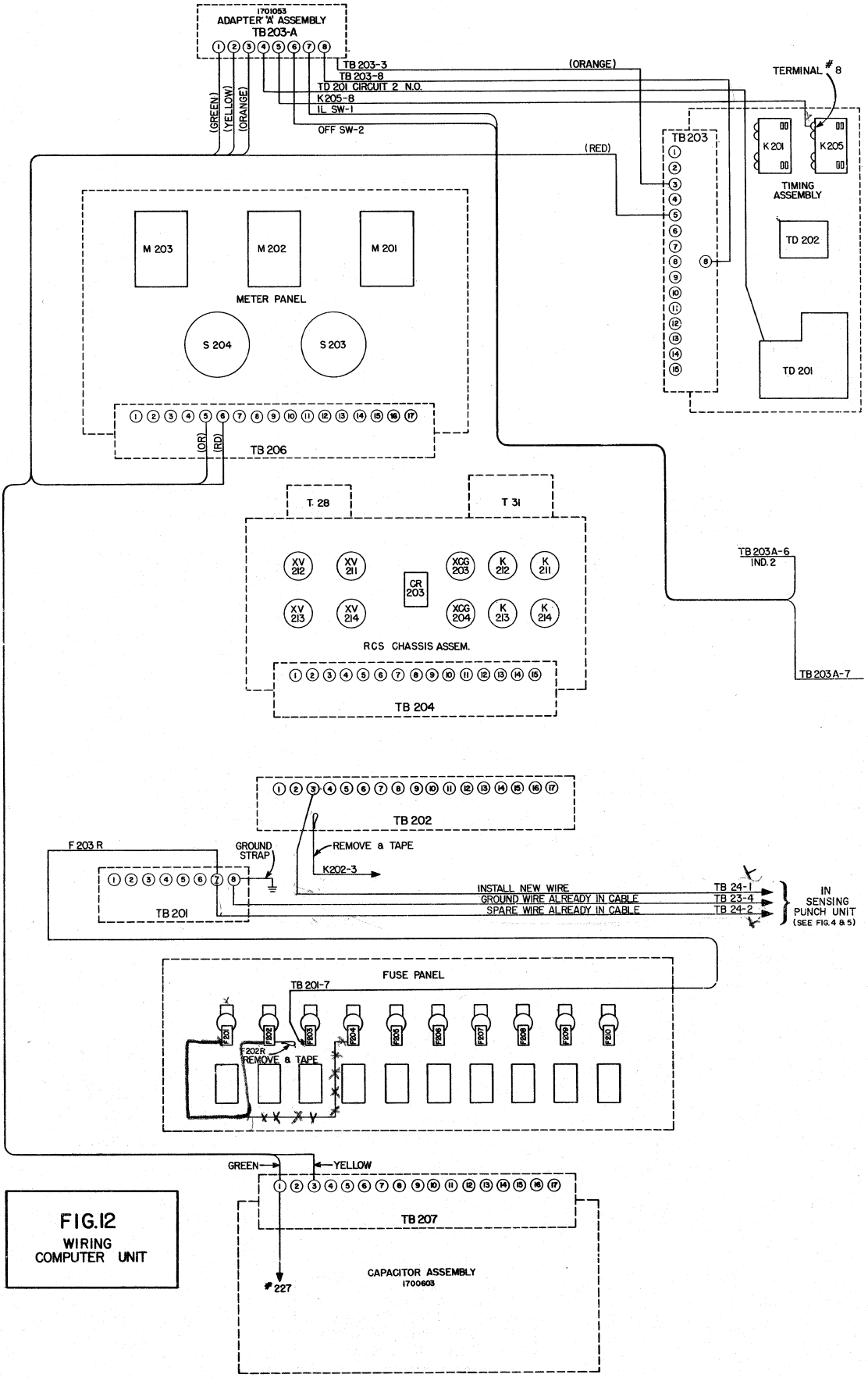


FIG.12
WIRING
COMPUTER UNIT

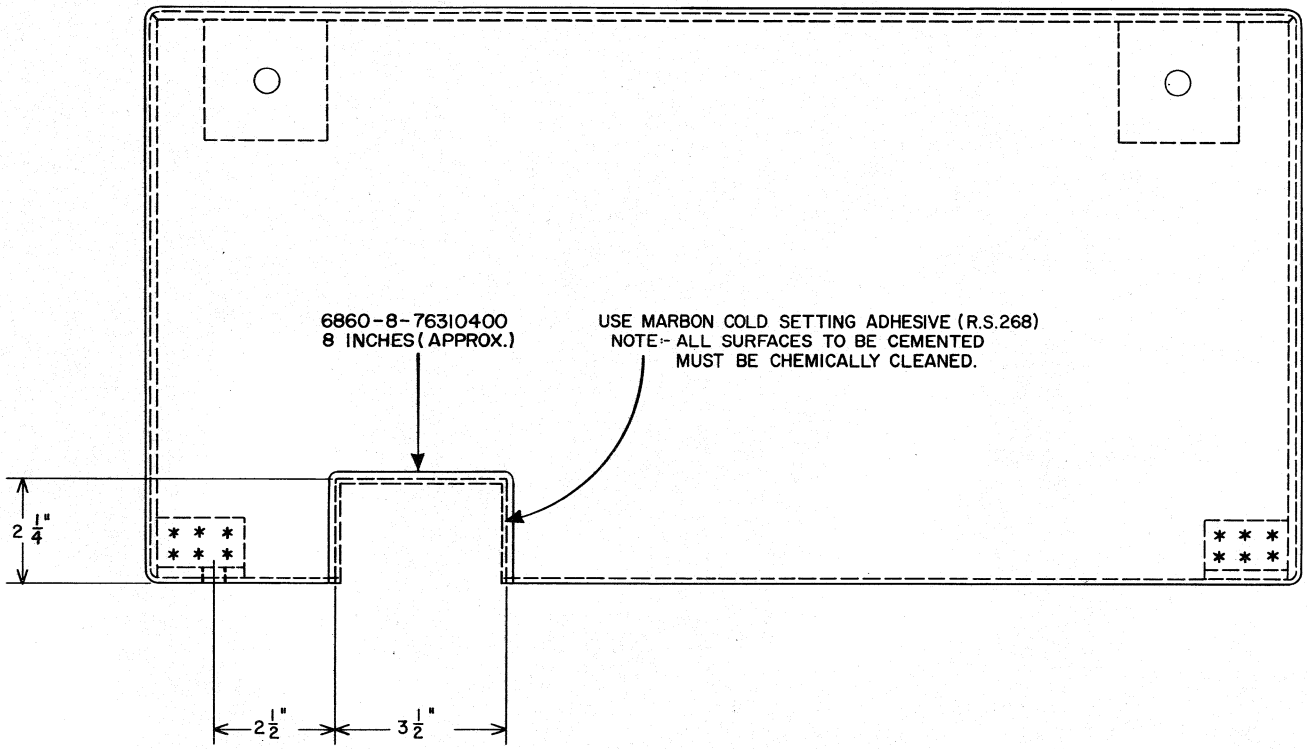
CONSTANT VOLTAGE TRANSFORMER INSTALLATION

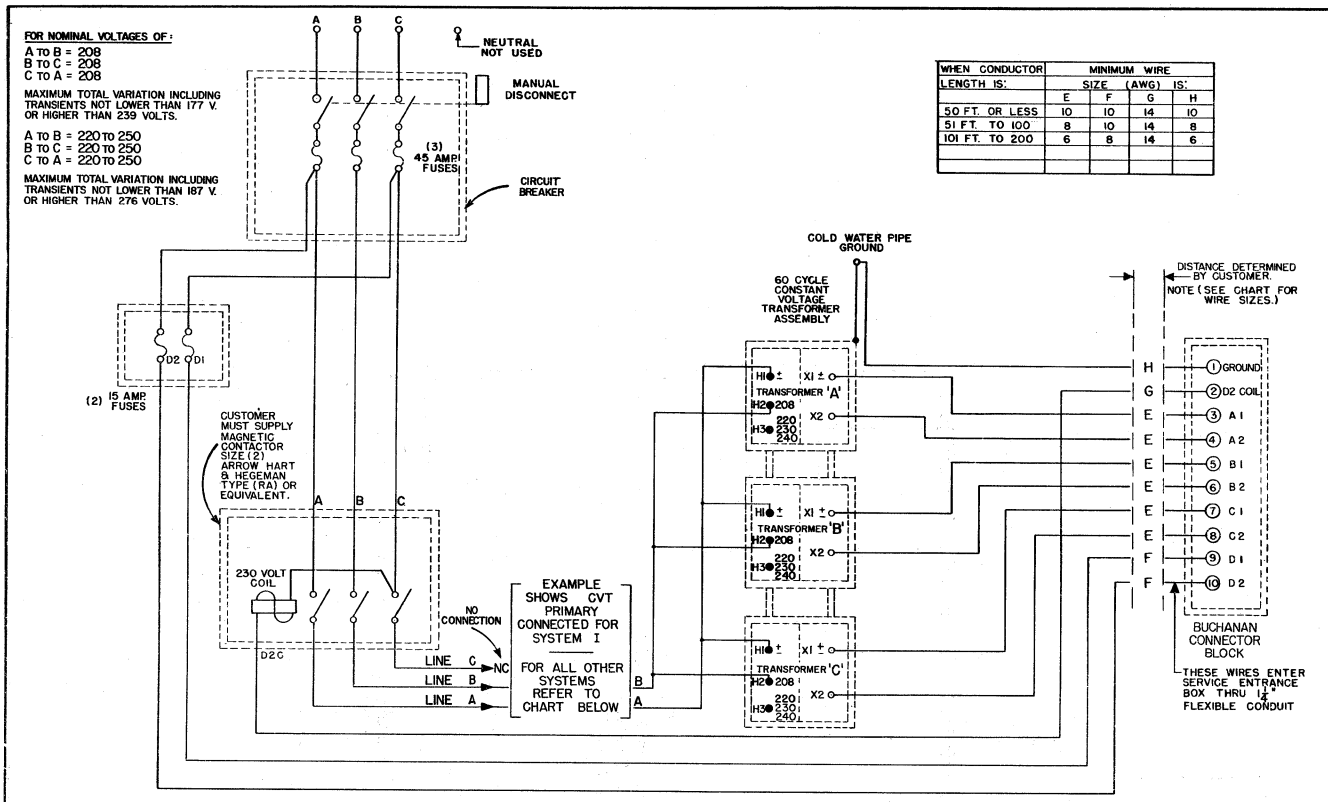
PLATE 8

CONSTANT VOLTAGE TRANSFORMER INSTALLATION

PLATE 9

FIG. 13
PUNCH-REAR
COVER MODIFICATION

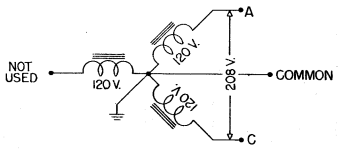




WHEN CONDUCTOR LENGTH IS:	MINIMUM WIRE SIZE (AWG) IS:			
	E	F	G	H
50 FT. OR LESS	10	10	14	10
51 FT. TO 100	8	10	14	8
101 FT. TO 200	6	8	14	6

SYSTEM	I (SHOWN CONNECTED IN DWG. ABOVE)			II				III		IV			V		
LINE	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C
TRANSFORMER 'A'	HI	H2	NC	HI	H3	NC	HI	H3	NC	H2	NC	HI	H3	NC	HI
TRANSFORMER 'B'	HI	H2	NC	HI	H3	NC	HI	H3	NC	HI	H2	NC	HI	H3	NC
TRANSFORMER 'C'	HI	H2	NC	HI	H3	NC	HI	H3	NC	NC	HI	H2	NC	HI	H3

NC=NO CONNECTION



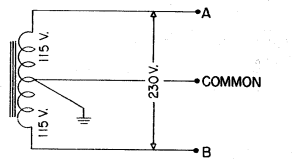
SYSTEM I

SINGLE PHASE OPERATION OF THE COMPUTER ON A THREE PHASE SYSTEM OF 208 VOLTS, 4 WIRE, 60 CYCLES.

TWO WIRES OF THE FOUR WIRE SYSTEM ARE USED, WITH 208 VOLTS ACROSS THE OUTSIDE WIRES. THE REMAINING TWO PHASES ARE NOT USED. THE CENTER WIRE IS FOR VOLTAGE REGULATOR ONLY, IF USED.

EACH WIRE FOR THIS TYPE OF INSTALLATION MUST BE CAPABLE OF CARRYING 40 AMPERES OF CURRENT. FULL LOAD IS 38 AMPERES.

THE COMMON WIRE OF THIS SYSTEM IS GROUNDED.



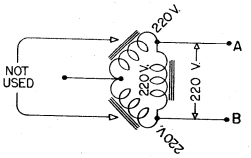
SYSTEM II

SINGLE PHASE OPERATION OF THE COMPUTER ON A SINGLE PHASE SYSTEM OF 230 VOLTS, 3 WIRE, 60 CYCLES.

TWO WIRES OF A THREE WIRE SYSTEM WITH 115 VOLTS FROM CENTER WIRE TO EACH OUTSIDE WIRE WITH 230 VOLTS ACROSS THE OUTSIDE WIRES. THE CENTER WIRE IS FOR VOLTAGE REGULATOR CONNECTION ONLY.

EACH WIRE USED IN THIS SYSTEM MUST BE CAPABLE OF CARRYING 40 AMPERES OF CURRENT. COMPUTER CURRENT IS 36 AMPERES.

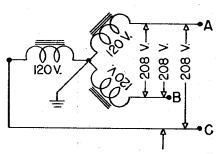
THE COMMON WIRE IS RETURNED TO THE SYSTEM GROUND.



SYSTEM III

SINGLE PHASE OPERATION ON A THREE PHASE SYSTEM OF 220 VOLTS, 3 WIRE, 60 CYCLE (DELTA SYSTEM).

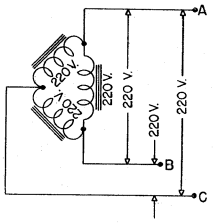
TWO WIRES OF A THREE WIRE SYSTEM ARE USED, WITH 220 VOLTS ACROSS EACH PAIR. NO COMMON GROUND IS USED. WIRES MUST BE CAPABLE OF CARRYING 40 AMPERES OF CURRENT. COMPUTER CURRENT IS 37 AMPERES.



SYSTEM IV

THREE PHASE OPERATION OF THE COMPUTER FROM A THREE PHASE SYSTEM OF 120 VOLTS, 4 WIRE, 60 CYCLES.

THREE WIRES OF THE FOUR WIRES ARE USED, WITH 208 VOLTS ACROSS EACH PAIR OF WIRES. WIRES MUST BE CAPABLE OF CARRYING 30 AMPERES. COMPUTER CURRENT IS 21 AMPERES, PLUS, OR MINUS 2 AMPERES ON EACH LEG.



SYSTEM V

THREE PHASE OPERATION OF THE COMPUTER ON A THREE PHASE SYSTEM OF 220 VOLTS, 3 WIRE, 60 CYCLE (DELTA SYSTEM).

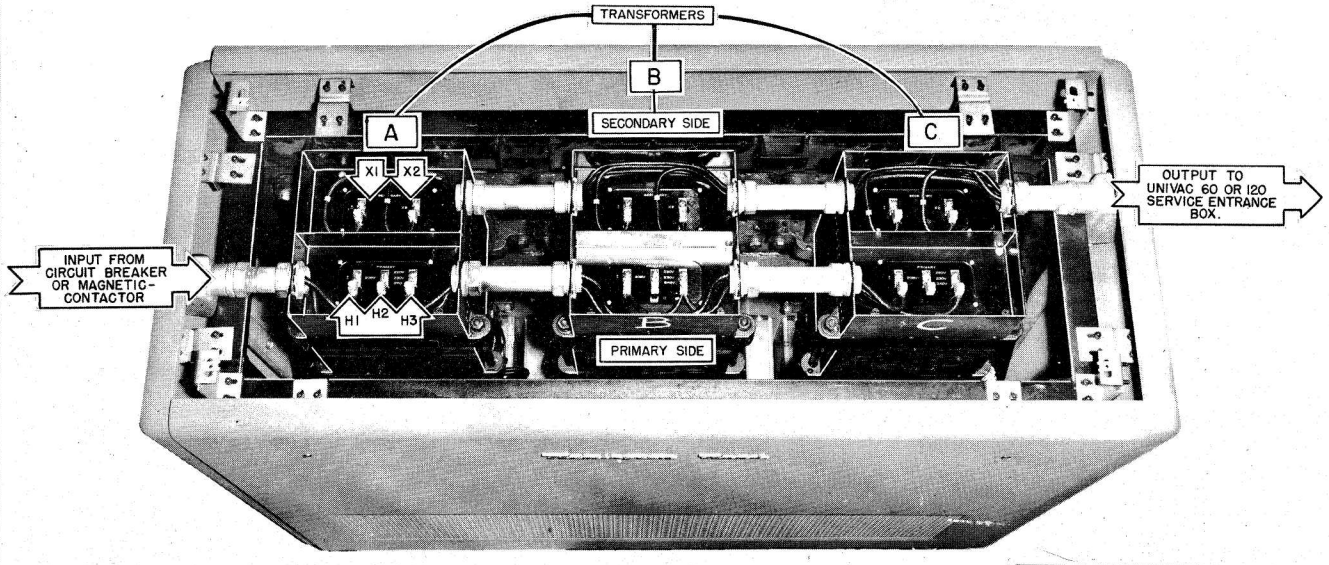
THREE WIRES OF A THREE WIRE SYSTEM ARE USED, WITH - 220 VOLTS ACROSS EACH PAIR OF WIRES. WIRES MUST BE CAPABLE OF CARRYING 30 AMPERES. COMPUTER CURRENT IS 21 AMPERES, PLUS OR MINUS 2 AMPERES ON EACH LEG.

FIG. 14
CVT WIRING.

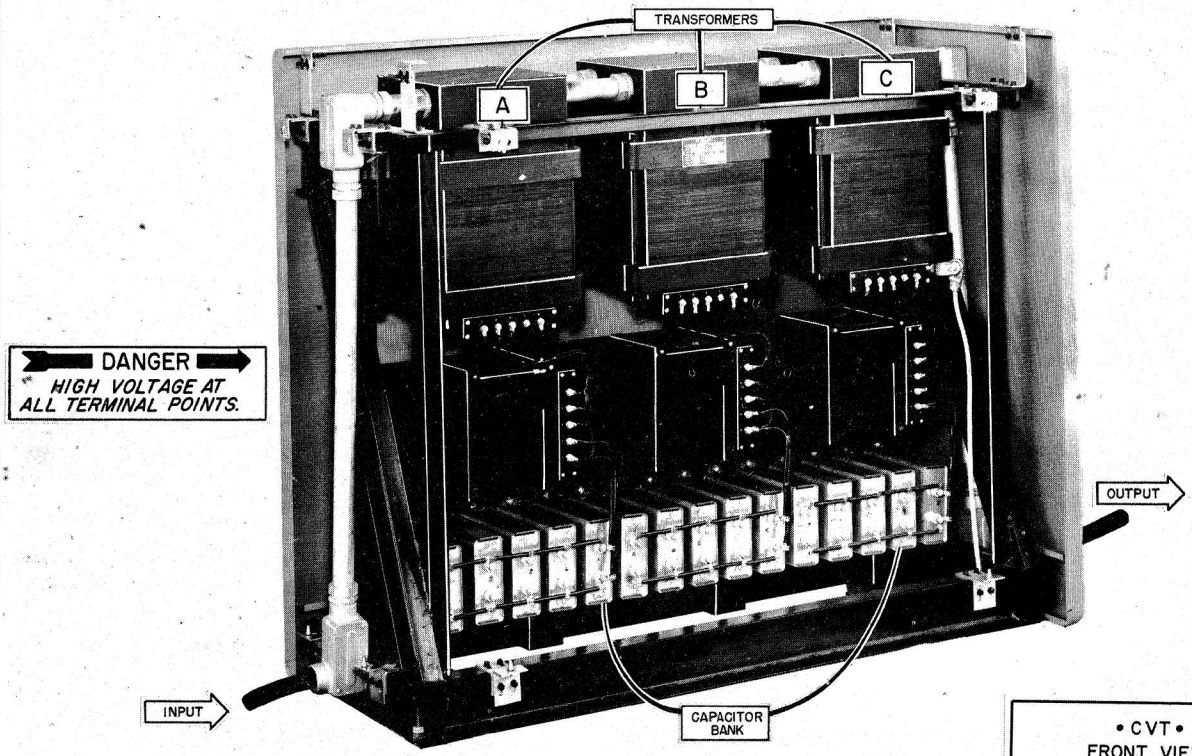
CONSTANT VOLTAGE TRANSFORMER INSTALLATION

PLATE 10

FOR WIRING OF ALL SYSTEMS
SEE FIG. 14



•CVT•
TOP VIEW
FIG. 15



•CVT•
FRONT VIEW
FIG. 16

CONSTANT VOLTAGE TRANSFORMER INSTALLATION

PLATE 11

CONSTANT VOLTAGE TRANSFORMER INSTALLATION

PLATE 12

FIG.17 INSTALLATION SPECIFICATIONS

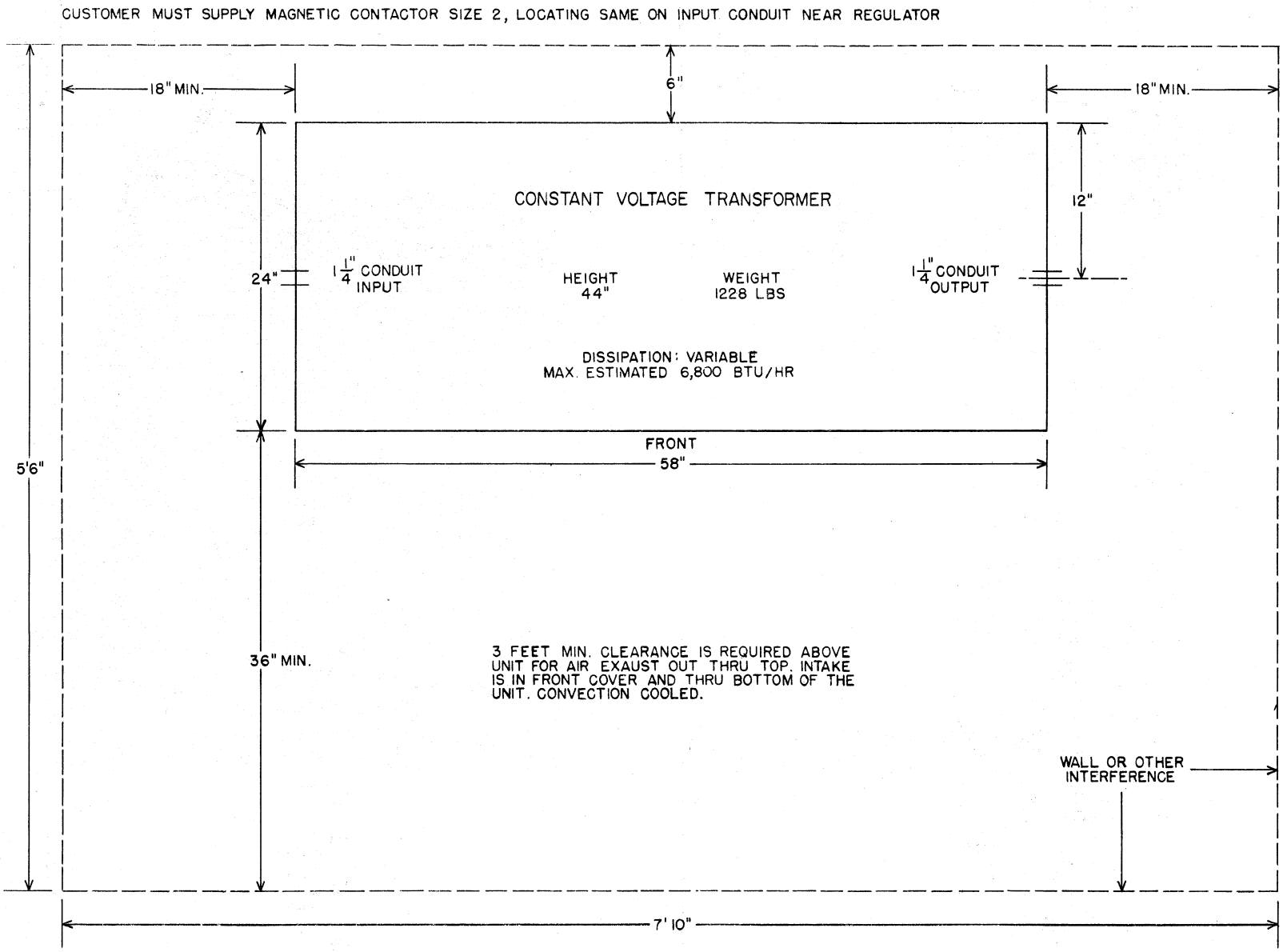


FIG. 18

POWER
DISTRIBUTION BOX
SINGLE PHASE CONNECTIONS –
AFTER CVT HAS BEEN REMOVED

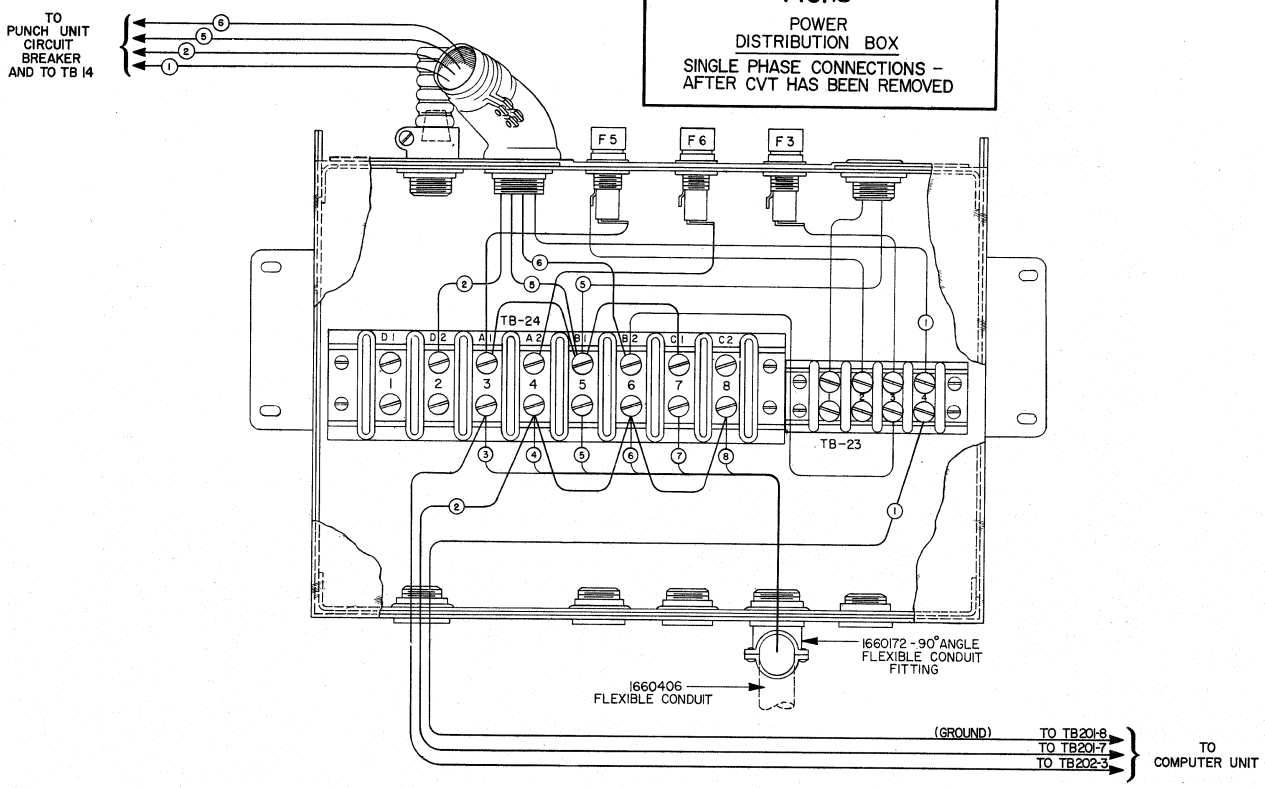
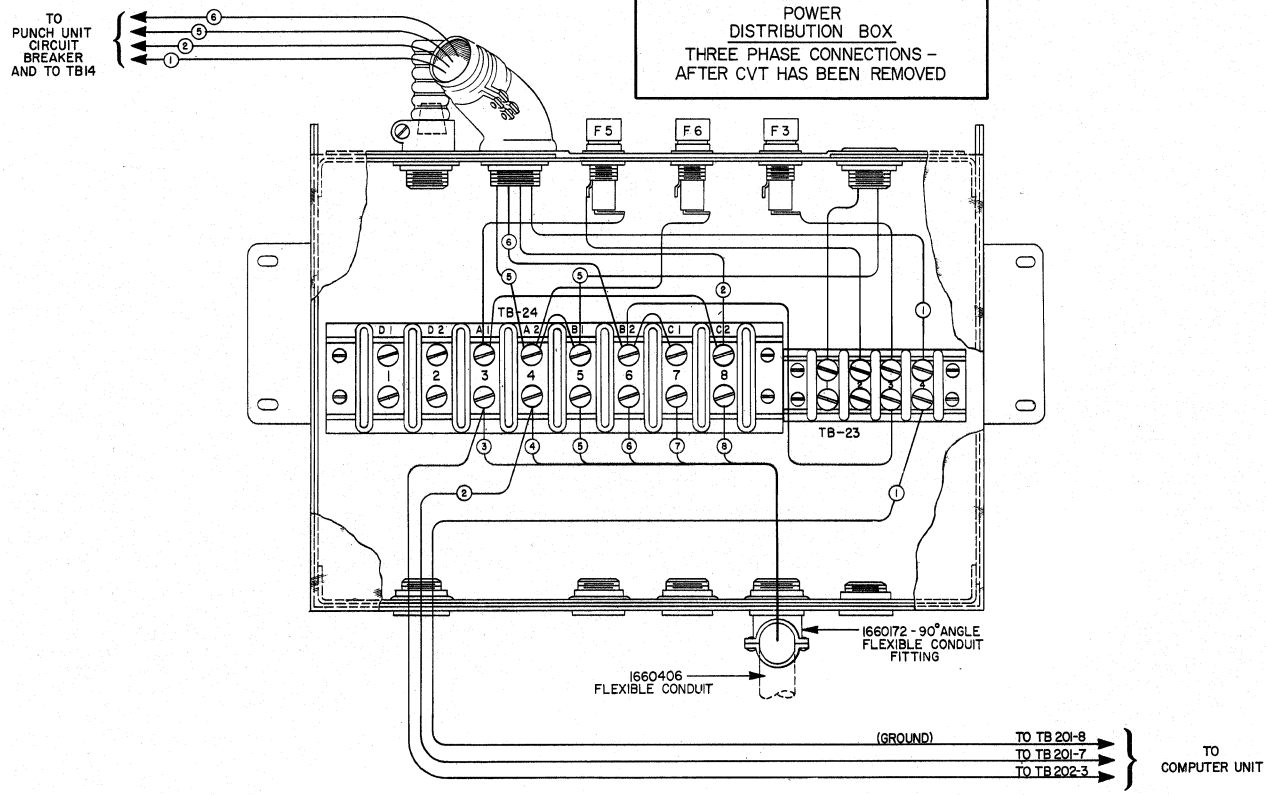
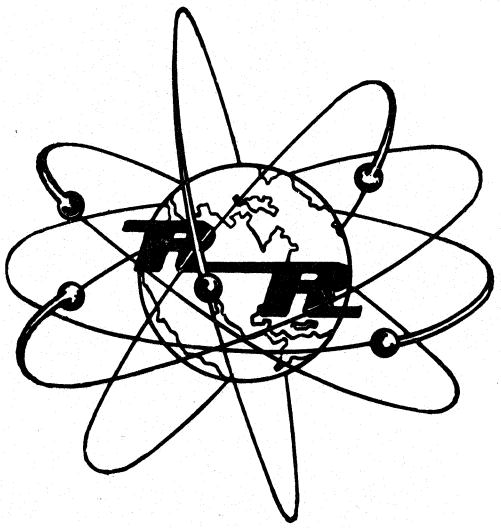


FIG. 19

POWER
DISTRIBUTION BOX
THREE PHASE CONNECTIONS –
AFTER CVT HAS BEEN REMOVED



ELECTRONIC COMPUTER
UNIVAC 60 & 120
SUPPLEMENT II
BUCK BOOST TRANSFORMER



Remington Rand
DIVISION OF SPERRY RAND CORPORATION
315 FOURTH AVENUE
NEW YORK, N. Y.

F O R E W O R D

In some customer installations, computers are expected to operate on 240 or 250 volts either single or three phase. Where this condition exists, high voltage conditions can be corrected through the use of the Buck Boost Transformer, provided the line fluctuation is within plus or minus 5%.

The Buck Boost Transformer is not to be used where the constant voltage transformer regulator is employed.

The complete installation instructions for the Buck Boost Transformer are explained in the following pages.

PLATE DRAWING INDEX

FIGURE TITLE	FIG.	PLATE
Buck Boost Transformer Assembly	1	1
Power Distribution Box - Single Phase Connection	2	2
Power Distribution Box - Three Phase Connection	3	2
Buck Boost Transformer Connections - Single Phase	4	3
Buck Boost Transformer Connections - Three Phase	5	3

ELECTRONIC COMPUTER

UNIVAC 60 & 120

BUCK BOOST TRANSFORMER

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Installation Instructions..... 2
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INSTALLATION INSTRUCTIONS

for the

ELECTRONIC COMPUTER
UNIVAC 60 & 120

BUCK BOOST TRANSFORMER

Remington Rand
DIVISION OF SPERRY RAND CORPORATION
315 FOURTH AVENUE
NEW YORK, N. Y.

INSTALLATION INSTRUCTIONS

Application:

Buck Boost Transformers are used to lower or raise the line voltage a given percentage below or above the nominal voltage. Although they change the voltage, they are not regulators and are not constant voltage transformers. They may be likened to step-down or filament transformers, which have one or more low voltage secondaries.

In some customer installations, machines are expected to operate on 240 or 250 volts, either Single or Three Phase power. This condition exists where a customer is close to a sub-station or where new power distribution lines are installed to replace older obsolete systems.

These high voltage conditions can be corrected through the use of Buck Boost Transformers. In such cases, variations of the line must be measured and if found to have a variation of not more than plus or minus 4% from a listed nominal, then this method of correction may be employed.

Bucking:

In addition to the Univac 60 and 120 nominals of 208, 220 and 230 volts, we can take advantage of the 4 volt adjustment windings (which in themselves are Buck Boost Windings) and operate the Computer on 204, 212, 216, 224, 226 and 234 volts. The use of these taps in conjunction with the Buck Boost Transformers now allows adjustments to 235, 240, 245, 250 and 255 volts. We now have a range of nominal input volts from 208 to 255 volts.

Boosting:

This unit could also be used to boost low voltages by the same percentages as bucking. This is not generally recommended because low voltage conditions are associated with high power line drops, which result in poor (outside of specifications) voltages. In such cases, regulation is required.

Single or Three Phase

The Transformer Assembly may be used for single phase or three phase operation of the Computer on 50 or 60 cycle power. IT SHOULD NOT BE USED IN CONJUNCTION WITH CONSTANT VOLTAGE TRANSFORMERS.

Description:

The Buck Boost Transformer Assembly consists of three transformers fastened to a mounting plate. Each has its own terminal box for connections. The center box is connected by a cable to the Power Distribution Box, into which the Calculating Section power lines are connected to the Sensing-Punching Unit.

The assembly is fastened across the rear of the Sensing-Punching Base Casting, underneath the Receiving Pockets. There are no holes to drill.

Since the location of the Transformers interferes with the mounting of skids during shipment, it must be mounted after the skids are removed by the Maintenance Department.

Parts Ordering:

The Buck Boost Transformer and necessary parts are not available on the standard factory parts order. These items must be ordered through the Sales Department on the regular sales order.

INSTALLATION INSTRUCTIONS

( ) Check each step when completed:

Figure #1

( ) 1. Turn off all power to the machine or remove plug from power source.

( ) 2. Remove lower right side and lower left side covers.

( ) 3. Remove two lower-left cover supports.

( ) 4. Open Service Entrance Box and disconnect 4 power leads.

( ) 5. Remove flexible conduit from bottom of Service Entrance Box.

( ) 6. Remove straight conduit fitting and replace with 90^{o} right angle fitting #1660172.

( ) 7. Reconnect the four leads, in the Service Entrance Box, as they were and tape properly.

( ) 8. Mount Transformer Assembly #1800171 on base as shown in Figure #1 using longer screws #402528.

NOTE: Transformer mounting plate must be placed underneath angle bracket to prevent interference of screws above. Loosen screws and drop vertical Unistrut members down to base casting to prevent interference with the Receiving Pocket door.

Figures #2 & #3

( ) 9. On right side of machine open proper size knockout slug in Power Distribution Box. Use care to remove only the smaller slug.

( ) 10. Install cable coming from Transformer Assembly as shown in Figure #2 & #3.

( ) 11. a. For Single Phase operation, connect leads in Power Distribution Box as shown in Figure #2.

b. For Three Phase operation, connect leads in Power Distribution Box as shown in Figure #3.

( ) 12. a. For Single Phase connections of the Buck Boost Transformer connection Boxes, refer to Figure #4.

b. For Three Phase Connections of the Buck Boost Transformer Connection Boxes, refer to Figure #5.

NOTE: One lead, #12, is used only in Single Phase connections. This lead will be found in one of the Buck Boost Transformer Connection Boxes.

Testing

( ) 13. Turn power on and operate circuit breaker to the "ON" position. Check for correct voltages on TB24. TB24 terminals 3 and 4 are the "A" line; 5 and 6 the "B" line; and 7 and 8 the "C" line. Each pair should now have similar voltages to the others. This may drop slightly due to line impedence when the computer is on.

( ) 14. Depress Computer "ON" button and allow Computer to "Crank Up". With DC "ON" and Punch Motor "ON", check voltages again. When the voltages are correct, make necessary adjustments to the Filament and Plate Transformers to achieve correct filament and D.C. voltages.

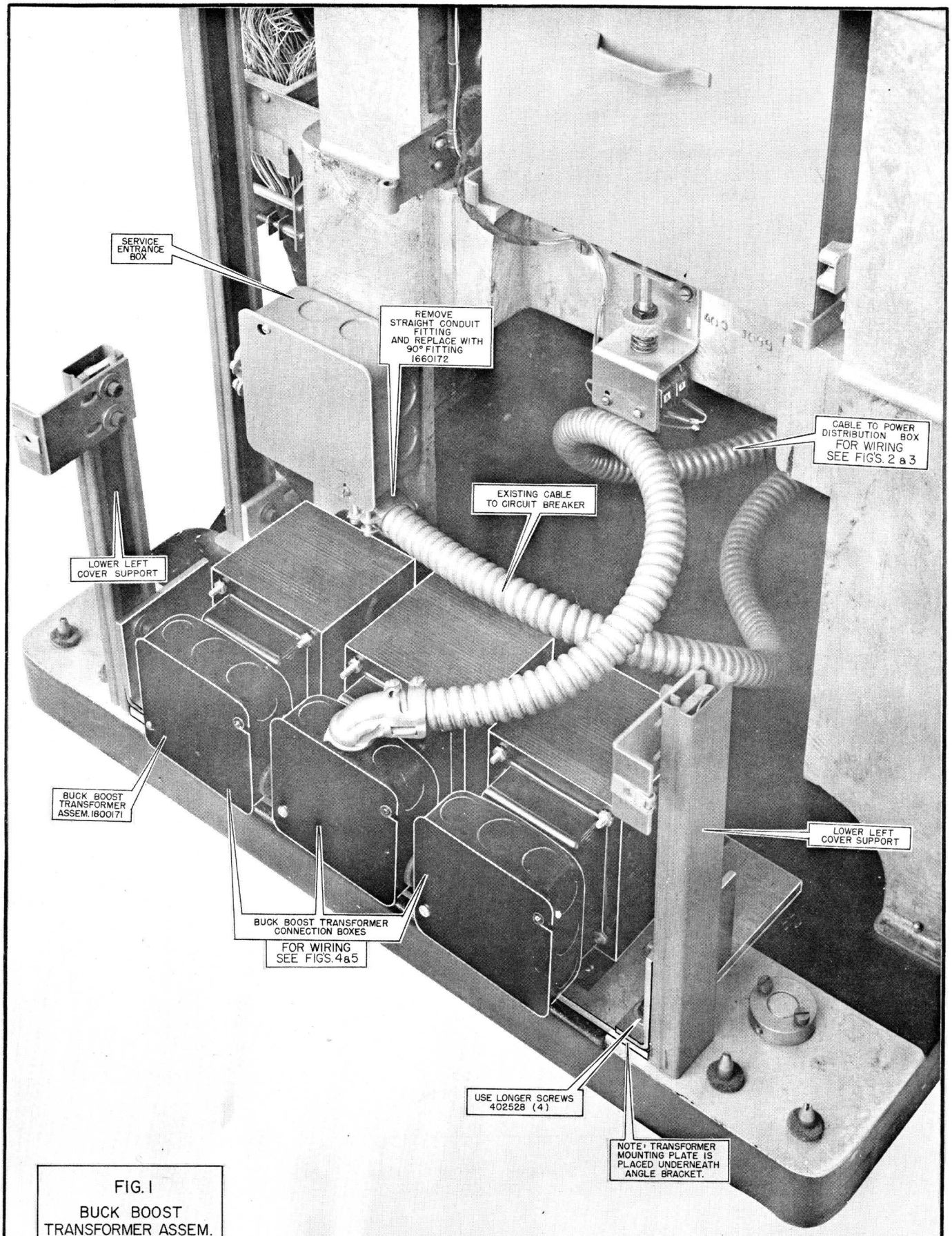
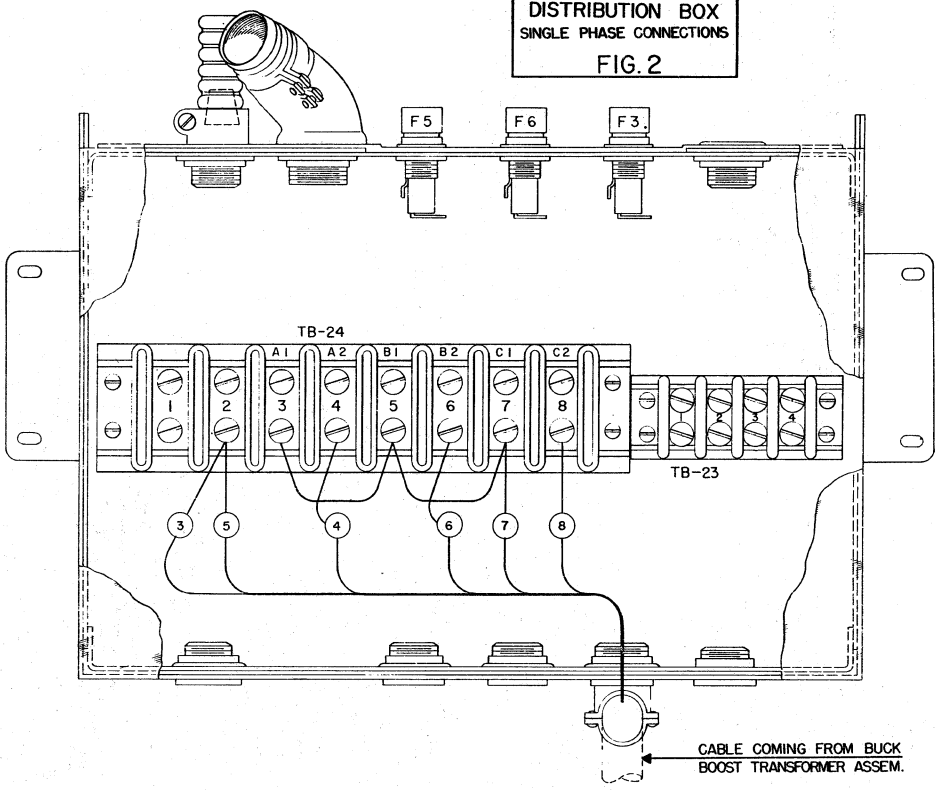


FIG. 1
BUCK BOOST TRANSFORMER ASSEM.

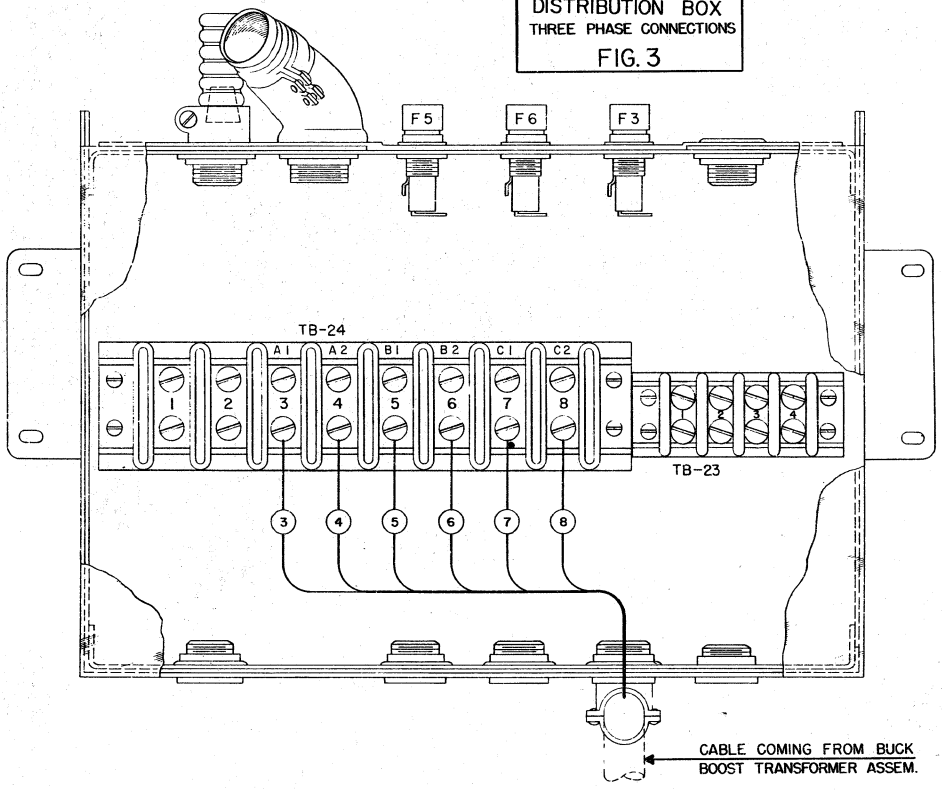
BUCK BOOST TRANSFORMER INSTALLATION

PLATE 1

POWER
DISTRIBUTION BOX
SINGLE PHASE CONNECTIONS
FIG. 2



POWER
DISTRIBUTION BOX
THREE PHASE CONNECTIONS
FIG. 3



BUCK BOOST TRANSFORMER INSTALLATION

PLATE 2

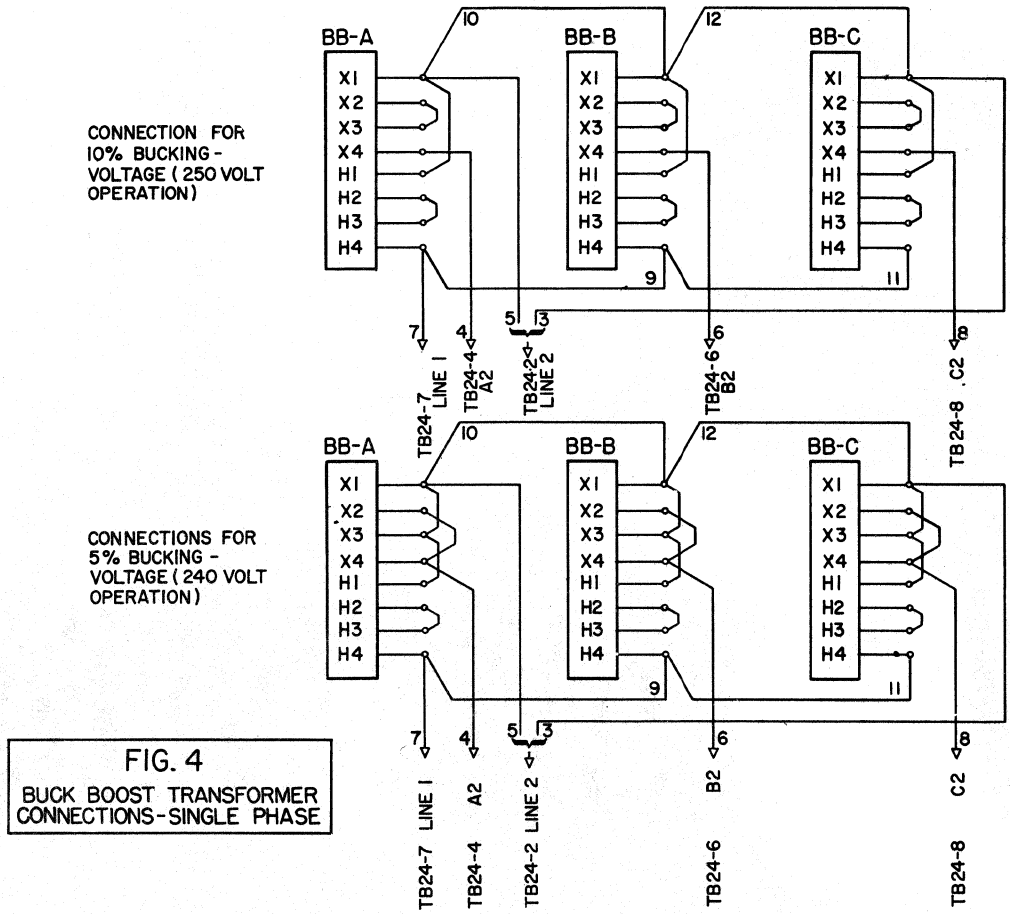


FIG. 4
BUCK BOOST TRANSFORMER CONNECTIONS-SINGLE PHASE

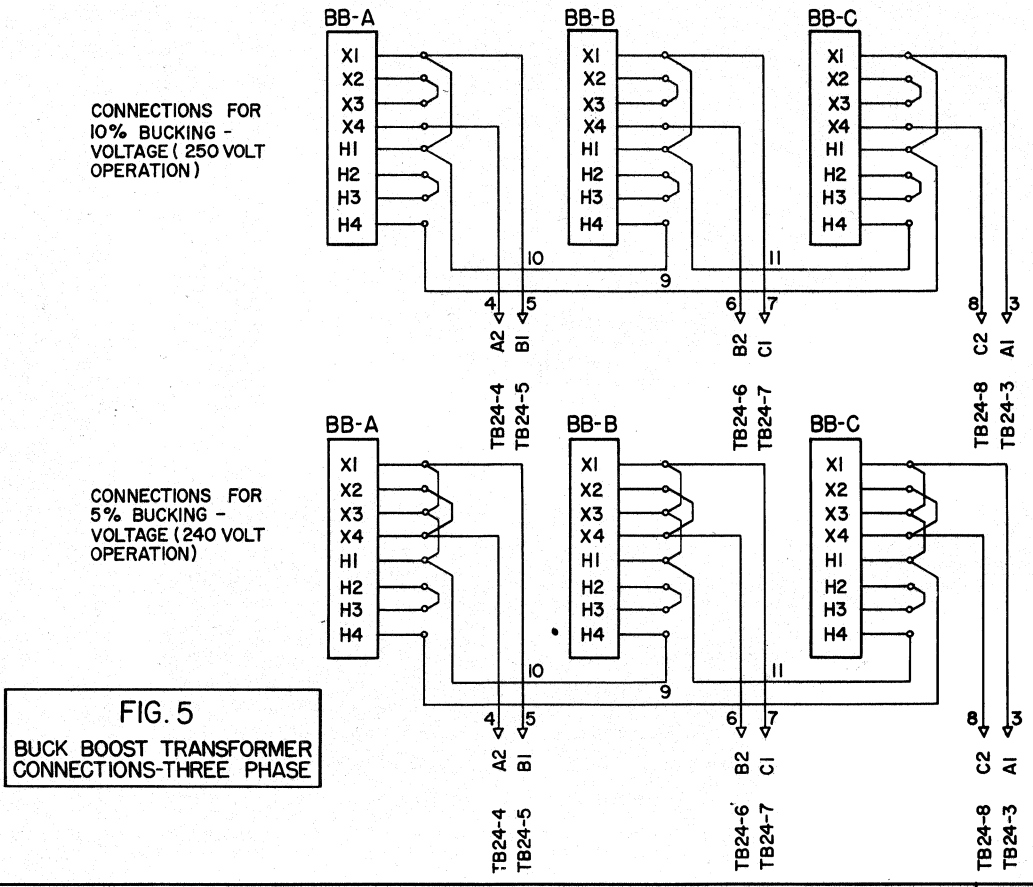


FIG. 5
BUCK BOOST TRANSFORMER CONNECTIONS-THREE PHASE

BUCK BOOST TRANSFORMER INSTALLATION

PLATE 3